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REGULAR ARTICLE

An Analytical Approach of Threshold Voltage Model in Junctionless Field Effect Transistor with Hexagonal Shaped Cross-section

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A novel Double Gate Junctionless Field Effect Transistor structure utilizing a hexagonal design is suggested in this paper. To evaluate the threshold voltage the depletion region width of a hexagonal junctionless transistor is first modeled. Here, 1D Poission's equation is employed under partial depletion conditions. The device's threshold voltage is determined using the device central potential throughout the channel length and the depletion region width. The generated model has been validated by comparing it with the results of TCAD simulations. For comparison, the threshold voltage variation with channel thickness, channel length, gate oxide thickness, dielectric constant of gate dielectric, temperature, drain to source voltage, and work function is studied. The comparison shows the closeness of the model with TCAD simulation results.

Keywords: JLFET, Hexagonal shaped, Depletion width, Threshold voltage.

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1. INTRODUCTION

By Moore's law, transistors have multiplied annually. The most complex computers are consequently constrained by the equation based on transistor count. To ensure compliance with this law, the average Metal Oxide Semiconductor Field Effect Transistor (MOSFET) must be minimized. To increase performance, MOSFET sizes have been gradually reduced. However, reduction in device's size results in various Short Channel Effects (SCE). Within the semiconductor industry, JLFET [1-5] is an amazing device that promotes in VLSI research.

The depletion in a JLFET is caused by the work function differential between the gate and the channel. The gate has higher work function than the channel due to which a negative gate field with respect to the channel is induced. The negative gate field repels the electrons in the channel underneath the gate, thereby generating a depletion region in the channel under the gate. Hence, a high work function gate enables this depletion layer. If the channel is thin, the depletion layer spreads throughout its thickness. When the device is fully depleted no current flows and the device is in off-state. The electric field produced by the work function difference is opposed when a positive gate voltage is provided. At a voltage known as the threshold voltage, the depletion layer begins to disappear and current begins to flow. This condition is called the ON-state and the device starts working. When the applied gate voltage is higher than threshold voltage (V_{th}) the current start flowing. The gate voltage at which the depletion region covers the entire body thickness and the device begins to conduct is known as the threshold voltage. The current increases exponentially with gate voltage. While with drain voltage the current initially increases sharply and finally settles at a constant value.

Table 1 – Brief summary of some existing structures and their techniques

Ref.	Comparison on techniques used
[6]	Graded-doped junctionless-gate-all-around, to determine threshold voltage and subthreshold current
[7]	Quasi-two-dimensional for short-channel junctionless double-gate MOSFETs, to determine threshold voltage and increasing the precision of forecasting changes brought on by short-channel effects.
[8]	Gaussian-like doping profile for DGJLFETs, provides better control over threshold voltage signifying its effect on device performance
[9]	Tri-gate JLFETs, incorporating substrate bias effects threshold voltage was determined
[10]	DGJLFET, variation of threshold voltage due to process changes and doping variation
[11]	Junctionless gate-all-around MOSFETs, effect of doping gradient on subthreshold features and threshold voltage was examined
[12]	Ultra-thin nanotube junctionless double gate-all-around MOSFETs, threshold voltage variation was determined, core-and-outer gate interactions were taken into account
Proposed work	N-channel hexagonal shaped DGJLFET with uniform doping with triangular shaped S-D regions, for high On Current

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This work presents a novel design for Hexagonal-shaped DGJLFETs with triangular S-D section and utilizes minimal central potential for determining device's threshold voltage (V_{th}) expression. The presence of a smaller channel length at the dielectric-semiconductor interface lowers the channel resistance and increases the On state current, while the longer channel length at the center mitigates leakage conduction and controls the Off state current.

2. DEVICE STRUCTURE AND SIMULATION

A hexagonal shaped DGJLFET is studied for simulation analysis. Fig 1. shows the schematic view of the proposed DGJLFET. The source and drain length is $L_s = L_d$ = 5 nm, channel length, $L = 20$ nm, $t_{ox} = 2$ nm, $t_{si} = 10$ nm.

The depletion approximation is taken into account when calculating the threshold voltage (V_{th}) using the device depletion width model as a reference. This formula is used to determine the device's potential along its central axis and the device's threshold voltage is computed by taking the effect of source and drain region into account. The models presented in this study have been simulated and the mathematical results have been compared and verified against TCAD simulation [13] results in order to validate the model.

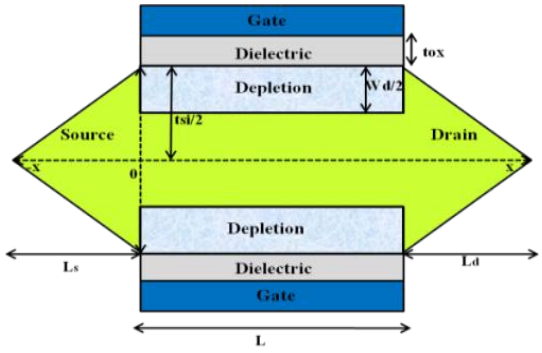


Fig. 1 – Schematic view of hexagonal double gate JLFET

3. ANALYTICAL MODEL

Since the quantity to be modeled is one dimensional, 1-D Poisson's equation has been employed for the mathematical formulation. Since the depletion width varies in the y-direction, depletion width, W_d to be represented in this case is a one-dimensional parameter. Therefore, the synthesis of numerical characterization is done using 1-D Poisson's equation whose expression for the device's channel region is given by Eq. (1) [14],

$$\frac{d^2\phi(y)}{dy^2} = -\frac{qN_d}{\in_{si}} \quad \text{for } n\text{-channel} \qquad (1)$$

where N_d is the donor doping concentration, $\phi(y)$ is the electrostatic potential, and q is a carrier's charge (either an electron or a hole) $\in_{si}$ is silicon's permittivity measurement. Using parabolic trial function method one solution of Poisson's equation can be considered as [14],

$$\phi(y) = C_0 + C_1 y + C_2 y^2 \qquad (2)$$

By taking into account the boundary limitations, the device's hexagonal-shaped JLFET may be solved using Eq.(2). Here, t_{si} is channel thickness. The distance between the device's centre line and surface is regarded as $t_{si}/2$.

At, $y = \frac{(t_{si} - W_d)}{2}$, the potential $\phi(y)$ can be expressed as Eq. (3) [15]

$$\Phi(y) = C_0 + C_1 \left(\frac{t_{si} - W_d}{2}\right) y + C_2 \left(\frac{t_{si} - W_d}{2}\right)^2 y^2 \qquad (3)$$

The values for C_1, C_2 and C_3 can be obtained as [15]

$$C_2 = \frac{\in_{ox}}{\in_{si} t_{ox} W_d}(\phi_{gs} - \phi_s)$$

$$C_1 = -\frac{\in_{ox} (t_{si} - W_d)}{\in_{si} t_{ox} W_d}(\phi_{gs} - \phi_s)$$

$$C_0 = \phi_0 + \frac{\in_{ox} (t_{si} - W_d)^2}{4 \in_{si} t_{ox} W_d}(\phi_{gs} - \phi_s)$$

where t_{ox} is the gate oxide's thickness, $\in_{ox}$ is its permittivity, and ϕ_s is its potential at the surface. Substituting all the values C_0, C_1 and C_2 in Eq.(3) and then putting $y = \frac{t_{si}}{2}$ we get ϕ_s as Eq.(4) [8]

$$\phi_s = \begin{bmatrix} \phi_0 + \frac{\in_{ox} (t_{si} - W_d)^2}{4 \in_{si} t_{ox} W_d}(\phi_{gs} - \phi_s) \\ -\frac{\in_{ox} (t_{si} - W_d)}{2 \in_{si} t_{ox} W_d}(\phi_{gs} - \phi_s) t_{si} \\ +\frac{\in_{ox}}{4 \in_{si} t_{ox} W_d}(\phi_{gs} - \phi_s) {t_{si}}^2 \end{bmatrix} \qquad (4)$$

On solving we get

$$W_d = \frac{-4 \in_{si} t_{ox} q N_d + \sqrt{\left(-4 \in_{si} t_{ox} q N_d\right)^2 - 32 {\in_{ox}}^2 \in_{si} (\phi_{gs} - \phi_0)}}{2 \in_{ox} q N_d} \qquad (5)$$

For the proposed structure, for 0 to $t_{si}/2$,

$$\frac{L_s}{\frac{t_{si}}{2}}\left(\frac{t_{si}}{2} - y\right) = L_{seff}$$

For 0 to $-t_{si}/2$,

$$\frac{L_s}{\frac{t_{si}}{2}}\left(\frac{t_{si}}{2} + y\right) = L_{seff}$$

And also $L_{seff} = L_{deff}$ so the equations of L_{deff} is similar to L_{seff}.

When modelling a device's threshold voltage, we can use the depletion width region model and the expression for W_d is given by Eq. (5). Through the channel length, the central potential is determined as Eq. (6)

$$\phi_0(x)=\left[\frac{(V_{ds}+C\lambda^2)e^{\frac{L+L_{deff}}{\lambda}}-\frac{C\lambda^2}{e^{\frac{L_{seff}}{\lambda}}}}{(e^{2\frac{L+L_{deff}}{\lambda}}-e^{-2\frac{L_{seff}}{\lambda}})}e^{\frac{x}{\lambda}}\right]-\left[\frac{\{(V_{ds}+C\lambda^2)e^{\frac{L+L_{deff}}{\lambda}}-\frac{C\lambda^2}{e^{\frac{L_{seff}}{\lambda}}}\}e^{-2\frac{L_{seff}}{\lambda}}}{(e^{2\frac{L+L_{deff}}{\lambda}}-e^{-2\frac{L_{seff}}{\lambda}})}+\frac{-C\lambda^2(e^{2\frac{L+L_{deff}}{\lambda}}-e^{-2\frac{L_{seff}}{\lambda}})e^{-\frac{L_{seff}}{\lambda}}}{(e^{2\frac{L+L_{deff}}{\lambda}}-e^{-2\frac{L_{seff}}{\lambda}})}e^{-\frac{x}{\lambda}}\right]-C\lambda^2 \quad (6)$$

Where, $\lambda=\sqrt{\frac{t_{si}(4\varepsilon_{si}t_{ox}+\varepsilon_{ox}t_{si})}{8\varepsilon_{ox}}}$ represents the device's scale length [16-17]. When a device's gate bias reaches its threshold voltage level, the device's total depletion is equal to its substrate thickness.

On solving Eq. (5) we obtain,

$$2\in_{ox} qN_d t_{si}+4\in_{si} t_{ox}qN_d=\sqrt{16\in_{si}{}^2 t_{ox}{}^2q^2N_d{}^2-32\in_{ox}{}^2\in_{si}(\phi_{gs}-\phi_0(x))} \quad (7)$$

At, $W_d=t_{si}$, $V_{gs}=V_{Th}$ where, V_{gs} = the gate to source voltage, V_{fb} =flat band voltage and V_{Th} = threshold voltage.

On solving (7) we get

$$\phi_{gs}=\phi_0(x)-\frac{\left[2\in_{ox} qN_d t_{si}+4\in_{si} t_{ox}qN_d\right]^2-16\in_{si}{}^2 t_{ox}{}^2q^2N_d{}^2}{32\in_{ox}{}^2\in_{si}}$$

$$V_{Th}=\phi_{gs}+V_{fb} \quad (8)$$

$$V_{Th}=\phi_0(x)+V_{fb}-\frac{\left[2\in_{ox} qN_d t_{si}+4\in_{si} t_{ox}qN_d\right]^2-16\in_{si}{}^2 t_{ox}{}^2q^2N_d{}^2}{32\in_{ox}{}^2\in_{si}}$$

$$V_{Th}=\left[\frac{(V_{ds}+C\lambda^2)e^{\frac{L+L_{deff}}{\lambda}}-\frac{C\lambda^2}{e^{\frac{L_{seff}}{\lambda}}}}{(e^{2\frac{L+L_{deff}}{\lambda}}-e^{-2\frac{L_{seff}}{\lambda}})}e^{\frac{x}{\lambda}}\right]-\left\{\frac{\{(V_{ds}+C\lambda^2)e^{\frac{L+L_{deff}}{\lambda}}-\frac{C\lambda^2}{e^{\frac{L_{seff}}{\lambda}}}\}e^{-2\frac{L_{seff}}{\lambda}}-}{(e^{2\frac{L+L_{deff}}{\lambda}}-e^{-2\frac{L_{seff}}{\lambda}})}+\frac{C\lambda^2(e^{2\frac{L+L_{deff}}{\lambda}}-e^{-2\frac{L_{seff}}{\lambda}})e^{-\frac{L_{seff}}{\lambda}}}{(e^{2\frac{L+L_{deff}}{\lambda}}-e^{-2\frac{L_{seff}}{\lambda}})}e^{-\frac{x}{\lambda}}\right\}-C\lambda^2 \quad (9)$$

$$+V_{fb}-\frac{\left[2\in_{ox} qN_d t_{si}+4\in_{si} t_{ox}qN_d\right]^2-16\in_{si}{}^2 t_{ox}{}^2q^2N_d{}^2}{32\in_{ox}{}^2\in_{si}}$$

Considering quantum confinement effect, ϕ_{gs} is replaced with ϕ'_{gs}, where ΔV_{th} is the shift in threshold voltage on account of quantum mechanical effects given in Eq. (10) as [17],

$$\Delta V_{th}=\frac{kT}{q}\ln\left(\frac{\alpha\,\mathrm{Erf}(\frac{t_{si}}{2}\sqrt{\frac{q^2N_d}{2\varepsilon_{si}kT}})}{\frac{4\pi kT\,N_d}{h^2\;N_c}[2m^*_{d,1}\Sigma_n e^{\frac{-E_{1,n}}{kT}}+4m^*_{d,2}\Sigma_n e^{\frac{-E_{2,n}}{kT}}]}\right) \quad (10)$$

Equating the central minimum potential to zero,

$$\Phi_{o\,ch\,min}(x)=2(ab)^{1/2}+c=0 \quad (11)$$

$$P=\lambda^2[-2e^{\frac{L+L_{deff}-3L_{seff}}{\lambda}}-e^{\frac{3L+3L_{deff}+L_{seff}}{\lambda}}+e^{\frac{L+L_{deff}-L_{seff}}{\lambda}}+e^{-4\frac{L_{seff}}{\lambda}}+e^{2\frac{L+L_{seff}}{\lambda}}-e^{-2\frac{L_{seff}}{\lambda}}+\frac{1}{4}]$$

$$q=\lambda^2[e^{2\frac{L+L_{deff}-L_{seff}}{\lambda}}-2V_{ds}e^{\frac{L+L_{deff}-3L_{seff}}{\lambda}}-$$

$$V_{ds}e^{\frac{3L+3L_{deff}+L_{seff}}{\lambda}} + V_{ds}e^{\frac{L+L_{deff}-L_{seff}}{\lambda}}]$$

$$r = 2V_{ds}e^{2\frac{L+L_{deff}-L_{seff}}{\lambda}}$$

Solving (11),

$$C = \frac{q - \sqrt{q^2 - 4pr}}{2p}$$

Again,

$$C = -q\frac{N_d}{\varepsilon_{si}} - \frac{1}{\lambda^2}\Phi_{gs} = q\frac{N_d}{\varepsilon_{si}} - \frac{1}{\lambda^2}(V_{th} - V_{fb}) \quad (12)$$

Threshold voltage is the minimum gate to source voltage ge required for current conduction between S-D terminals nd is obtained as,

$$V_{th} = V_{fb} + [\frac{q-\sqrt{q^2-4pr}}{2p} - q\frac{N_d}{\varepsilon_{si}}]\lambda^2 \quad (13)$$

Similarly the flat band voltage can be obtained as,

$$V_{fb} = \frac{q_1-\sqrt{{q_1}^2-4p_1r_1}}{2p} - q\frac{N_d}{\varepsilon_{si}}]{\lambda_1}^2 \quad (14)$$

$$P_1 = {\lambda_1}^4[-2e^{\frac{L+L_{deff}-3L_{seff}}{\lambda_1}} - e^{\frac{3L+3L_{deff}+L_{seff}}{\lambda_1}} + e^{\frac{L+L_{deff}-L_{seff}}{\lambda_1}} + e^{-4\frac{L_{seff}}{\lambda_1}} + e^{2\frac{L+L_{seff}}{\lambda_1}} - e^{-2\frac{L_{seff}}{\lambda_1}} + \frac{1}{4}]$$

$$q_1 = {\lambda_1}^2[e^{2\frac{L+L_{deff}-L_{seff}}{\lambda_1}} - 2V_{ds}e^{\frac{L+L_{deff}-3L_{seff}}{\lambda_1}} - V_{ds}e^{\frac{3L+3L_{deff}+L_{seff}}{\lambda_1}} + V_{ds}e^{\frac{L+L_{deff}-L_{seff}}{\lambda_1}}]$$

$$r = V_{ds}e^{2\frac{L+L_{deff}-L_{seff}}{\lambda_1}}$$

Where, $\lambda_1 = \sqrt{\frac{t_{si}\varepsilon_{si}t_{ox}}{2\varepsilon_{ox}}}$

5. RESULTS AND DISCUSSION

In Fig. 2, the variation of V_{th} with channel thickness is displayed and as the channel thickness increases, channel resistance decreases and degrades gate control at the center, causing decrease in threshold voltage. Fig. 3 shows shorter channel length results in lower threshold voltage. Fig. 4 shows the variation of V_{th} with temperature and it is evident that the threshold voltage falls as the temperature increases. Fig. 5 shows the V_{th} fluctuation with gate oxide thickness, showing that a thicker oxide results in a lower threshold voltage due to reduced gate control. A graph of the threshold voltage is shown for different drain-to-source voltages in Fig. 6 It is demonstrated that the threshold voltage drops with increase in drain-to-source voltage. Fig. 7 illustrates the influence of gate work function on the threshold voltage, showing a progressive increase in threshold voltage with increasing gate work function.

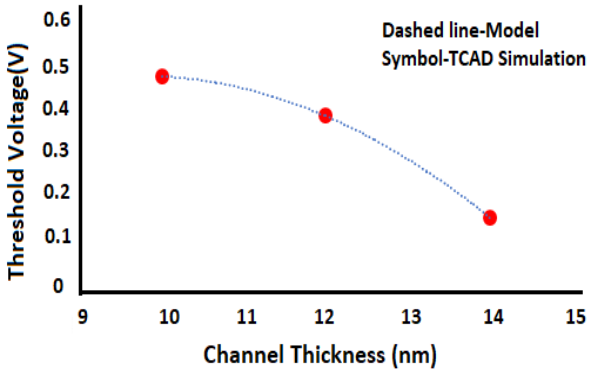


Fig. 2 – Threshold voltage vs channel thickness (nm)

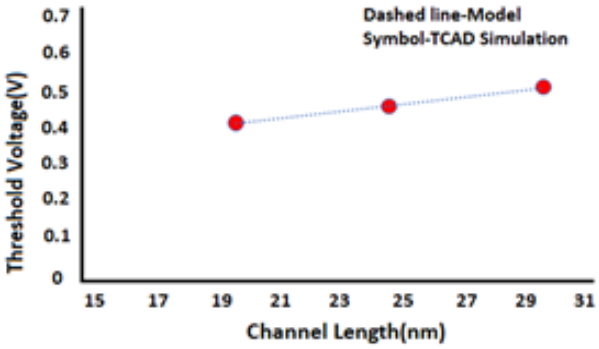


Fig. 3 – Threshold voltage vs channel length(nm)

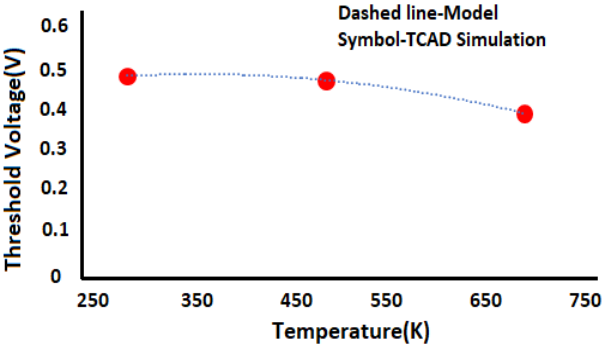


Fig. 4 – Threshold voltage vs temperature (K)

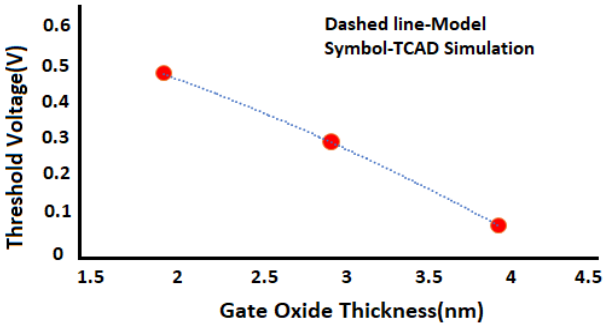


Fig. 5 – Threshold voltage vs gate oxide thickness (nm)

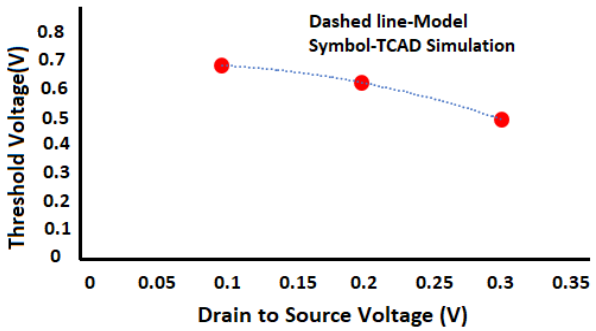


Fig. 6 – Threshold voltage vs drain to source voltage (V)

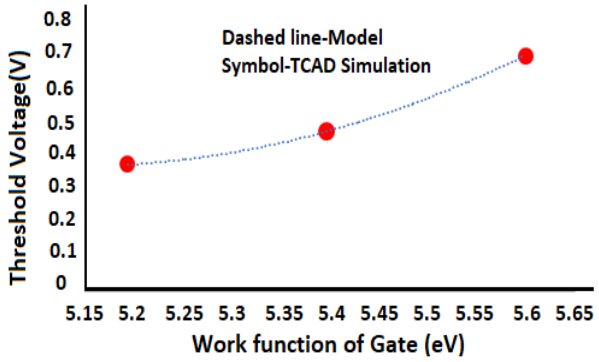


Fig. 7 – Threshold voltage vs work function of gate (eV)

Table 2 – Comparison of proposed work with some existing models

Parameters	Threshold Voltage (V)	
	[15, 18]	Proposed Work
Temperature (300 K)	0.47-0.6	0.46
Work Fn (5.4 eV)	0.47-0.6	0.46
V_{ds} (0.8 V)	0.47-0.6	0.4

6. CONCLUSION

The threshold voltage for the proposed model is derived using the depletion width expression. A brief explanation of threshold voltage is presented here and simulations with TCAD are used to validate the model. The new double gate hexagonal JLFETs threshold voltage is thus computed in this paper, and the results of TCAD simulations validate the model's accuracy. To ascertain the threshold voltage, the model is also exposed to the minimum potential technique method. The suggested hexagonal structure's threshold voltage variation with channel thickness, channel length, temperature, gate dielectric thickness, gate dielectric constant, drain to source voltage and gate work function has been computed and various out comes have been plotted.

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Аналітичний підхід до моделювання порогової напруги в безперехідному польовому транзисторі з поперечним перерізом шестикутної форми

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У статті запропоновано нову структуру польового транзистора з подвійним затвором і без p-n-переходів (junctionless), що має шестикутну конфігурацію. Для визначення порогової напруги спочатку моделюється ширина збідненої області такого транзистора. При цьому використовується одновимірне рівняння Пуассона в умовах часткового збіднення. Порогова напруга пристрою визначається на основі потенціалу в центральній частині каналу (уздовж усієї його довжини) та ширини збідненої області. Розроблена модель була перевірена шляхом порівняння з результатами моделювання за допомогою

інструментів TCAD. У рамках цього порівняння досліджено залежність порогової напруги від таких параметрів, як товщина та довжина каналу, товщина оксиду затвора, діелектрична проникність діелектрика затвора, температура, напруга між стоком і витоком, а також робоча функція виходу. Результати порівняння демонструють високу точність моделі порівняно з даними TCAD-моделювання.

Ключові слова: JLFET, Шестикутна форма, Ширина збідненої області, Порогова напруга.