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REGULAR ARTICLE

Performance Enhancement of an InAs Source/Pocket Dual-Source Trench Gate Tunnel Field-Effect Transistor Using an HfO_2 Filled Cavity: A TCAD Investigation

R. Kiruthika[1], S. Ashok Kumar[1,*], J. Charles Pravin[2]

[1] *Department of ECE, Karpagam Academy of Higher Education, Tamil Nadu, India*
[2] *Department of ECE, Kalasalingam Academy of Research and Education, Tamilnadu, India*

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Tunnel field-effect transistors (TFETs) are widely recognized as potential alternatives to conventional MOSFETs for low-power applications because they exhibit ultra-low leakage current and excellent subthreshold performance. However, the large bandgap of silicon suppresses the BTBT rate at the source-channel junction, thereby restricting the achievable ON-state current. This work proposes an InAs-based Dual-Source Trench Gate Tunnel Field-Effect Transistor (DSTGTFET) in which the silicon sources and pocket are replaced with Indium Arsenide (InAs), and the conventional air cavity is filled with HfO_2. The device was designed and evaluated using Synopsys Sentaurus TCAD with the models drift–diffusion transport model, dynamic non-local Kane BTBT model, Shockley–Read–Hall (SRH) recombination, Fermi–Dirac statistics, bandgap narrowing, and mobility degradation. The influence of HfO_2 cavity thickness was investigated by varying it from 4 nm to 13 nm. The optimized device with a 9 nm cavity achieved an ON-state current of 6.5×10^{-5} A, an OFF-state current of 3.27×10^{-16} A, and an I_{ON}/I_{OFF} ratio of approximately 2×10^{11}. The threshold voltage was reduced from 0.75 V to 0.69 V, indicating improved switching characteristics. The enhanced performance is attributed to the combined effect of the InAs source/pocket and the HfO_2-filled cavity, which improve carrier tunneling and gate control. These results demonstrate the suitability of the proposed device for future low-power and high-performance integrated circuit applications.

Keywords: TFET, InAs, DSTGTFET, BTBT, TCAD.

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1. INTRODUCTION

TFET have emerged as one of the promising alternatives to conventional MOSFET, for future low-power integrated circuits because current conduction is occurs through band-to-band tunneling (BTBT) instead of thermionic emission and also TFET provide very low OFF-state leakage current and a steep subthreshold swing, making them attractive for energy-efficient applications and the performance of conventional silicon TFET is still constrained by their low ON-state current provided in [1]. The wide bandgap and larger carrier effective mass property of silicon results reduction in BTBT generation rate and limiting the current drive capability of the device.

To overcome this problem, where the air cavity in trench-gate TFET biosensors was replaced by dielectric materials to alter the electric field distribution near the tunneling junction was discussed in the given reference, this method increased the interaction between the gate and channel while maintaining negligible leakage current. Then the dual source concept with trench gate structure formulates additional junctions for resulting larger tunneling rate comparing with conventional single-source configurations are discussed in [2]. Further optimization of the trench geometry and dielectric arrangement produced a more uniform electric field distribution and improved the transfer characteristics of the device given in [3, 4] and the silicon TFETs confirmed the feasibility of BTBT-based switching under low operating voltages, providing a reliable foundation for device modelling and TCAD calibration done experimentally that results are discussed in [5].

Among the above materials, engineering also becomes one of the most effective approaches for overcoming the current limitation of silicon TFETs. III–V semiconductors [6, 7], particularly InAs and GaSb, provide a narrower bandgap and lower carrier effective mass than silicon [8] and allowing electrons to tunnel more easily across the source-channel junction [9]. The different high-k gate dielectrics with source-pocket engineering are investigated in [10] additionally with heterojunction device structural implementation reshapes the electric field profile and shorten the tunnelling distance are addressed in [11], advanced device restructure developments strategies with vertical device architectures outlined in [12], dual-source configurations examined in [13], and dual-channel trench-gate structures discussed in [14] this leads to higher ON-state current, lower threshold voltage, and improved switching response are focused in [15]. Eventhough things that work investigates and concentrate an InAs-based Dual-Source Trench Gate Tunnel Field-Effect Transistor (DSTGTFET) by replacing the conventional

* Correspondence e-mail: 6691ashok@gmail.com

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silicon source and pocket regions with InAs and substituting the air-filled trench cavity with a high-k HfO_2 dielectric. The device is analyzed by using Synopsys Sentaurus TCAD to investigate the influence of HfO_2 cavity thickness on gate electrostatic control, band-to-band tunneling efficiency, threshold voltage, and current transport. The case study identifies that optimum cavity thickness for achieving enhanced switching performance and demonstrates the potential of the developed architecture for future ultra-low power and high-performance integrated circuit applications. The rest of this paper has been dividing into the following sections Device Structure Results and Discussions.

2. DEVICE STRUCTURE

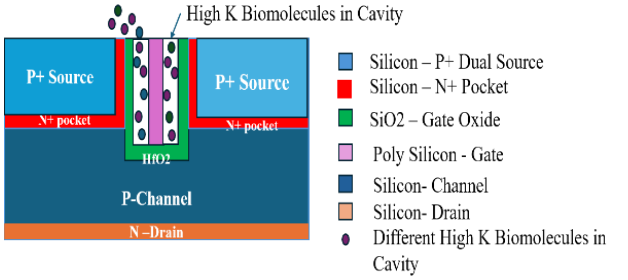


Fig. 1 – Schematic diagram of Conventional DM-DSTGTFET [2]

Article Structure and the corresponding Styles

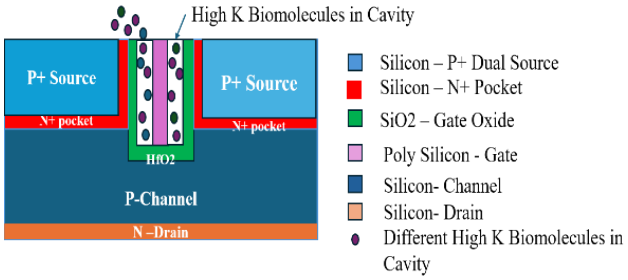


Fig. 2 – Schematic diagram of Proposed InAs/HfO_2 DM-DSTGTFET

Fig. 1 shows the validated conventional DM-DSTGTFET, which serves as the reference device [2]. Fig. 2 illustrates the proposed InAs-DSTGTFET, where the silicon sources and pockets are replaced with an InAs and the air cavity is replaced with HfO_2 [6], while all other structural dimensions remain unchanged for a fair comparison. The device consists of two P^+ InAs source regions, N^+ InAs pockets, a lightly doped P-type silicon channel, and an N-type silicon drain. The channel height, drain height, pocket thickness, gate oxide thickness, and source oxide thickness are 37 nm, 18 nm, 5 nm, 1 nm, and 2 nm, respectively [2-4]. The cavity thickness is varied from 4 nm to 13 nm, the gate work function is 4.2 eV (optimized to 4.6 eV), and the source, pocket, channel, and drain doping concentrations are 1×10^{20}, 1×10^{19}, 1×10^{15}, and 1×10^{17} cm^{-3}, respectively [2].

The proposed device was simulated using Synopsys Sentaurus TCAD. The simulations employed the drift–diffusion transport model, dynamic non-local Kane BTBT model, SRH recombination, Fermi–Dirac statistics, bandgap narrowing, and mobility degradation models [2, 3]. The electrical transfer characteristics were obtained by varying the gate voltage from 0 to 1.5 V under a fixed drain bias of 0.5 V. A refined non-uniform mesh was applied near the tunneling junction, and the InGaAs material database was calibrated to represent the electrical properties of an InAs.

3. RESULTS AND DISCUSSION

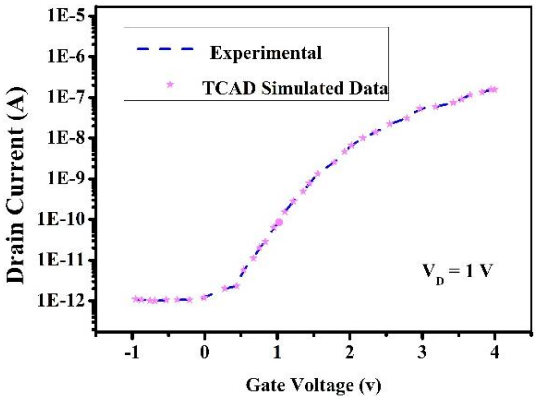


Fig. 3 – Comparison of simulation model with prefabricated TFET [5]

Fig. 3 compares the published transfer characteristics of the prefabricated TFET, with the corresponding Synopsys Sentaurus TCAD simulation results at V_D = 1 V. The close agreement between the two curves confirms the accuracy of the calibrated TCAD model and the adopted physical models [5].

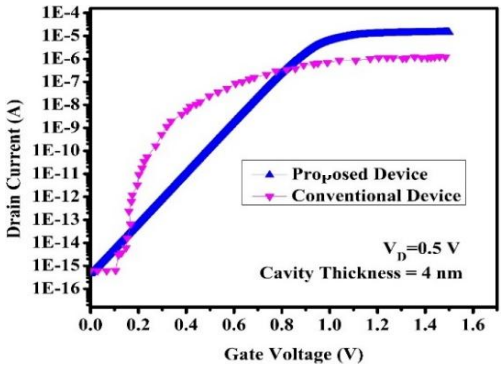


Fig. 4 – Transfer characteristics Comparison of Proposed model with Conventional DM-TGTFET [2]

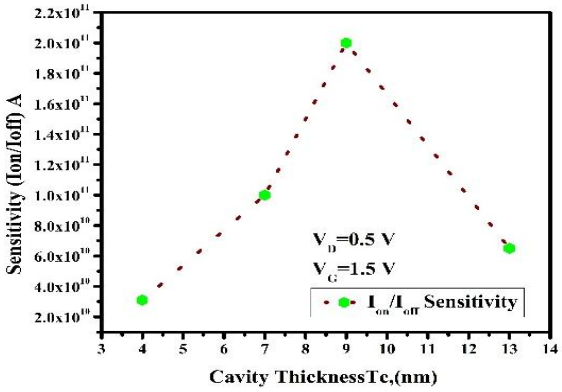


Fig. 5 – I_{ON}/I_{OFF} Sensitivity of Proposed model with different Cavity Thickness at V_D = 0.5 V and V_G = 1.5 V

The exponential increase in drain current (I_D) with gate voltage reflects the dominant band-to-band tunnelling (BTBT) transport mechanism. henceforth, the validated simulation framework is implemented to evaluate the proposed InAs/HfO_2 DSTGTFET.

Fig. 4 compares the transfer characteristics of the conventional silicon-based TFET and the InAs/HfO_2 DSTGTFET at $V_D = 0.5$ V with a cavity thickness of 4 nm. Both devices exhibit an ultra-low OFF-state current of approximately 4.5×10^{-16} A, indicating excellent leakage suppression. Fig. 5 illustrates the variation of the I_D with HfO_2 cavity thickness at $V_D = 0.5$ V and $V_G = 1.5$ V. The I_D increases from 1.4×10^{-5} A to 6.5×10^{-5} A as the cavity thickness increases from 5 nm to 9 nm, owing to enhanced gate electrostatic control and improved BTBT tunneling. Beyond 9 nm, the I_D decreases to approximately 3.2×10^{-5} A because the thicker dielectric weakens the gate-to-channel coupling and reduces the tunneling efficiency. Therefore, a 9 nm HfO_2 cavity thickness provides the optimum electrical performance for the presented device.

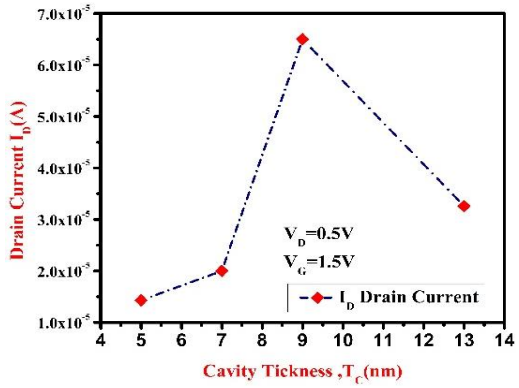


Fig. 6 – Effect of Proposed model with different Cavity Thickness at $V_D = 0.5$ V and $V_G = 1.5$ V on I_{ON}

The proposed device achieves a substantially higher ON-state current of approximately 6.5×10^{-5} A (From Fig. 6 at 9 nm cavity thickness (T_C), compared with 10^{-6} A for the conventional device, owing to the enhanced band-to-band tunneling provided by the InAs source/pocket and improved gate electrostatic control from the HfO_2-filled cavity. Therefore, the presented structure exhibits a higher I_{ON}/I_{OFF} ratio and improved switching performance, demonstrating the effectiveness of the optimized material engineering approach.

Fig. 6 illustrates the variation of the I_D with HfO_2 filled different cavity thickness at $V_D = 0.5$ V and $V_G = 1.5$ V. The I_D increases from 1.4×10^{-5} A to 6.5×10^{-5} A as the cavity thickness increases from 5 nm to 9 nm, owing to enhanced gate electrostatic control and improved band-to-band tunnelling [13, 14]. Beyond 9 nm, the drain current decreases to approximately 3.2×10^{-5} A because, the thicker dielectric weakens the gate-to-channel coupling and reduces the tunneling efficiency. Therefore, a 9 nm HfO_2 cavity thickness provides the optimum electrical performance for the novel device.

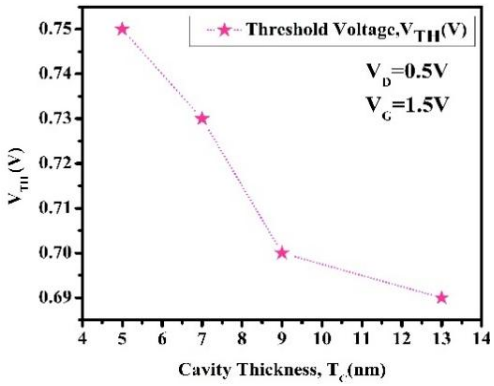


Fig. 7 – V_{TH} of investigated model with different Cavity Thickness at $V_G = 1.5$ V, $V_D = 0.5$ V and $k = 23$

Fig. 7 illustrates the variation of the threshold voltage (V_{TH}) with HfO_2 filled cavity thickness range from 4 nm, 7 nm, 9 nm and 13 nm at $V_D = 0.5$ V. The threshold voltage decreases from 0.75 V at 5 nm to 0.69 V at 13 nm, indicating improved gate control as the cavity thickness increases. A more pronounced reduction is observed between 7 nm and 9 nm, whereas a marginal change occurs beyond 9 nm. This behaviour indicates that a 9 nm HfO_2 cavity provides the optimum balance between reduced threshold voltage and enhanced switching performance for the modified InAs-DSTGTFET.

4. CONCLUSION

An InAs-based Dual-Source Trench Gate Tunnel Field-Effect Transistor (DSTGTFET) with an HfO_2-filled cavity was designed and evaluated using Synopsys Sentaurus TCAD. Replacing the conventional silicon sources and pockets an InAs significantly, improved the BTBT efficiency and enhanced the device performance. The effect of HfO_2 cavity thickness was investigated over the range of 4-13 nm, with 9 nm identified as the optimum thickness. At this condition, the device achieved an I_{ON} of 6.5×10^{-5} A, an I_{OFF} of 3.27×10^{-16} A, and an I_{ON}/I_{OFF} ratio of approximately 2×10^{11}, while the threshold voltage decreased from 0.75 V to 0.69 V. The improved electrical characteristics are attributed to enhanced carrier tunneling and stronger gate electrostatic control. It is noted that demonstrate InAs/HfO_2 DSTGTFET is a promising device architecture for future ultra-low-power, high-speed, and energy-efficient integrated circuit applications.

DECLARATION OF COMPETING INTEREST

The authors declare that they have no known

ACKNOWLEDGEMENTS

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DATA AVAILABILITY

Data will be made available on request.

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Підвищення ефективності тунельного польового транзистора з траншейним затвором, що має подвійне джерело, на основі InAs, шляхом використання порожнини, заповненої HfO_2: дослідження методом TCAD

R. Kiruthika[1], S. Ashok Kumar[1], J. Charles Pravin[2]

[1] *Department of ECE, Karpagam Academy of Higher Education, Tamil Nadu, India*
[2] *Department of ECE, Kalasalingam Academy of Research and Education, Tamilnadu, India*

Тунельні польові транзистори (TFET) розглядаються як перспективна альтернатива традиційним польовим транзисторам із ізольованим затвором (MOSFET) у пристроях з низьким енергоспоживанням, оскільки вони характеризуються наднизькими струмами витоку та відмінними підпороговими характеристиками. Однак велика ширина забороненої зони кремнію обмежує швидкість міжзонного тунелювання (BTBT) на межі розділу «джерело – канал», що, своєю чергою, обмежує максимально досяжний струм у відкритому стані. У цій роботі запропоновано тунельний польовий транзистор із двома джерелами та траншейним затвором (DSTGTFET) на основі арсеніду індію (InAs), у якому кремнієві джерела та області «кишень» (pockets) замінено на InAs, а традиційна повітряна порожнина заповнена діоксидом гафнію (HfO_2). Проектування та оцінювання характеристик пристрою здійснювалися за допомогою програмного забезпечення Synopsys Sentaurus TCAD із використанням таких моделей: дрейфово-дифузійного перенесення, динамічної нелокальної моделі BTBT Кейна, рекомбінації Шоклі–Ріда–Холла (SRH), статистики Фермі–Дірака, а також моделей звуження забороненої зони та деградації рухливості носіїв заряду. Досліджено вплив товщини порожнини, заповненої HfO_2, шляхом її варіювання в діапазоні від 4 нм до 13 нм. Оптимізований пристрій із товщиною порожнини 9 нм продемонстрував струм у відкритому стані $6{,}5 \times 10^{-5}$ А, струм у закритому стані $3{,}27 \times 10^{-16}$ А та відношення струмів у відкритому й закритому станах (I_{ON}/I_{OFF}) приблизно 2×10^{11}. Порогова напруга знизилася з 0,75 В до 0,69 В, що свідчить про покращення характеристик перемикання. Покращені робочі характеристики досягаються завдяки поєднанню використання InAs у джерелах/«кишенях» та наявності порожнини, заповненої HfO_2, що сприяє ефективнішому тунелюванню носіїв заряду та кращому керуванню з боку затвора. Отримані результати підтверджують доцільність застосування запропонованого пристрою в інтегральних схемах майбутнього, що потребують низького енергоспоживання та високої продуктивності.

Ключові слова: TFET, InAs, DSTGTFET, BTBT, TCAD.