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REGULAR ARTICLE

Benchmarking Performance of a Double Gate CNTFET Against the GNRFET with Schottky Contact

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Graphene Nano Ribbon Field Effect Transistor (GNRFET) and Carbon Nano Tube (CNTFET) are emerging technologies that have received a lot of attention in recent years. They are being extensively investigated as possible candidates for replacing silicon-channel devices in the next-generation integrated circuits and systems. Both devices represent attractive physical properties for electronic applications and can be used to overcome the different physical limits and several drawbacks, including high leakage current (I_{OFF}), short-channel effects (SCEs), and increase of the threshold voltage (V_{TH}) and velocity saturation.

The effect of the lateral spacing parameter on the reliability of the device is necessary to be considered because it directly dictates the parasitic capacitances. In this paper, we compare the two varieties of both de-vices and explore their respective strengths in terms of the leakage current (I_{OFF}) and the I_{ON} current using the Schottky contact. The numerical modeling is performed using the non-equilibrium Green's function formalism (NEGF) to describe quantum transport in both devices. The 3D quantum simulation study covers transfer characteristics, transconductance, potential profiles, and transmission coefficients used to extract the performance ratio using the Nano TCAD Vides tool. The novelty of this paper is to present a better de-vice performance using the lateral spacing parameter optimization on both devices. The results of this simulation confirm that increasing the lateral spacing parameter in-creases the I_{ON} current by 15.2 % and 4.20 % for CNTFET and GNRFET, respectively. The study of this paper reveals that the CNTFET de-vice is more attracted to designing the speed CMOS circuit with lower power consumption under optimal parameters presented here.

Keywords: CNTFET, GNRFET, Lateral spacing, Leakage current.

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1. INTRODUCTION

Even though conventional Si-CMOS devices have dominated the semiconductor industry for decades, the challenges posed by the incredibly small feature sizes and the scaling length such as increased wire resistivity, significant mobility degradation, leakage current degradation, decreasing the performance ratio and large dopant fluctuations have made it harder to keep up with Moore's Law [1].

In order to overcome the heat issue brought in by the on-chip power densities resulting from increasing the number of transistors and to avoid processor frequency limitations, future high-performance nano devices will surely need ultra-scaled transistors, a lower power supply voltage (V_{DD}), and a lower subthreshold swing (SS). However, the main obstacles to standard metal-oxide-semiconductor field-effect transistor (MOSFET) technology are short channel effects and the fundamental Boltzmann constraint of 60 mV/decade at ambient temperature.

Several types of field effect transistors have been proposed in previous studies based on non-classical physical mechanisms in order to break the SS thermal limit. Different research studies have demonstrated that the graphene nano-ribbons FET (GNRFET) and the CNTFET are presented as successful devices for CMOS circuits for sub 10 nm node technology. The GNRFETs can potentially be good transistors with high I_{ON}/I_{OFF} ratio and low subthreshold swing.

There are mainly two types of GNRFETs: Metal-Oxide Semiconductor-(MOS-) type GNRFETs (MOS-GNRFETs) and Schottky-Barrier-type GNRFETs (SB-GNRFETs). MOS-GNRFETs have GNR-based drains, channels, and the current conduction inside MOS-GNRFETs is mostly based on thermionic emission. SB-GNRFETs also have intrinsic GNR channels, but drains and sources are made of metal therefore, Schottky barriers occur at the graphene-metal junctions, and the current conduction is mainly based on Schottky barrier tunnelling.

Field-effect transistors (FETs) made of carbon nanotubes (CNTs) are one of the leading emerging technologies being researched to prolong the life of CMOS technology. This is explained by the superior material qualities of carbon nanotubes. Transistors with significantly lower leakage current and higher radio-frequency (RF) power gain are made possible by CNTs' reasonable bandgap.

Lazzaz *et al.* in 2022 [4] have studied a theoretical model based on the Bohm Quantum Potential (BQP) theory and compared it with experimental data. The

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theory fits with the experiment after an optimization. Shams Ul Haq *et al.* in 2024 [5] have demonstrated the energy-efficient High-Speed dynamic logic-based One-Trit multiplier in CNTFET technology. The results of this study demonstrate that the proposed circuit shows a 34.16 %, 66.44 %, and 82.80 % reduction in power, PDP, and EDP as compared to the lowest power, delay, and PDP of the designs under consideration.

Recip Emir *et al.* in 2024 [6] have presented a deep approach for modelling the power consumption and delay of logic circuits employing GNRFET technology. The results of this study demonstrate that the delay advantage of the logic circuits employing GNRFETs was calculated to be 53.2 % lower than those using Si-based MOSFET.

Sneha Arora *et al.* in 2024 [7] have presented a comprehensive analysis of ultra-low power GNRFET based 20T hybrid full adder for computing applications. The results of this simulation demonstrate that this proposed hybrid full adder reduces the power consumption by 99.9 %, delay by 99.0 %, and PDP by 99.8 % compared to other adders.

So, the literature of this paper confirms that both CNTFET and GNRFET devices are very important for CMOS circuits application which need to improve them using a different quantum approach.

In this paper, we study and compare the performance of GNRFET and CNTFET devices using the Non-Equilibrium Green Function formalism to have a speed CMOS inverter circuit. The impact of the lateral spacing has been studied to generate a minimum leakage current in both devices.

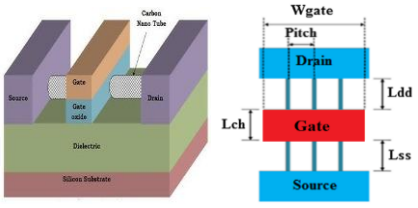
2. DEVICE STRUCTURE AND SIMULATION MODEL

Fig. 1 illustrates the CNTFET device used in this simulation. Single wall Carbon Nano Tube (CNT) is preferred in nano electronics applications because of their high current-carrying capacity and, depending on the angle at which the tubes are placed, their metallic and semiconducting qualities.

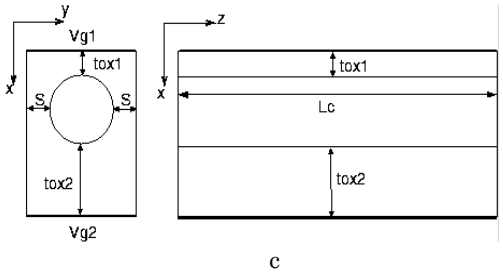
The channel device is characterized by the chirality vector specified by integer pair (n,m). It defines the angle of formation of the carbon atom along the nanotube. If the $n = m$ or $n - m = 3i$, then the CNT nanotube is metallic. The CNT diameter can be determined by the following expression:

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \qquad (1)$$

Where the a_0 is the interatomic distance between each carbon atom and its neighbor. We note from the Eq. 1 that if the chirality change, the CNT diameter change.



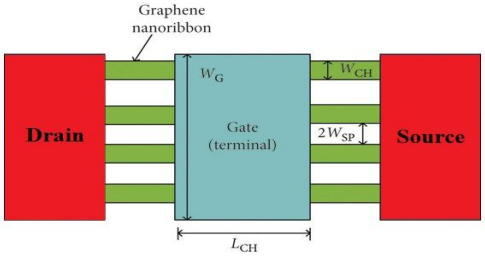
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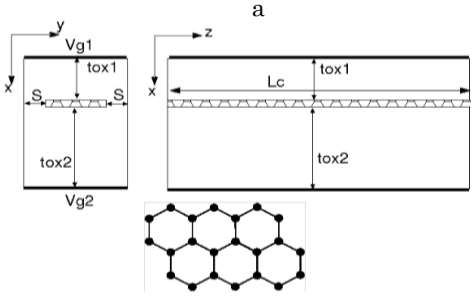
c

Fig. 1 – (a): CNTFET device, (b): Top view of the CNTFET device, (c): structure parameters of CNTFET

The silicon substrate used in GNRFETs has substantially doped graphene drain and source regions. Graphene nanoribbons are arranged in parallel to form the channel. The drive strength increases with the number of nanoribbons because they make better contact with the source and drain. Fig. 2 shows the GNRFET device.



a



b

Fig. 2 – (a): GNRFET device, (b): Structure parameters [14, 15]

W_{CH}: Channel width, L_{CH}: channel length, W_{SP}: space width of the adjacent GNRs

Table 1 displays the geometrics parameters used in this simulation for both devices for 5 nm channel length.

In this paper, the GNRFET and CNTFET are simulated and analysed using the Self-consistent numerical solution of Poisson-Schrodinger equations and Non-Equilibrium Green's Function (NEGF) method. The method is applied to simulate nanoscale devices in which the iterative self-consistent method is used to determine the electron density and equilibrium potential.

Table 1 – Geometric and operating parameters

Parameter	Values
Channe length	5 nm
Top gate oxide	1 nm
Bottom gate oxide	1 nm
Lateral spacing (s)	1 nm
Number of atoms along the ring of enrolled (n)	4

Supply voltage (V)	0.8
Gate length (L_G)	5 nm
Dielectric constant HfO_2	24

This paper uses the Non-Equilibrium Green's Function (NEGF) approach and the self-consistent numerical solution of Poisson-Schrodinger equations to simulate and analyse the GNRFET and CNTFET. This approach is used to model nanoscale devices where the electron density and equilibrium potential are found using the iterative self-consistent method [9, 10].

The usual time-independent Schrödinger equation:

$$E\{\psi\} = |H|\{\psi\} + |\Sigma|\{\psi\} + \{s\} \quad (2)$$

H: Hamiltonian matrix whose eigenvalues represent the allowed energy levels and describe the quasiparticle dynamics around the equilibrium state.

Σ represents self-energy and it defines the disturbance from the open boundary conditions, it is included as part of the system Hamiltonian, $|\Sigma|\{\psi\}$ and $\{s\}$ represents the outflow and inflow respectively.

Using this modified Schrodinger equation, the wave function can be represented by the following equation:

$$\{\psi\} = \left[EI - H - \Sigma\right]^{-1}\{s\} \quad (3)$$

I: is an identity matrix of the same size as the rest.

Σ^{in}: In-scattering function.

ħ: Plank constant.

G^n, G^A and G^R are the matrix defining as follows:

$$G^R = \left[EI - H - \Sigma\right]^{-1} \quad (4)$$

$$\left[G^R\right]^+ = G^A \quad (5)$$

The second equation of the NEGF is presented by the following expression:

$$G^n = G^R \Sigma^{in} G^A \quad (6)$$

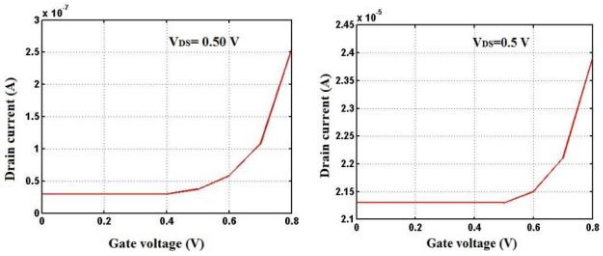
The current equation of CNTFET structure using NEGF formalism can be represented by the following equation:

$$I^{op} = \frac{(\Sigma G^n - G^n \Sigma^+)}{i\hbar} + \frac{(\Sigma^n G^A - G^R \Sigma^{in})}{i\hbar} \quad (7)$$

3. RESULTS AND DISCUSSION

Fig. 3a shows the transfer characteristics of the CNTFET 5 nm. The gate voltage swept from 0 to 0.8 V for V_{DS} = 0.5 V. The maximum current presents the ON current when $V_{GS} = V_{DD}$ and the value of on current is 2.5×10^{-7} A. The leakage current of this simulation is 39 nA and it presents the value of the current when V_{GS} = 0 V.

Fig. 3b shows the transfer characteristic of the GNRFET 5 nm for V_{DS} = 0.5 V. The value of the ON current is 2.36×10^{-5} A and the leakage current 21.4 μA. The ON current for GNRFET is higher than the CNTFET due to the strain effect and the leakage current is very lower for CNTFET than the GNRFET because the direct tunnelling current is more important in this device.



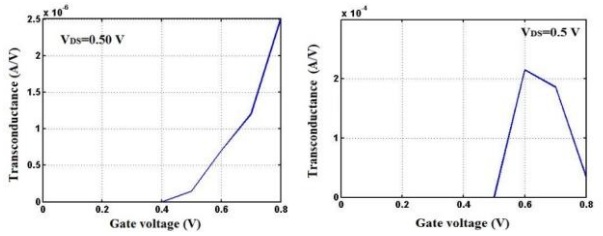
a b

Fig. 3 – Transfer characteristics for both devices

Transconductance represents the variation of drain I_D current as a function of gate source voltage (V_{GS}). The transconductance is defined by the following equation [11, 12]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (8)$$

Fig. 4a shows the transconductance of the CNTFET 5 nm for V_{DS} = 0.5 V. The gate voltage is swept from 0 to 0.8 V and the maximum transconductance in this simulation reads 2.5 μA/V.



a b

Fig. 4 – (a) Transconductance of the CNTFET, (b) Transconductance of the GNRFET

Fig. 4b presents the transconductance of the GNRFET 5 nm for V_{DS} = 0.5 V and the gate voltage swept from 0 to 0.8 V. The maximum value of the transconductance presented in this simulation is 2.1×10^{-4} A/V.

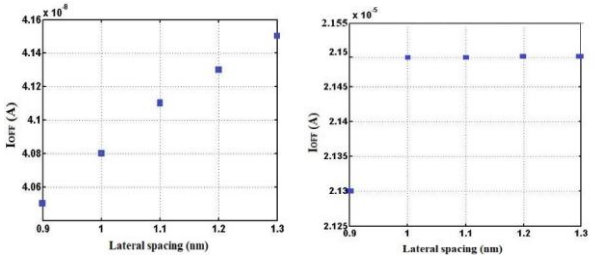
CNTFER and GNRFET are the modern devices for electronic amplifiers because it is closely related to the amplifier voltage gain, the transconductance, or short slope, is a crucial design parameter. We can explain the higher transconductance in the GNRFET than the CNTFET due surface roughness morphology used in this simulation.

The lateral spacing is presented as a key geometric parameter for both CNTFET and GNRFET devices. The scaling of channel length for sub 10 nm requires optimization of this parameter to minimize the leakage current and improve the performance ratio I_{ON}/I_{OFF} of the device.

Fig. 5 (a) and (b) show the impact of the lateral spacing on the leakage current for both devices. The lateral spacing is swept from 0.9 nm to 1.3 nm. The results of this simulation confirm that the increase of the lateral spacing parameters increases the leakage current for both devices.

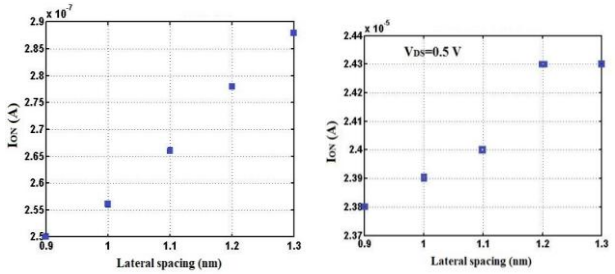
Complementary metal oxide semiconductors are thought to be exceptional for the semiconductor industry due to their fabrication in integrated circuits (ICs). The number of transistors on a device increases rapidly

as transistor size decreases exponentially. The ON current presents the metric parameter that can control the performance of the device for low power CMOS applications [16, 17].



a b

Fig. 5 – Impact of the lateral spacing on the leakage current of the CNTFET (a) and CNTFET (b)



a b

Fig. 6 – (a) Impact of the lateral spacing on the ON current of the CNTFET, (b) Impact of the lateral spacing on the ON current of the GNRFET

Fig. 6a shows the impact of the lateral spacing parameter on the ON current of the CNTFET device. The lateral spacing parameter is swept from 0.9 nm to 1.3 nm. We note that the ON current increases with the increase of the lateral spacing parameter and the maximum ON current calculated to be 2.88×10^{-7} A.

Fig. 6b shows the impact of the lateral spacing parameter on the ON current of the GNRFET device. The lateral spacing parameter is swept from 0.9 nm to 1.3 nm. We note that the ON current increases with the increase of lateral spacing parameter and the maximum ON current is calculated to be 2.43×10^{-5} A.

4. CONCLUSION

In this paper, we have presented a comparative study of the performance of CNTFET and GNRFET devices for 5 nm channel length. The results of this simulation confirm that CNTFET have a higher performance ratio I_{ON}/I_{OFF} than the GNRFET. The results of this simulation confirm also that the increase of the lateral spacing distance parameter increases the ON current with 15.2 % and 4.20 % for CNTFET and GNRFET. The leakage current increases with 2.45% and 1.17 % for both devices.

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Порівняльний аналіз характеристик CNTFET із подвійним затвором та GNRFET із контактом Шотткі

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Польові транзистори на основі графенових нанострічок (GNRFET) та вуглецевих нанотрубок (CNTFET) – це перспективні технології, які останніми роками привертають значну увагу. Вони активно досліджуються як можливі альтернативи пристроям із кремнієвим каналом для інтегральних схем і систем наступного покоління. Обидва типи пристроїв мають привабливі фізичні характеристики для застосування в електроніці й можуть допомогти подолати різноманітні фізичні обмеження та недоліки, зокрема високий струм витоку (I_{OFF}), ефекти короткого каналу (SCE), а також проблеми, пов'язані зі зростанням порогової напруги (V_{TH}) та насиченням швидкості носіїв заряду.

Необхідно враховувати вплив параметра латерального рознесення на надійність пристрою, оскільки він безпосередньо визначає величину паразитних ємностей. У цій роботі ми порівнюємо два різновиди пристроїв і досліджуємо їхні переваги з погляду струму витоку (I_{OFF}) та струму увімкненого стану (I_{ON}), використовуючи контакт Шотткі. Для опису квантового транспорту в обох пристроях застосовано чисельне моделювання на основі формалізму нерівноважних функцій Гріна (NEGF). У межах тривимірного квантового моделювання, виконаного за допомогою програмного інструменту Nano TCAD Vides, проаналізовано передавальні характеристики, крутизну, профілі потенціалу та коефіцієнти пропускання, що дозволило визначити показники ефективності пристроїв. Наукова новизна роботи полягає в досягненні кращих робочих характеристик пристроїв завдяки оптимізації параметра латерального рознесення. Результати моделювання підтверджують, що збільшення параметра латерального рознесення призводить до зростання струму I_{ON} на 15,2 % для CNTFET і на 4,20 % для GNRFET. Дослідження показує, що за умови застосування наведених тут оптимальних параметрів пристрої типу CNTFET є більш перспективними для створення швидкодіючих CMOS-схем зі зниженим енергоспоживанням.

Ключові слова: CNTFET, GNRFET, Бічний інтервал, Струм витоку.