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REGULAR ARTICLE

Investigation of Electrical Characteristics of a SiGe Multi-Channel Junctionless Nanowire FET at the Sub-5 nm Technology Node

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As semiconductor technology advances toward the sub-5 nm regime, maintaining high device performance while suppressing short-channel effects, leakage current, threshold-voltage instability, and power dissipation has become increasingly challenging. Thus, the design and analysis of new silicon-germanium (SiGe) based Multi-Channel Junctionless Nanowire Field Effect Transistor (MC-JL-NWFET) are discussed in this paper to enhance performance of such devices. The proposed device includes two stacked channels made from nanowires controlled by several gates, which makes it possible to improve electrostatic control and enlarge conduction area. Realistic results concerning the properties of the proposed device were obtained considering the effects such as Fermi-Dirac statistics, bandgap narrowing, electron mobility decrease, self-heating and quantum confinement. It was found out that the device demonstrates excellent behavior characterized by high level of transfer and output characteristics, reliable operation because of good electrostatic properties, high level of drive current and prevention of short-channel effect. Device scaling allows stating that 5 nm MC-JL-NWFET has 181.8 % improvement in transconductance, 78.6 % increase in ON-state current comparing with 120 nm one. Also, it is necessary to note that the changes in threshold voltage due to reduction in gate length are relatively small (only 18.8 %). All these results are achieved owing to high electron mobility of SiGe materials and better electrostatic control.

Keywords: SiGe, Transconductance, Short-Channel Effects, Nanoelectronics.

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1. INTRODUCTION

The progressive decrease in size of metal–oxide–semiconductor field-effect transistors (MOSFETs) was one of the critical drivers in the improvement of integrated circuits during many years. Scaling provided improvements in speed, increase in integration density, and enhancement of efficiency in terms of power consumption [1, 2]. However, nowadays, as transistors shrink to the dimensions smaller than 5 nm, classical planar structures begin to face various limitations. They are manifested as severe short-channel effects, large leakage currents, threshold voltage instability, and higher dissipated power [3, 4].

Therefore, there is a need to develop new transistor architectures to further improve performance at small dimensions due to stronger electrostatic control. Multi-gate devices such as FinFETs, gate-all-around (GAA) nanowire transistors, nanosheets, and complementary FETs (CFETs) became the most promising options for future technology nodes [5, 6]. In particular, among all possible options, nanowire transistors have a number of advantages related to the surrounding of the gate of nanowires that significantly suppress short-channel effects and decrease leakage currents [5, 6]. In addition, another promising direction in device development is the use of junctionless transistors where the need to fabricate sharply defined source and drain regions is excluded. Instead, these devices consist of a uniformly doped channel, which leads to simplified fabrication and decreased variability [7, 9]. Also, the use of a junctionless design makes it possible to improve some carrier transport properties and thus enhance overall performance. Therefore, junctionless nanowire transistors become attractive as a future option for highly scaled semiconductor technologies. Besides changes in structure, modification of the materials used in transistors became another way of improving their performance. It should be mentioned that SiGe became widely acknowledged as the right channel material due to high carrier mobility and flexibility in controlling parameters compared to silicon [10, 13]. Thus, the use of SiGe instead of silicon improves the performance and efficiency without changing CMOS process flows. Besides, different thermal properties of SiGe compared to silicon make electrothermal analysis crucial for this type of transistor. Having considered all aforementioned issues, in this work, we propose a SiGe Multi-Channel Junctionless Nanowire Field-Effect Transistor (MC-JL-NWFET). Its main features include vertical stacking of two SiGe nanowire channels with electrostatic control performed by a tri-gate structure. This solution allows for increasing the channel area available for charge carriers with enhanced electrostatic integrity. As a result, the combination of a multi-channel design with

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junctionless principle and SiGe channel ensures the opportunity for increasing transconductance, drive current, and switching properties along with better scalability and stability against short-channel effects. In order to perform simulation and electrothermal analysis of this transistor, the Synopsys Sentaurus TCAD software will be used. Electrical and electrothermal behavior of this transistor will be assessed via detailed analysis of transfer and output characteristics, threshold voltage, transconductance, and scaling.

2. DEVICE STRUCTURE

Figure 1 shows the architectural schematic of the proposed SiGe MC-JL-NWFET targeting sub-5 nm technology node. The MC-JL-NWFET has two vertically stacked SiGe nanowire channels named as Channel 1 and Channel 2 and separated by the gate dielectric layer. The control of carriers is done using the gate electrodes around the channel region. The stack channel structure enhances the conductance path area as well as the strength of gate control.

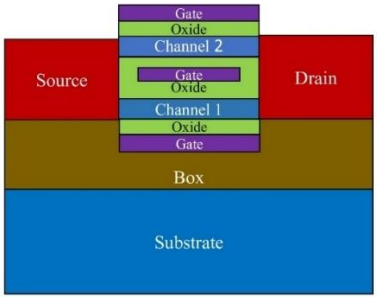

Fig. 1 – Structure of proposed device

Both source and drain regions are placed on opposite sides of the channel stack and have the same type of doping as that of the channel material. Thus, there is no formation of *p-n* junctions in the device, making the device to work based on the junctionless principle. The SOI platform has a buried oxide (BOX) layer over the silicon substrate to provide effective isolation from the underlying substrate and thus prevent the leakage through the substrate [11]. The values of design parameters used in the simulation investigation is taken from [1]. The replacement of silicon channel with SiGe channel improves the mobility of the carriers and is beneficial for nanoscale devices [10, 12].

Experimental values of thermal conductivity are used for all device regions including SiGe nanowire channel, source/drain extension, gate electrode, gate dielectric, substrate, and metal contact. The contribution of BEOL interconnect stack, Si-SiO_2 interface, and substrate contact thermal resistances is included in the simulation model. The ambient thermal boundary condition is considered as 300 K in the present analysis. The performance investigation of the proposed MC-JL-NWFET is carried out using Synopsys Sentaurus TCAD. Advanced physical models are considered to accurately simulate the transport of carriers in the high doping nanoscale devices. These models include the Fermi-Dirac statistics, old slotboom bandgap narrowing, doping dependence of mobility, transverse-field mobility degradation, and high-field velocity saturation effect. The carrier generation and recombination are simulated using both Shockley-Read-Hall (SRH) and Auger process [14, 15]. The quantum effects due to the ultrascaling of SiGe nanowire channel are accounted for using the density gradient quantum correction. To analyze the self-heating phenomenon and thermal transport in the device, the thermodynamic transport model is used. Through the use of thermodynamic transport, a self-consistent solution of Poisson's equation, carrier continuity equation, and lattice heat flow equation becomes possible. As a consequence, this simulation methodology is capable of providing thorough performance investigation of the proposed SiGe based multi-channel junctionless nanowire FET.

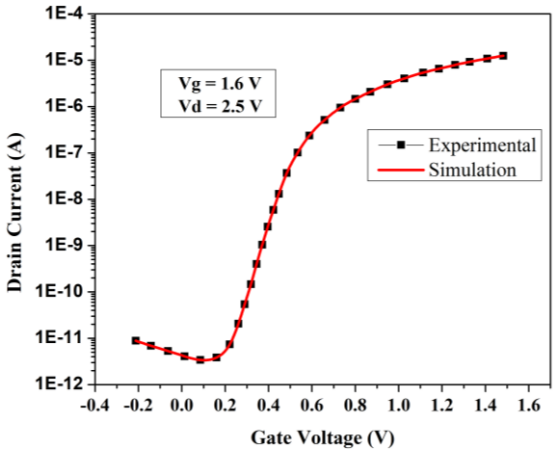

Fig. 2 – Validation of conventional structure [1]

Figure 2 shows the comparison of the simulated transfer characteristic of the reference nanowire transistor with respect to the experimental measurement at a drain voltage of 2.5 V. As seen from the figure, there is excellent correlation between the two data sets within the entire range of gate voltage variation.

3. RESULTS AND DISCUSSION

The output characteristic curves for the JL-NWFET using SiGe material, proposed in this work, are shown in Figure 3. For low drain voltages, it can be noticed that there is almost a linear increment of drain current as a function of V_D, which shows excellent carrier conduction with minimum channel resistance. As the value of the drain voltage increases, there appears the transition of the device from linear mode to saturation mode due to the development of pinch-off region near the drain end. A clear indication is seen for the saturation current with an increasing value for increasing gate voltage, showing effective tuning of channel charge density through the GAA configuration. The increasing values of currents under increasing gate biasing condition have been achieved due to good carrier transport properties such as higher electron mobility and smaller effective mass of the carrier in SiGe material when compared to the silicon material. The transfer characteristics of the proposed device at the various drain voltages of 0.5 V, 1.5 V, and 2.5 V are presented in Figure 4. In this figure, the value of the drain current is extremely small in the subthreshold region and increases considerably when the

threshold voltage is attained; therefore, this characteristic is a clear indication of successful gate modulation and channel conduction. With an increase in drain voltage, the drain current in the ON state increases significantly due to improved carrier injection and reduced source-channel potential barrier.

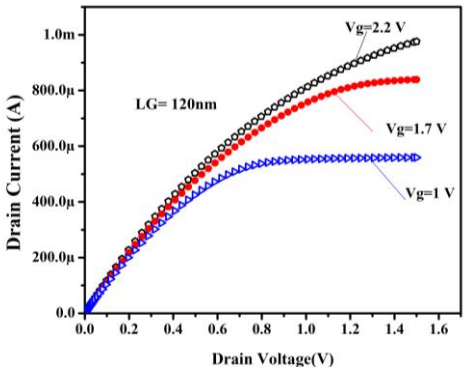

Fig. 3 – Output characteristics of MC-JL-NWFET for L_g = 120 nm

The negligible difference in the transfer characteristics at various drain voltages demonstrates a good resistance to the short-channel effect and reduced drain-induced barrier lowering (DIBL). Moreover, the abrupt change in the transfer characteristics of the proposed SiGe MC-JL-NWFET in moving from the OFF state to the ON state indicates successful switching operation. However, the higher value of ON-state current is a result of improved features of the proposed device such as the junctionless structure, better electrostatic control of the gate-all-around architecture and good carrier transport in the SiGe channel.

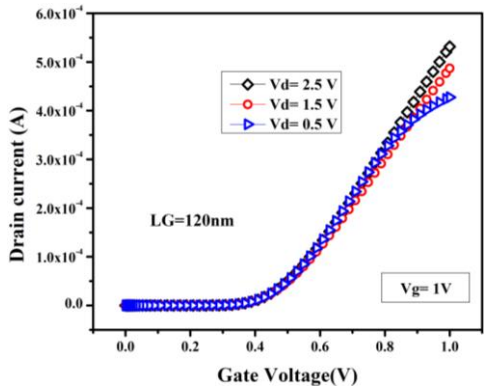

Fig. 4 – Transfer characteristics of MC-JL-NWFET for L_g = 120 nm

The output characteristics of the proposed device at gate voltages of 1.0 V, 1.3 V, and 1.6 V are shown in Figure 5. At relatively low drain voltages, the drain current increases almost linearly since the lateral electric field strength across the channel rises with the rising drain voltage. When the drain voltage exceeds the certain threshold value, the drain current approaches saturation levels. This means that the pinch-off effect arises in the vicinity of the drain. With higher gate voltages, the drain current grows since the concentration of carriers in the SiGe channel becomes higher. It should be noted that the device demonstrates the early saturation effect when the drain current remains unchanged within the saturation range. No noticeable degradation of the current occurs with further increase in the drain voltage, which confirms that the effective carriers transport takes place within the channel.

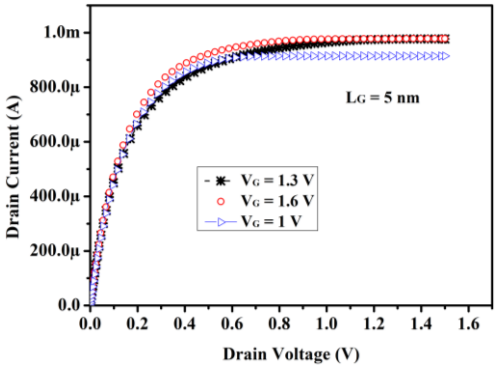

Fig. 5 – Output Characteristics of of MC-JL-NWFET for L_g = 5 nm

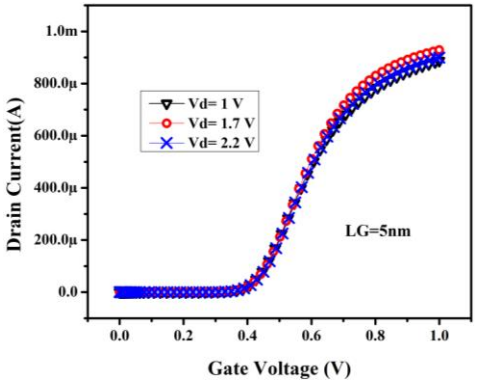

Fig. 6 – Transfer characteristics of of MC-JL-NWFET for L_g = 5 nm

Figure 6 shows the transfer characteristics of the proposed 5 nm SiGe junctionless nanowire FET at drain voltages of 1.0 V, 1.7 V, and 2.2 V. An increase in the gate voltage causes the FET to operate in the OFF state and then turn into the ON state close to the threshold voltage. Thereafter, there is a marked increase in the drain current. This indicates that the modulation efficiency of the channel carriers by the gate voltage is quite high. The abrupt switch from the subthreshold regime to the on-state can be explained by the gate-all-around structure that ensures the efficient electrostatic modulation of the nanowire channel. Furthermore, the transfer curves at different drain voltages are close to each other, which means that the short-channel effects are well-controlled even with the scaled gate length of 5 nm. A moderate drain current increase with increasing drain voltage is observed, which can be related to improved carrier injection and the small effect of DIBL. The maximum drain current in the on-state equals 0.9 mA, which proves the superiority of the SiGe channel over other materials in terms of enhancing the carrier mobility and decreasing the channel resistance.

The graph presented in Figure 7 demonstrates the transconductance characteristics of the designed SiGe JLNWFET when operating at different gate length parameters, i.e., 120 nm and 5 nm, as well as under

diverse gate-bias values. When increasing the drain voltage, the transconductance grows as a result of an increase in the lateral electric field that favors carriers movement within the material and thus enables more effective modulation of channel charge by gate bias. For the 120 nm structure, the gm grows constantly until reaching a maximum value around 1.1 mS, after which there is an almost constant pattern with the very slight decrease towards the higher drain voltages. On the contrary, the smaller transistor shows significantly higher g_m with its maximum value reaching nearly 3.1 mS at V_G = 1.6 V. Such results are explained by an increased electrostatic control from the gate, shorter transport path for carriers, and superior mobility features inherent to SiGe channels. Then the transconductance starts falling down, primarily due to such factors as velocity saturation, decrease in mobility as a consequence of strong electric field, as well as short channel effect. Nevertheless, despite decreasing, the maximum transconductance for the smaller transistor turns out to be almost three times higher than for the larger one. Figure 6 represents the dependency of threshold voltage (VTH) on gate length for the proposed SiGe junctionless nanowire FET. An increase in gate length from 10 nm to 80 nm causes an increase in the threshold voltage, ranging from about 0.25 V to 0.31 V. The increasing threshold voltage with increased gate length may be attributed to better electrostatic control in devices with long channels, where there is a stronger influence of the gate on the channel potential while minimizing short-channel effects like DIBL.

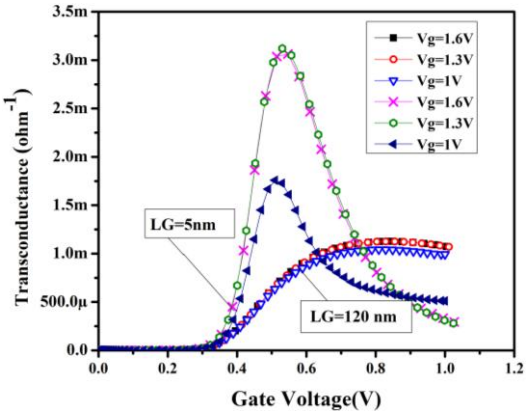

Fig. –7 Transconductance characteristics of SiGe JLNWFET at different Gate Length

For short gate lengths, however, the electrostatic control is less effective; hence, the influence of the drain electric field on the channel is higher. Consequently, the source-channel potential barrier becomes smaller and hence reduces the threshold voltage. While there has been gate length scaling, the variation in the threshold voltage is insignificant, indicating high electrostatic performance of the gate-all-around SiGe junctionless nanowire.

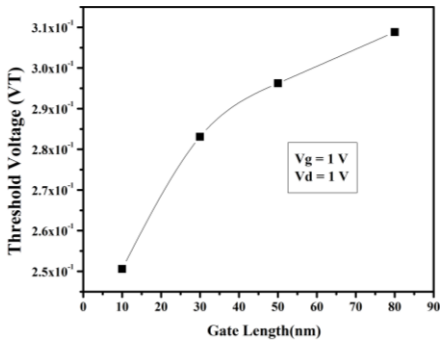

Fig. 8 – Threshold Voltage(VTH) of proposed SiGe JLNWFET

4. CONCLUSION

A proposed design of MC-JL-NWFET for sub-5 nm technology nodes has been presented in this work along with the evaluation of electrical characteristics. The proposed multi-channel structure of SiGe nanowire channels combined with the multi-gate configuration allows for better electrostatic control, more effective conduction, and faster carriers. It was found that there is an outstanding level of performance due to high transconductance and ON-current, effective gate control, and reduced short channel effect in the proposed structure. The scaling analysis also reveals that the 5nm device can offer the transconductance improvement of approximately 181.8 % and increased ON-state current of about 78.6 % with respect to the 120 nm transistor. Furthermore, there is relatively small variation in the threshold voltage for the whole range of gate lengths under analysis, which makes the proposed transistor suitable for further scaling to the smaller dimensions.

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Дослідження електричних характеристик багатоканального безперехідного польового транзистора SiGe з нанодротом у вузлі технології Sub-5 нм

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Оскільки напівпровідникова технологія розвивається в напрямку режиму розмірів менше 5 нм, підтримка високої продуктивності пристрою, одночасно придушуючи ефекти короткого каналу, струм витоку, нестабільність порогової напруги та розсіювання потужності, стає все більш складною. Таким чином, у цій статті обговорюються розробка та аналіз нового багатоканального безперехідного нанодротового польового транзистора (MC-JL-NWFET) на основі кремнію-германію (SiGe) для підвищення продуктивності таких пристроїв. Запропонований пристрій включає два складені канали, виготовлені з нанодротів, керовані кількома затворами, що дозволяє покращити електростатичний контроль та збільшити площу провідності. Були отримані реалістичні результати щодо властивостей запропонованого пристрою з урахуванням таких ефектів, як статистика Фермі-Дірака, звуження забороненої зони, зменшення рухливості електронів, самонагрівання та квантове обмеження. Було виявлено, що пристрій демонструє чудову поведінку, що характеризується високим рівнем передавальних та вихідних характеристик, надійною роботою завдяки хорошим електростатичним властивостям, високим рівнем струму керування та запобіганням ефекту короткого каналу. Масштабування пристрою дозволяє стверджувати, що 5-нм MC-JL-NWFET має покращення крутизни на 181,8 % та збільшення струму увімкненого стану на 78,6 % порівняно зі 120-нм. Також необхідно зазначити, що зміни порогової напруги внаслідок зменшення довжини затвора є відносно невеликими (лише 18,8 %). Всі ці результати досягнуті завдяки високій рухливості електронів SiGe матеріалів та кращому електростатичному контролю.

Ключові слова: SiGe, Транспровідність, Короткоканальні ефекти, Наноелектроніка.