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REGULAR ARTICLE

Development of a High-Performance Lead-Free Cs_2SnX_6 (X = Br)-Based Perovskite Solar Cell with Various Transport Layers Optimization

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This research article showed a performance analysis of an FTO/ETL/Cs_2SnBr_6/HTL/Au-based PSC device using the SCAPS-1D simulator. To make an optimized PV device, three ETL mate-rials (CdS, SnO_2, and ZnSe) and HTL materials (CBTS, P_3HT, and CuO) have been used in the simulator. CdS-based ETL showed better performance at 80 nm thickness, where PCE achieved 25.14 %, and CBTS HTL material recorded an optimum PCE of 29.04 % at 60 nm thickness among all other used ETL and HTL materials. In a further look at optimized ETL and HTL, the Cs_2SnBr_6-based PSC has shown optimal photovoltaic performance at 500 nm thickness, where VOC, JSC, PCE, and FF values were recorded as 1.19 V, 32.12 mA/cm^2, 27.66 %, and 62.4 %, respectively. Above 500 nm thickness of the Cs_2SnBr_6-based PSC, the device PV performance remained almost constant. On the other hand, it has been observed that between 10 °C-20 °C temperature, the PCE of the device increased significantly, and after 20 °C temperature, the PCE of the device does not change continuously. The optimized device temperature is 20 °C. All the simulation studies have been performed under the ambient temperature of 27 °C, and all the other recombination parameters have remained at ideal conditions.

Keywords: Perovskite, ETL, HTL, PV, Thickness, PCE.

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1. INTRODUCTION

Rapid industrial growth is the key contributor to the emission of anthropogenic gases, which is a serious issue across the world [1-3]. Thus, the demand of renewable energy is increasing significantly. Solar energy is one of the major contenders among the renewable energy sources that will be a prime contributor in the fulfillment of energy demand. Perovskite solar cells (PSC) are the new generation of photovoltaic (PV) materials that have the following key properties: suitable band energy, superior carrier mobility, diffusion length, and absorption coefficient. Despite having the above-mentioned advantages, it has few disadvantages, including toxicity due to the Pb-element and device stability. Thus, lead-free PSC materials are creating huge interest among the researchers to find the environment-friendly solar materials [4-6]. Lead-free Ti-based material was explored by Ju et al., where they identified that Cs_2TiX_6-based PSCs exhibit a tunable band gap of 1-1.8 eV [7]. Chen et al., with Cs_2TiBr_6-PSC, achieved 0.89 V VOC (open circuit voltage), 3.87 % JSC (short circuit current density), 2.05 % PCE (power conversion efficiency), and 59.5 % FF (fill factor), where TiO_2 and P3HT are used as ETL (electron transport layer) and HTL (hole transport layer), respectively [8]. Other PSC materials, $Cs_2AgBiBr_6$, $La_{0.7}Sr_{0.3}MnO_3$ /Nb:$SrTiO_3$-based PV model, showed 7.25 % and 32 % PCE, respectively [9-10].

In our study, an FTO/ETL/Cs_2SnBr_6/HTL/Au-based PV device has been developed with various ETL and HTL materials taken into consideration to find the suitable

HTL and ETL material for the device performance optimization. All the physical and optical parameters used in the simulation study are collected from various reported articles.

Our study has the following significant outcomes:

i) optimization of ETL material (CdS, SnO2, and ZnSe) performance used in the device.

ii) optimization of HTL material (CBTS, P3HT, and CuO) performance used in the device.

iii) optimization of the thickness of the Cs2SnBr6-based PSC and analysis of its PV performance.

iv) Device temperature optimization to check the device stability.

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2. DEVICE STRUCTURE AND SIMULATION

In our study, we have proposed an n-i-p structure device model, an FTO/ETL/Cs_2SnBr_6/HTL/Au-based PV module. Where we have taken three ETL materials: CdS, SnO_2, and ZnSe; and three HTL materials: CBTS, P3HT, and CuO for the simulation and FTO and Au used as electrodes. Here, Table 1 and Table 2 show the different parameters used for the FTO/ETL/Cs_2SnBr_6/HTL/Au-based PV module [11-15].

Here, λ, E_g, E_a, ζ_r, μ_n, μ_h, N_D, and N_A are denoted as thickness, band gap, electron affinity, permittivity, electron mobility, hole mobility, donor doping concentration, mobility, and acceptor doping concentration, respectively. Our study was performed at AM 1.5 G, 1000 W/m^2 power with Gaussian energy distribution, where characteristic energy is kept at 0.1 eV [16-17]. Here, Fig. 1 indicates the schematic diagram of the proposed PSC, and Fig. 2 shows the energy band diagram of the proposed PV model.

Table 1 – Absorbing and ETL materials parameters

Parameters	Cs_2SnBr_6	CdS	SnO_2	ZnSe
λ (nm)	varied	varied	varied	varied
E_g (eV)	1.36	2.4	3.6	1.8
E_a(eV)	4.09	4.2	4	4.55
ζ_r	4	10	9	5.54
μ_n (cm^2/vs)	250	100	100	100
μ_h (cm^2/vs)	100	25	25	50
N_D (cm^{-3})	0	10^{19}	10^{16}	10^{18}
N_A (cm^{-3})	10^{18}	0	0	0

Table 2 – Electrode and HTL materials parameters

Parameters	FTO	CBTS	CuO	P3HT
λ (nm)	varied	varied	varied	varied
E_g (eV)	3.6	1.9	1.51	1.7
E_a(eV)	4.5	3.6	4.07	3.5
ζ_r	10	5.4	18.1	3
μ_n (cm^2/vs)	100	30	100	0.0018
μ_h (cm^2/vs)	20	10	10	0.0186
N_D (cm^{-3})	0	0	0	0
N_A (cm^{-3})	1.8×10^{19}	10^{18}	10^{18}	10^{18}

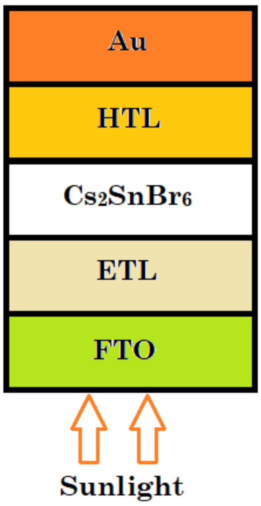

Fig. 1 – Schematic diagram of the proposed PV model

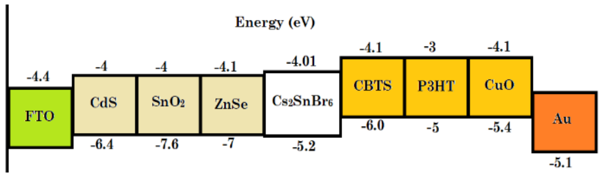

Fig. 2 – Energy band diagram of the proposed PV model

3. RESULTS AND DISCUSSION

3.1 ETL Optimization

In this sub-section, to select an appropriate ETL material among all three materials, CdS, SnO_2, and ZnSe, we have used an HTL-free FTO/ETL/Cs_2SnBr_6 structure in the SCAPS model where the thickness of the absorbing layer was kept fixed and the thickness of the ETL varied from 20 nm to 100 nm. Here, Fig. 3 shows the thickness-PCE plot of the PV device. From this figure, it is clearly observed that CdS as ETL material has outperformed the other two ETL materials SnO_2 and ZnSe, where PCE achieved 25.14 % at 80 nm thickness. SnO_2 and ZnSe achieved the best performance, 23.10 % and 17.62 % of PCE, at 100 nm and 20 nm thickness, respectively.

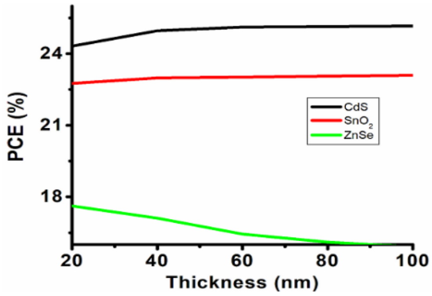

Fig. 3 – ETL materials thickness optimization

3.2 HTL Optimization

Here, we have optimized the PV performance of the three HTL materials, CBTS, P3HT, and CuO. In the previous section, it was observed that CdS will be an appropriate ETL material that has an optimized thickness of 80 nm. Now, our device model structure is FTO/CdS/Cs_2SnBr_6/HTL-based, and the thickness of the HTL material varies from 20 nm to 100 nm. Here, Fig. 4 shows the thickness-PCE plot of the PV device. The above figure shows that CBTS HTL material has the highest PCE of 29.04 % at 60 nm thickness, whereas the other two HTL materials, P_3HT and CuO, have optimum PCEs of 26.14 % and 24.82 % at 60 nm and 100 nm thickness.

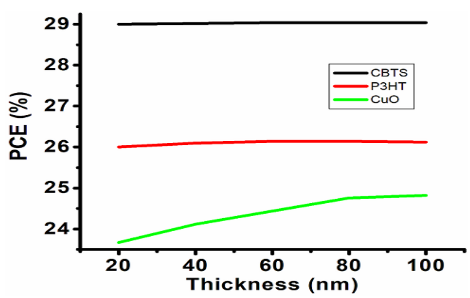

Fig. 4 – HTL materials thickness optimization

3.3 Cs_2SnBr_6 Thickness Optimization

In the previous section, we have discussed the best PV performers as ETL and HTL materials for the FTO/CdS/Cs_2SnBr_6/CBTS/Au-based device, which are CdS and CBTS. Now, the thickness of the Cs_2SnBr_6-based PSC was varied from 100 nm to 700 nm. Here, Fig. 5 indicates the PCE-thickness graph of the device. After that 500 nm thickness, the device shows insignificant changes in the PCE. So, the optimized thickness of the Cs_2SnBr_6-based PSC is 500 nm.

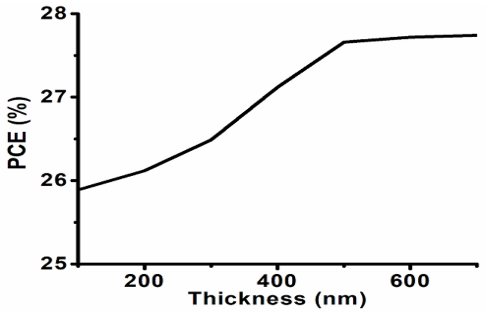

Fig. 5 – Variation of active layer thickness with PCE

3.4 Device Temperature Optimization

Device stability was checked in the air where the temperature of the atmosphere was changed from 10 °C to 60 °C. Here, Fig. 6 showed the PCE-temperature plot. From this figure, it is clearly observed that up to 20 °C, the PCE of the device increases, and after that temperature, PCE remains almost constant. So, the optimized device temperature is 20 °C.

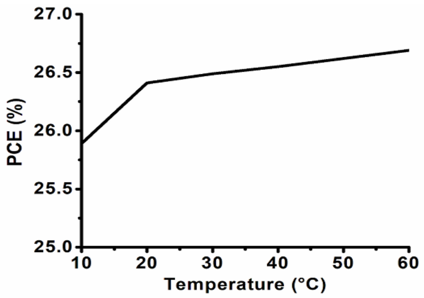

Fig. 6 – Variation of device temperature with PCE

3.5 Optimized Device Model

The optimized device model *J-V* plot is shown in Fig. 7.

Table 3 – PV performance of the device

Material	V_{OC} (V)	J_{SC} (mA/cm^2)	PCE (%)	FF (%)
Cs_2SnBr_6	1.19	32.12	27.66	62.4

The performance of the device at the optimized value of the thickness of the Cs_2SnBr_6, CdS, and CBTS layers is mentioned in Table 3.

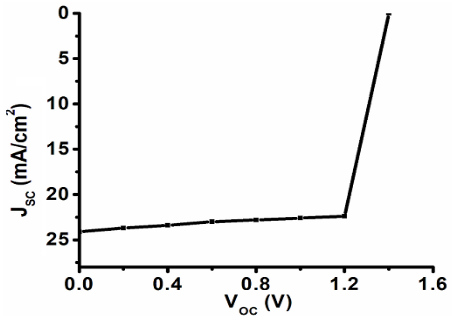

Fig. 7 – *J-V* plot of the optimized device

3.6 Quantum Efficiency Studies

Quantum efficiency (QE) is an important tool to understand the rate of conversion of incident photon into electricity. Here, Fig. 8 shows QE plot of the optimized device. From QE plot it is clear that at 350 nm wavelength the device has optimum QE.

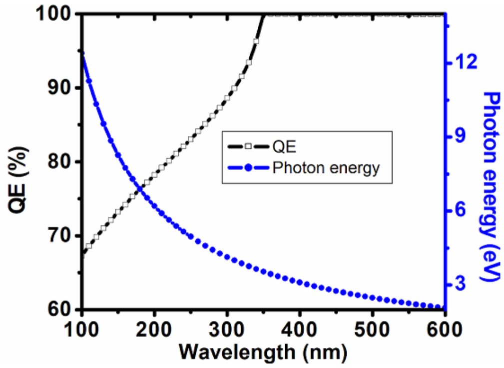

Fig. 8 – QE plot of the optimized device

4. CONCLUSION

Our study showed an optimized Cs_2SnBr_6-based PV device where an optimum PCE of 27.66 % can be achieved at 500 nm thickness. Such a device is optimized at 20 °C temperature. This high-performance device requires an optimized ETL and HTL material. In our study, CdS as ETL and CBTS as HTL outperformed all other materials in terms of better PV performance. This PV analysis will be very useful to explore the optical properties of that Cs_2SnBr_6-based PSC. To improve the PCE further of Cs_2SnBr_6, band gap optimization is required.

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Розробка високопродуктивного безсвинцевого перовскітного сонячного елемента на основі Cs2SnX6 (X = Br) з оптимізацією різних транспортних шарів

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У роботі показано аналіз продуктивності пристрою PSC на основі FTO/ETL/Cs_2SnBr_6/HTL/Au за допомогою симулятора SCAPS-1D. Для створення оптимізованого фотоелектричного пристрою в симуляторі було використано три матеріали ETL (CdS, SnO_2 та ZnSe) та HTL-матеріали (CBTS, P_3HT та CuO). ETL на основі CdS показав кращу продуктивність при товщині 80 нм, де PCE досяг 25,14 %, а HTL-матеріал CBTS зафіксував оптимальний PCE 29,04 % при товщині 60 нм серед усіх інших використаних ETL та HTL-матеріалів. При подальшому розгляді оптимізованих ETL та HTL, PSC на основі Cs_2SnBr_6 продемонстрував оптимальну фотоелектричну продуктивність при товщині 500 нм, де значення V_{OC}, J_{SC}, PCE та FF були зареєстровані як 1,19 В, 32,12 мА/см2, 27,66 % та 62,4 % відповідно. При товщині понад 500 нм PSC на основі Cs_2SnBr_6 фотоелектрична продуктивність пристрою залишалася майже постійною. З іншого боку, було помічено, що в діапазоні температур від 10 °C до 20 °C PCE пристрою значно збільшувався, а після температури 20 °C PCE пристрою не змінюється безперервно. Оптимізована температура пристрою становить 20 °C. Всі моделювальні дослідження проводилися за температури навколишнього середовища 27 °C, а всі інші параметри рекомбінації залишалися в ідеальних умовах.

Ключові слова: Перовскіт, ETL, HTL, PV, Товщина, PCE.