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REGULAR ARTICLE

Carrier Mobility Analysis of Raised Source Drain Double Gate JLFET for Power Devices

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The continuous downscaling of semiconductor devices has significantly influenced the evolution of advanced transistor architectures that are capable of ensuring high performance while minimizing short channel effects (SCEs). Among these novel structures the Raised Source Drain Double Gate Junctionless Field Effect Transistor (RSD DG JLFET), a junctionless device with elevated source and drain regions has attracted considerable attention due to its unique design and operational advantages. This device offers superior electrostatic control over the channel, reduced parasitic series resistance and enhanced carrier transport properties when compared with conventional MOSFETs and other junctionless devices. In this work a comprehensive carrier mobility analysis of RSD DG JLFET structures is carried out to investigate its suitability. The study systematically considers the influence of key physical parameters including the choice of dielectric material, dielectric thickness, gate work function and operating temperature. Using TCAD simulations the dependence of both electron and hole mobilities was evaluated along the longitudinal as well as transverse axes of the device. The results clearly demonstrate that the raised source drain configuration significantly mitigates parasitic resistances which are a major limitation in aggressively scaled devices. Furthermore, the structural modification also improves electrostatic integrity thereby boosting the overall device stability under varying bias conditions. Enhanced carrier mobility was observed which directly contributes to better current drive capability and reduced conduction losses. The findings suggest that RSD DG JLFET possess a promising balance between device scaling and performance reliability.

Keywords: JLFET, Raised Source Drain, Carrier Mobility, Nanoelectronics, Power Devices.

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1. INTRODUCTION

The demand for faster, smaller, and more energy-efficient devices in power electronics and VLSI systems has driven significant advancements in semiconductor device technology. Conventional MOSFETs, although extensively used in switching applications, face critical performance and reliability issues when scaled below the 50 nm node. Short-channel effects, elevated leakage currents and parasitic resistances increasingly hinder their effectiveness in modern integrated circuits. To address these challenges, various innovations have been explored. One such development is the Raised Source/Drain (RSD) structure introduced to lower parasitic resistance and improve short-channel control. Early pioneering work on self-aligned and dual-spacer RSD MOSFETs was reported by [1-2], followed by studies evaluating the influence of epitaxial layers on short-channel effects in 50 nm MOSFETs, as demonstrated [3]. Beyond structural refinements, a paradigm shift occurred with the introduction of JLFETs which eliminate PN junctions by employing uniformly doped or intrinsic channels. This approach simplifies fabrication while enabling improved scalability. J. P. Colinge et al. first presented the concept of SOI-based junctionless devices as "CMOS without junctions" [4], which was subsequently extended to multi-gate architectures [5] and [6] further presents the inherent versatility of the junctionless concept that has spurred numerous performance-enhancement strategies. The [7] outlined junctionless transistor, highlighting their advantages in low-power and nanoscale applications and [8] reviewed trends in topology, modeling and applications. Analytical models recessed double-gate JLFET proposed by [9] further demonstrate improvements in subthreshold behavior. The importance of accurate mobility extraction for reliable modeling emphasized by [10] while [11] discussed technology boosters, including high-k dielectrics and gate engineering, to suppress short-channel effects. Recent studies have emphasized electrostatic optimization and gate engineering for fine-tuning device performance. The [12] introduced a circular double-gate SOI MOSFET with raised source/drain which improved drive current and suppressed leakage. This convergence of RSD and junctionless concepts has led to the development of raised source/drain JLFETs hybrid devices that leverage the strengths of both architectures. Key innovations include dopingless accumulation-mode designs [13], gated RSD configurations [14].

Simulation studies have validated these theoretical findings with [15-16] reporting that raised source-drain DG JLFETs can effectively mitigate short-channel effects and enhance device reliability. Collectively, the reviewed literature highlights significant progress in the modeling, design and application of junctionless transis-

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tors underscoring the shift from conventional junction-based devices to junctionless architectures. Since carrier mobility is a key factor governing device performance, this paper presents a detailed analysis of carrier mobility in raised source-drain DG JLFETs. The study shows that RSD DG JLFETs successfully address mobility degradation, parasitic resistance, and short-channel effects that hinder traditional MOSFETs. By combining the raised source drain structure with the junctionless concept the device demonstrates improved carrier transport and electrostatic control.

2. RAISED SOURCE DRAIN DOUBLE GATE JLFET STRUCTURE

The device investigated in this work is a double-gate junctionless FET incorporating a raised source/drain architecture [15-16]. Fig. 1 shows an RSD DG JLFET structure. The raised source and drain regions are positioned above the channel plane to reduce series resistance and enhance carrier injection efficiency. The simulated channel length (L_{ch}) was varied from 20 nm to 100 nm to assess scaling behavior, while raised source/drain height (H_{sd}) ranged from 5 nm to 20 nm. The uniformly doped channel and source/drain regions had doping concentrations (N_{dop}) 10^{19}/cm^3. Gate oxide thickness (T_{ox}) was varied from 2 nm to 4 nm, and three dielectric materials: SiO_2, Si_3N_4 and HfO_2 were considered to evaluate the impact of dielectric properties on mobility. The work is performed on COGENDA Visual TCAD simulation platform. In all simulations Fermi-Dirac statistics without impact ionization is considered.

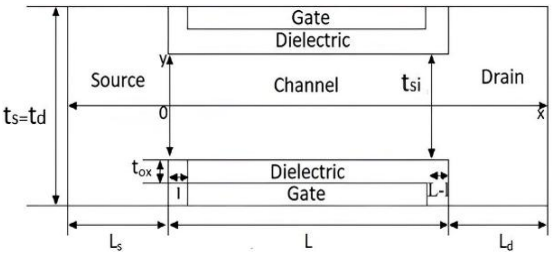

Fig. 1 – A RSD DG JLFET Structure [15-16]

3. ANALYTICAL MODEL DEVELOPMENT

The modified potential equation of RSD DG JLFET is:

$$\phi(x,y) = \phi_0(x) + \frac{4\varepsilon_{ox}}{t_{Si}(4t_{ox}\varepsilon_{Si}+t_{Si}\varepsilon_{ox}+t_g\varepsilon_g)}x + \left(\phi_{gs} - \phi_0(x)\right)y^2 \quad (1)$$

where, t_g is the permittivity of the additional gate layer and a? $?_g$ contribute to the gate capacitance.

Let,

$$C = \frac{4\varepsilon_{ox}}{t_{Si}(4t_{ox}\varepsilon_{Si}+t_{Si}\varepsilon_{ox}+t_g\varepsilon_g)}$$

$$\phi(x,y) = \phi_0(x) + Cx + \left(\phi_{gs} - \phi_0(x)\right)y^2 \quad (2)$$

$$E(x) = -\frac{\partial\phi}{\partial x} \quad (3)$$

$$\frac{\partial\phi}{\partial x} = \phi_0{}'(x) + C - \phi_0{}'(x)y^2 = \phi_0{}'(x)(1-y^2) + C \quad (4)$$

$$E_x(x) = -\phi_0{}'(x)(1-y^2) - C \quad (5)$$

$$E(y) = -\frac{\partial\phi}{\partial y} \quad (6)$$

$$\frac{\partial\phi}{\partial y} = 2y(\phi_{gs} - \phi_0(x)) \quad (7)$$

$$E(y) = -2y\left(\phi_{gs} - \phi_0(x)\right) = 2y2y(\phi_0(x) - \phi_{gs}) \quad (8)$$

4. RESULTS AND DISCUSSION

The results provide detailed insights into the carrier mobility characteristics of RSD DG JLFET under varying material and structural parameters. Figs. 2-5 illustrate the longitudinal electron mobility along the x-axis at $y = 0$. As shown in Fig. 2, the dielectric material significantly impacts electron transport. Devices with high-k HfO_2 demonstrated enhanced mobility compared to conventional SiO_2, owing to stronger electrostatic control and reduced scattering effects. Fig. 3 highlights the influence of gate oxide thickness where thinner oxides 2 nm yielded higher mobility than thicker ones 4 nm due to improved gate-channel coupling. Fig. 4 shows the effect of gate workfunction variation, where lower values 5.2 eV facilitated higher mobility by reducing the barrier height whereas higher workfunction 5.6 eV suppressed mobility and Fig. 5 demonstrates the role of temperature, with mobility degrading as temperature increased from 300 K to 700 K consistent with enhanced phonon scattering at elevated thermal conditions. The longitudinal hole mobility results presented in Figs. 6-8 exhibit similar behavior to electrons. As depicted in Fig. 6 high-k HfO_2 provided improved hole transport compared to SiO_2. Fig. 7 confirms that thinner oxides enhance hole mobility by maintaining stronger gate control while thicker oxides degrade performance. Fig. 8 shows that variations in gate workfunction affected hole mobility in a manner consistent with electron transport where mid-range values 5.4 eV offered a good compromise between mobility and threshold stability. Although hole mobilities were generally lower than electron mobilities due to larger effective mass of holes.

Transverse carrier mobility results further validate these observations. Figs. 9-12 present electron mobility along y-axis at $x = 0$. Fig. 9 high-k dielectrics again proved superior in enhancing transverse electron mobility. Fig. 10 demonstrates that thinner oxides yielded higher mobility while thicker oxides degraded performance. Fig. 11 illustrates the impact of workfunction where lower values promoted better carrier transport. Fig. 12 shows the degradation of mobility at higher temperatures reinforcing the detrimental role of phonon scattering. Hole mobility trends along the transverse axis are presented in Figs. 13-15 which follow the same behavior. Fig. 13 highlights the benefits of high-k dielectrics while Fig. 14 confirms the mobility degradation with increasing oxide thickness. Fig. 15 shows that workfunction variations once again influenced hole transport with lower values providing favourable mobility characteristics.

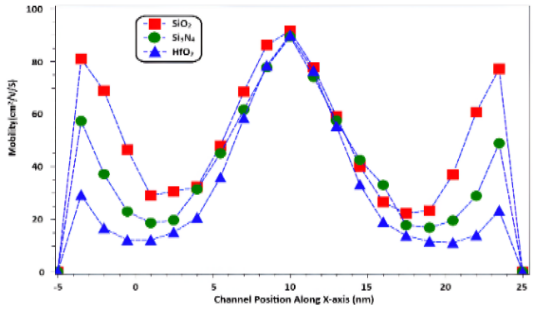

Fig. 2 – Electron mobility along longitudinal potential for x-axis at $y = 0$ for various dielectric materials

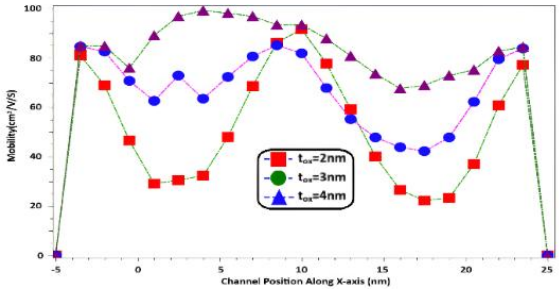

Fig. 3 – Electron mobility along longitudinal potential for x-axis at $y = 0$ for different dielectric thickness values

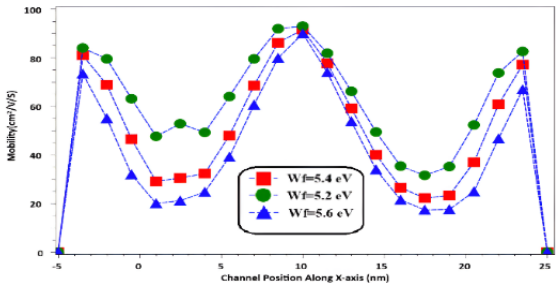

Fig. 4 – Electron mobility along longitudinal potential for x-axis at $y = 0$ for different workfunction values

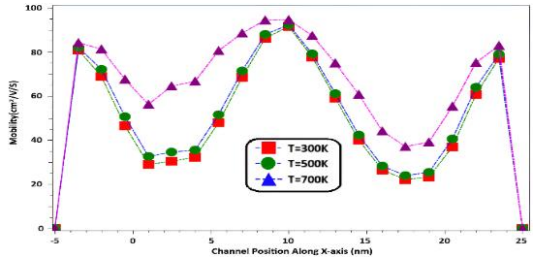

Fig. 5 – Electron mobility along longitudinal potential for x-axis at $y = 0$ under different temperature values

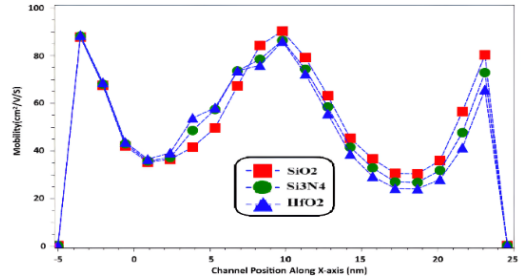

Fig. 6 – Hole mobility along longitudinal potential for x-axis at $y = 0$ for various dielectric materials

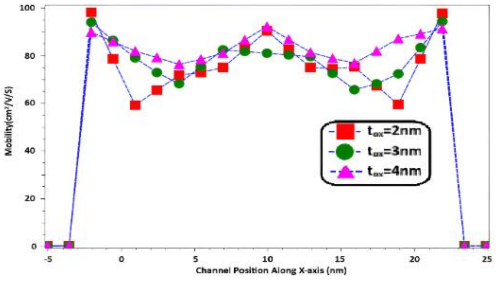

Fig. 7 – Hole mobility along longitudinal potential for x-axis at $y = 0$ for different dielectric thickness values

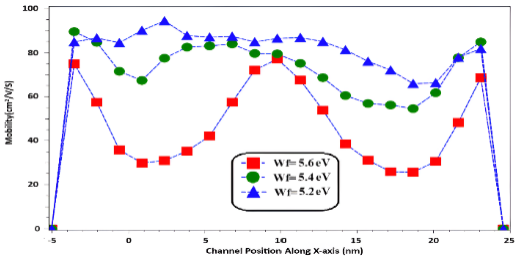

Fig. 8 – Hole mobility along longitudinal potential for x-axis at $y = 0$ for different workfunction values

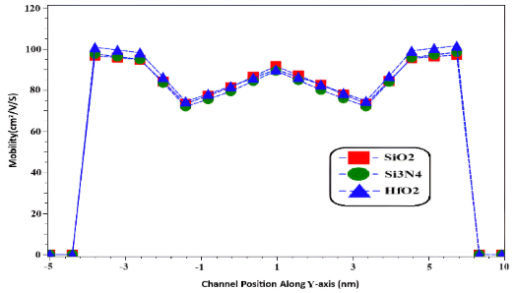

Fig. 9 – Electron mobility along transverse potential for y-axis at $x = 0$ for various dielectric materials

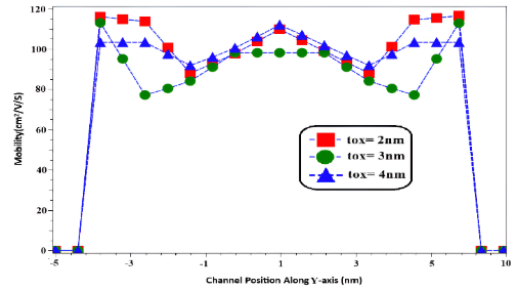

Fig. 10 – Electron mobility along transverse potential for y-axis at $x = 0$ for different dielectric thickness

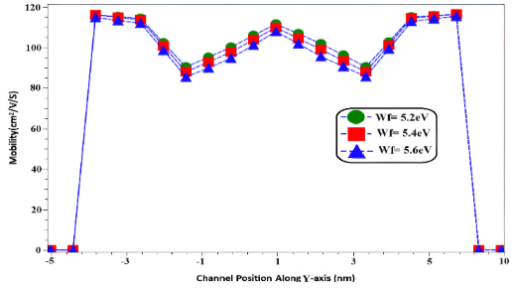

Fig. 11 – Electron mobility along transverse potential for y-axis at $x = 0$ for different workfunction values

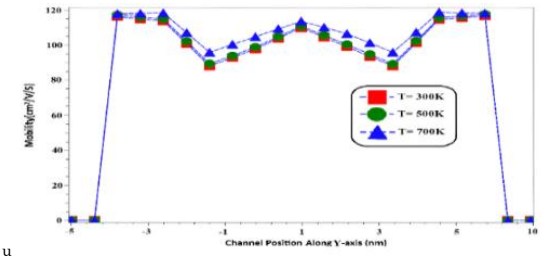

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Fig. 12 – Electron mobility along transverse potential for y-axis at $x = 0$ under different temperature values

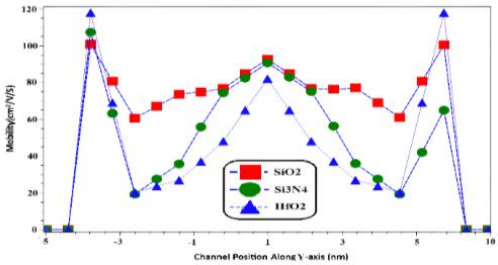

Fig. 13 – Hole mobility along transverse potential for y-axis at $x = 0$ for various dielectric materials

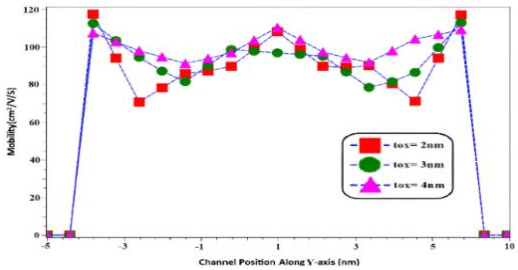

Fig. 14 – Hole mobility along transverse potential for y-axis at $x = 0$ for different dielectric thickness

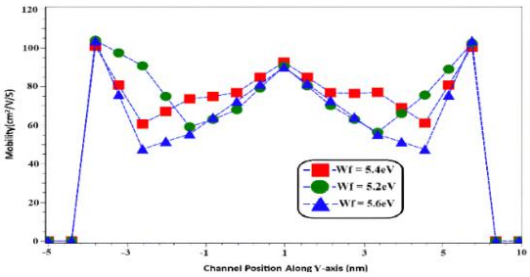

Fig. 15 – Hole mobility along transverse potential for y-axis at $x = 0$ for different workfunction values

5. CONCLUSIONS

A carrier mobility analysis of RSD DG JLFETs has been presented with a focus on its suitability for power device applications. Mobility degradation due to aggressive channel length scaling can be mitigated by using high-k dielectrics while optimal doping levels can balance ON-resistance and mobility. Thinner oxide layers improve mobility but must be optimized to balance leakage concerns. Workfunction provides a powerful design handle for tuning carrier transport and threshold control, while temperature remains a limiting factor due to phonon scattering. The integration of these design strategies makes the RSD DG JLFET a next-generation power electronics transistor where high current drive and low conduction losses are essential.

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Аналіз рухливості носіїв сигналу з двома затворами JLFET з піднятим витоком-стоком для силових пристроїв

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Постійне зменшення масштабу напівпровідникових приладів суттєво вплинуло на еволюцію передових транзисторних архітектур, здатних забезпечити високу продуктивність, мінімізуючи при цьому ефекти короткого каналу (SCE). Серед цих нових структур безперехідний польовий транзистор з піднятим витоком-стоком та двома затворними переходами (RSD DG JLFET), безперехідний прилад з піднятими областями витоку та стоку, привернув значну увагу завдяки своїй унікальній конструкції та експлуатаційним перевагам. Цей прилад пропонує чудовий електростатичний контроль над каналом, знижений паразитний послідовний опір та покращені властивості переносу носіїв заряду порівняно зі звичайними MOSFET та іншими безперехідними приладами. У цій роботі проведено комплексний аналіз рухливості носіїв заряду структур RSD DG JLFET для дослідження їх придатності. У дослідженні систематично розглядається вплив ключових фізичних параметрів, включаючи вибір діелектричного матеріалу, товщину діелектрика, роботу виходу затвора та робочу температуру. За допомогою TCAD-моделювання було оцінено залежність рухливості як електронів, так і дірок вздовж поздовжньої, так і поперечної осей приладу. Результати чітко демонструють, що піднята конфігурація витоку-стоку значно зменшує паразитні опори, які є основним обмеженням в агресивно масштабованих пристроях. Крім того, структурна модифікація також покращує електростатичну цілісність, тим самим підвищуючи загальну стабільність пристрою за різних умов зміщення. Спостерігалася підвищена рухливість носіїв заряду, що безпосередньо сприяє кращій здатності до керування струмом та зменшенню втрат провідності. Результати дослідження свідчать про те, що RSD DG JLFet має багатообіцяючий баланс між масштабуванням пристрою та надійністю роботи.

Ключові слова: JLFET, Підвищений стік джерела, Мобільність носіїв, Наноелектроніка, Силові пристрої.