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REGULAR ARTICLE

Impact of Body Material on Electrical Characteristics of Raised Source Drain Double Gate JLFET

R. Swargiary[1,*], K.C.D. Sarma[1], B.N. Thakur[2]

[1] *Department of Instrumentation Engineering, Central Institute of Technology, 783370 Kokrajhar, India*
[2] *Department of Electrical and Electronics Engineering, Bhilai Institute of Technology, 481001 Chhattisgarh, India*

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This paper presents the influence of body material properties on electrical characteristics of Raised Source Drain Double Gate Junctionless Field-Effect Transistor (RSD DG JLFET). A mathematical analysis of the drain current, threshold voltage and subthreshold swing considering Raised Source Drain region is performed to understand the device behavior. The study is carried out using TCAD-based simulations with five semiconductor materials: Silicon (Si), Germanium (Ge), Silicon Carbide (SiC), Gallium Nitride (GaN) and Gallium Arsenide (GaAs). The simulation results reveal that compound semiconductors particularly SiC and GaN demonstrate superior electrical performance compared to elemental semiconductors such as Si and Ge, primarily due to their higher carrier mobility and wider bandgap. The study systematically analyzes key device parameters including channel thickness, channel length, gate oxide thickness and gate oxide dielectric constant to assess their impact on device performance. The analysis indicates that SiC and GaN exhibit higher drain current, improved threshold voltage stability and lower subthreshold swing resulting in better device efficiency and reduced leakage currents under elevated temperatures. Overall, the findings demonstrate that wide-bandgap compound semiconductors, such as SiC and GaN, are highly promising for high-performance and thermally robust nanoelectronic applications.

Keywords: JLFET, Double gate, Raised source drain, Body materials.

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1. INTRODUCTION

The continuous scaling of semiconductor devices to nanometer dimensions has introduced major challenges in achieving reliable and high-performance transistors due to short-channel effects, random dopant fluctuations and complex junction formation. Raised source/drain (RSD) and junctionless transistor concepts have been explored to overcome short-channel effects, parasitic resistance and dopant fluctuation issues in nanoscale devices. Early works by Pfiester *et al.* [1] and Rodder and Yeakley [2] introduced elevated S/D MOSFETs to reduce resistance, while Waite et al. [3] demonstrated the influence of epitaxial layer thickness on short-channel behaviour. Kallepelli and Maheshwaram [4] later proposed a circular double-gate SOI MOSFET with RSD to enhance drive current and suppress leakage. Meanwhile Colinge and Lee [5-6] pioneered junctionless FETs in which uniformly doped channels eliminate abrupt junctions, simplifying fabrication and improving variability control. Theoretical models for junctionless nanowire FETs were subsequently developed by Gnani et al. [7], while Colinge et al. [8] provided experimental validation of nanowire JLFETs. The integration of RSD architecture with JLFET technology has since emerged as a hybrid design strategy that effectively reduces parasitic resistance and enhances drive current critical parameters for high-speed, low-power electronic systems. Comprehensive reviews by Siddiqui et al. [9] and Raut et al. [10] have further emphasized the advantages of JLFETs in terms of simplified fabrication, strong electrostatic control and scalability for nanoscale applications. Ramaswamy and Kumar [11] proposed a Raised Source/Drain Dopingless Junctionless Accumulation Mode FET focusing on improved electrostatic control and reduced series resistance, while Chen et al. [12] demonstrated a gated raised source/drain poly-Si nanowire FET achieving better gate control and enhanced current transport. Recent simulation studies by Sarma et al. [13-14] on RSD double-gate JLFETs have shown further performance improvements through optimized structural configurations. Franklin [15] explored the role of nanomaterials in thin-film applications, while Talukdar et al. [16] demonstrated the critical influence of body material properties on electrical performance of junctionless transistors.

This work study comparative assessment of different semiconductor body materials Si, Ge, SiC, GaN, and GaAs in the RSD DG JLFET configuration. The study provides valuable insights into how material properties influence electrical characteristics of RSD DG JLFET. This work bridges the gap between material engineering and device physics.

* Correspondence e-mail: ph22ie1001@cit.ac.in

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2. RAISED SOURCE DRAIN DOUBLE GATE JLFET STRUCTURE

The device studied is a double-gate junctionless FET with an RSD architecture [12-13], as shown in Figure 1. The elevated source/drain regions reduce series resistance and improve device performance. Simulations were carried out with channel lengths (L_{ch}) from 20-100 nm and raised source/drain heights (H_{sd}) of 5-20 nm. A uniformly doped channel and source/drain regions (N_{dop} = 10^{19}/cm^3) were used with five semiconductor materials: Si, Ge, SiC, GaN and GaAs. All simulations employed the COGENDA Visual TCAD platform using Fermi-Dirac statistics without impact ionization.

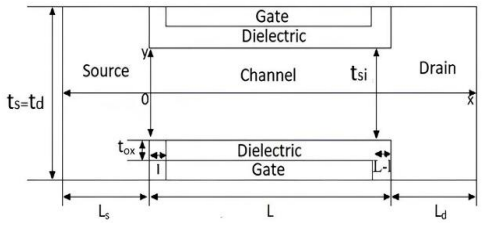

Fig. 1 – An RSD DG JLFET Structure [12-13]

3. ANALYTICAL MODEL DEVELOPMENT

The channel conductance is given by

$$G_{ch} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \quad (1)$$

where, μ: carrier mobility, $C_{ox}: \frac{\epsilon_{ox}}{t_{ox}}$, ϵ_{ox} is permittivity of the oxide, t_{ox} is gate oxide thickness, W is device width, L is channel length, V_{GS} is gate-to-source voltage, V_{th} is threshold voltage.

Raised source drain series resistance of rectangular cross-section is

$$R_{sd} = \frac{L_{sd}}{q\mu N_{dop} W H_{sd}} \quad (2)$$

where, L_{sd} raised source drain length, q: electron charge, N_{dop} channel doping, H_{sd} raised source drain height

The on-state current considering raised source drain voltage drop

$$I_{on} = \frac{G_{ch} V_{DS}}{1+G_{ch} R_{sd}} = \frac{\mu C_{ox} \frac{W}{L} (V_{GS}-V_{th})}{1+\frac{C_{ox} L_{sd}}{qN_{dop} L H_{sd}} (V_{GS}-V_{th})} \quad (3)$$

Where, V_{DS} is drain to source voltage.

Threshold voltage considering raised source drain region is

$$V_{th,RSD} = \frac{1}{k_{RSD}} \left(\frac{qN_{dop} t_{si,eff}^2}{8\epsilon_{si}} \right) - \frac{Q_{ox}}{C_{ox}} \quad (4)$$

where, $K_{RSD} = 1 + \gamma \frac{H_{sd}}{t_{si,eff}}$ = multiplicative factor that accounts for the electrostatic screening of the raised source drain region, γ is fitting constant to be extracted from TCAD, $t_{si,eff}$ is effective silicon body thickness, ϵ_{si} is permittivity of silicon, Q_{ox} is fixed oxide charge per unit area.

The standard subthreshold swing is

$$SS = \ln(10) \frac{kT}{q} \left(1 + \frac{C_{dep}}{C_{ox}} \right) \quad (5)$$

where, k is Boltzmann constant, T is absolute temperature and C_{dep} is depletion capacitance.

Raised source drain effect on effective capacitance:

$$C_{ox,eff} = C_{ox} \left(1 + \delta \frac{H_{sd}}{t_{ox}} \right) \quad (6)$$

where, δ Fitting constant to be extracted from TCAD.

The subthreshold swing with raised source drain is

$$SS = \ln(10) \frac{kT}{q} \left(1 + \frac{C_{dep}}{C_{ox,eff}} \right) \quad (7)$$

4. RESULTS AND DISCUSSION

The Fig. 2 shows transfer characteristics of RSD DG JLFET illustrating drain current plot with gate to source voltage for different body materials Si, SiC, Ge, GaN and GaAs. Each material's bandgap, mobility, dielectric constant and effective mass strongly affect current conduction and electrostatics. Si offers balanced performance with moderate threshold voltage, good subthreshold slope and a reliable ON/OFF ratio. SiC with its wide bandgap 3.2 eV provides low leakage and high breakdown strength making it suitable for high-power, high-temperature use at lower ON current due to reduced mobility. Ge delivers very high ON current from its superior mobility but suffers from high leakage and low threshold voltage due to its narrow bandgap. GaN combines wide bandgap and high mobility achieving strong gate control, high ON current, low leakage and a sharp subthreshold slope making it ideal for high-frequency and high-power devices. GaAs with very high mobility and moderate bandgap also ensures good ON current but shows slightly higher leakage and weaker threshold control compared to GaN or Si. Overall, Ge and GaN enhance ON-state performance, SiC suppresses leakage, and Si provides balanced characteristics highlighting that body material selection should align with specific application needs.

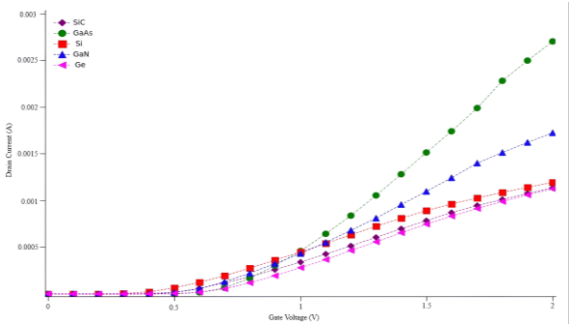

Fig. 2 – Transfer Characteristics Comparison for JLFET with Different Body Materials

Figs. 3-6 present the variation of On-State Current (I_{on}) in RS DG JLFET with respect to channel thickness, dielectric constant, channel length and gate oxide thickness for five materials Si, SiC, Ge, GaN and GaAs. I_{on} shows strong dependence on these parameters highlight-

ing their importance in device optimization. As channel thickness increases from 5-12 nm shown in Fig. 3 Ion rises for all materials due to reduced resistance and better carrier transport with GaAs showing the highest values and Ge the lowest. With higher dielectric constant shown in Fig. 4 Ion also increases driven by stronger electrostatic control favouring GaAs and GaN for high-performance applications. In contrast, I_{on} decreases with longer channel lengths 10-30 nm shown in Fig. 5 because of higher resistance and weaker electric fields emphasizing the advantage of shorter channels despite potential short-channel effects. Finally, increasing gate oxide thickness 2-6 nm shown in Fig. 6 lowers Ion as thinner oxides enhance gate control and channel formation thereby improving drive current.

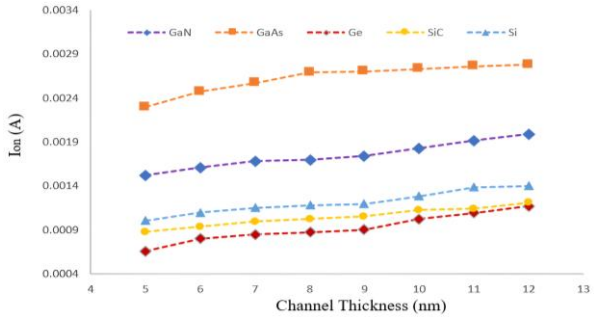

Fig. 3 – Effect of channel thickness on On-state current

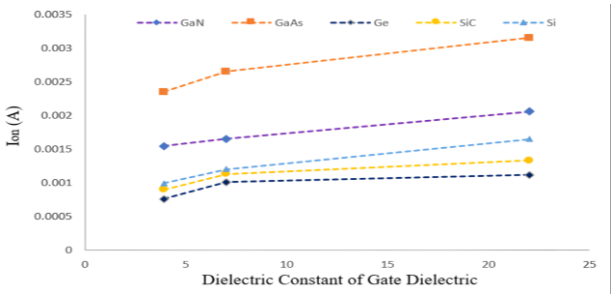

Fig. 4 – Dielectric constant of gate oxide effect on On-state current

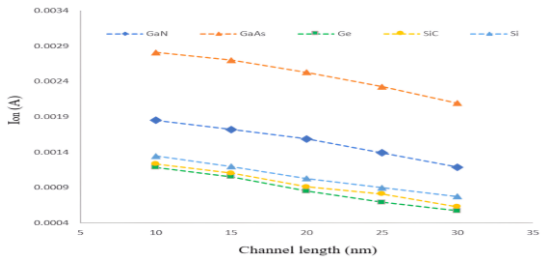

Fig. 5 – Effect of channel length on On-state current

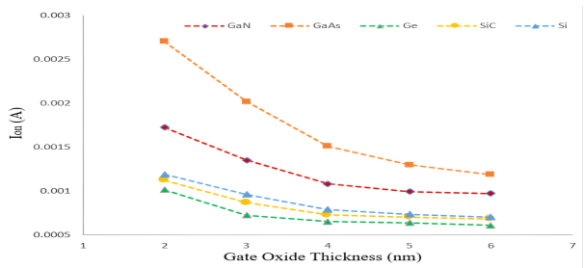

Fig. 6 – Effect of gate oxide thickness on On-state current

The threshold voltage characteristics of RSD DG JLFETs shown in Figs. 7-10 influenced by channel thickness, dielectric constant, channel length and gate oxide thickness for different body materials Si, SiC, Ge, GaN and GaAs. Threshold voltage is highly sensitive to these parameters varying distinctly across materials. As channel thickness increases from 5-15 nm shown in Fig. 7 threshold voltage decreases due to weaker gate control with Ge and GaAs showing higher values at thinner channels, while Si remains lowest. Increasing dielectric constant shown in Fig. 8 improves threshold voltage for all materials by enhancing gate capacitance with GaAs, Ge, and GaN showing strong gains. Longer channel lengths 5-15 nm shown in Fig. 9 yield higher threshold voltage confirming higher short-channel effects with GaAs showing the steepest rise. In contrast,

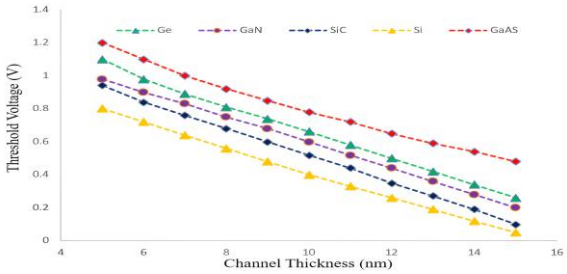

Fig. 7 – Effect of channel thickness on threshold voltage

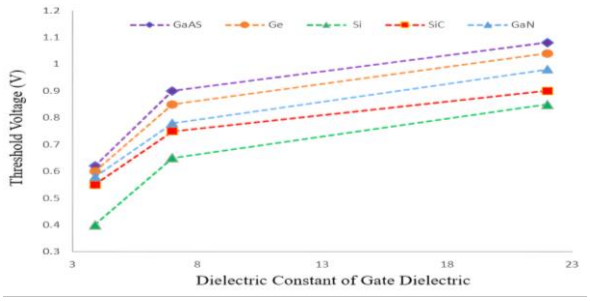

Fig. 8 – Dielectric constant of gate oxide effect on threshold voltage

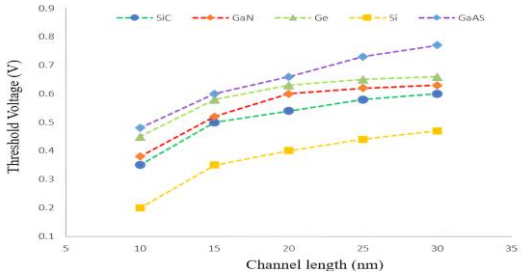

Fig. 9 – Effect of channel length on threshold voltage

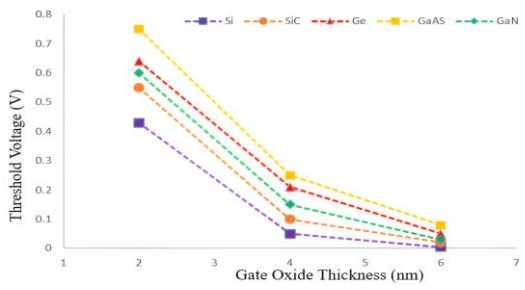

Fig. 10 – Effect of gate oxide thickness on threshold voltage

thicker oxides 2-6 nm shown in Fig. 10 shows threshold voltage variation across all materials showing GaAS at higher value with fall in rising oxide thickness.

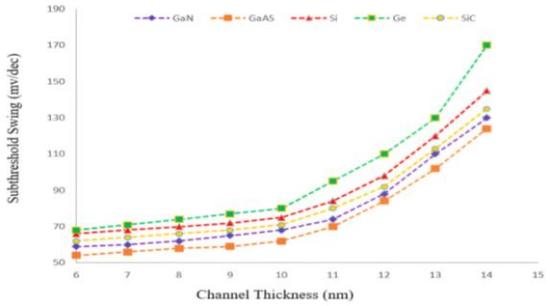

Fig. 11 – Effect of channel thickness on subthreshold swing

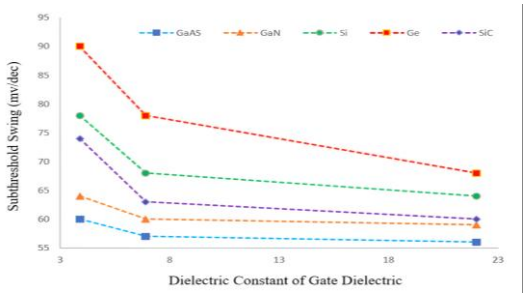

Fig. 12 – Dielectric constant of gate oxide effect on subthreshold swing

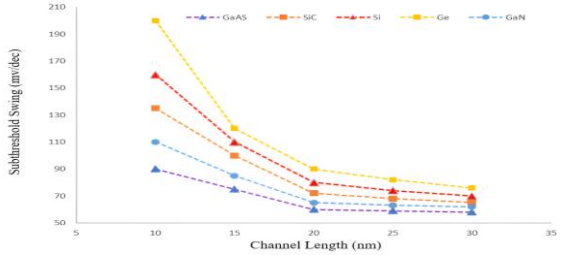

Fig. 13 – Effect of channel length on subthreshold swing

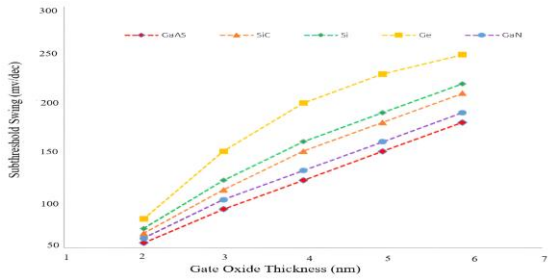

Fig. 14 – Effect of gate oxide thickness on subthreshold swing

Figs. 11-14 illustrate the subthreshold swing of RSD DG JLFETs for different body materials Si, SiC, Ge, GaN and GaAs under varying device parameters. Subthreshold swing increases with channel thickness as shown in Fig. 11 across all materials due to weaker gate control indicating degraded switching with thinner channels proving more effective for low- subthreshold swing operation. Higher dielectric constant shown in Fig. 12 lowers subthreshold swing by improving gate-to-channel coupling thereby enhancing switching performance. With longer channel lengths 10-30 nm shown in Fig. 13, subthreshold swing decreases for all materials as short-channel effects are suppressed. In contrast, thicker gate oxides 2-6 nm shown in Fig. 14 raise subthreshold swing in gate oxide by reducing gate control leading to poorer switching and higher subthreshold conduction.

5. CONCLUSIONS

A comprehensive comparative simulation study of RSD DG JLFETs based on elemental and compound semiconductors has been conducted by analyzing key electrical characteristics. The results clearly demonstrate that RS DG JLFET based on compound semiconductors exhibit superior electrical performance compared to their elemental counterparts. Despite their superior performance it is important to note that compound semiconductors typically involve higher material and fabrication costs compared to traditional elemental semiconductors.

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Вплив матеріалу корпусу на електричні характеристики двозатворного JLFET з піднятим витоком-стоком

R. Swargiary[1], K.C.D. Sarma[1], B.N. Thakur[2]

[1] *Department of Instrumentation Engineering, Central Institute of Technology, 783370 Kokrajhar, India*
[2] *Department of Electrical and Electronics Engineering, Bhilai Institute of Technology, 481001 Chhattisgarh, India*

Gредставлено вплив властивостей матеріалу корпусу на електричні характеристики безпольового транзистора з піднятим витоком та двома затворними переходами (RSD DG JLFET). Для розуміння поведінки пристрою проведено математичний аналіз струму стоку, порогової напруги та підпорогового коливання з урахуванням області піднятого витоку та стоку. Дослідження проведено за допомогою моделювання на основі TCAD з п'ятьма напівпровідниковими матеріалами: кремнієм (Si), германієм (Ge), карбідом кремнію (SiC), нітридом галію (GaN) та арсенідом галію (GaAs). Результати моделювання показують, що складні напівпровідники, зокрема SiC та GaN, демонструють кращі електричні характеристики порівняно з елементарними напівпровідниками, такими як Si та Ge, головним чином завдяки їхній вищій рухливості носіїв заряду та ширшій забороненій зоні. У дослідженні систематично аналізуються ключові параметри пристрою, включаючи товщину каналу, довжину каналу, товщину затворного оксиду та діелектричну проникність затворного оксиду, для оцінки їхнього впливу на продуктивність пристрою. Аналіз показує, що SiC та GaN демонструють вищий струм стоку, покращену стабільність порогової напруги та нижчий підпороговий розмах, що призводить до кращої ефективності пристрою та зменшення струмів витоку за підвищених температур. Загалом, отримані результати демонструють, що широкозонні складні напівпровідники, такі як SiC та GaN, є дуже перспективними для високопродуктивних та термічно стійких наноелектронних застосувань.

Ключові слова: JLFET, Подвійні ворота, Піднятий витік джерела, Матеріали корпусу.