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REGULAR ARTICLE

Impact of Hole Density on Sub-10 nm SOI Trigate MOSFET Using Charge Plasma Technique with Circuit-Level Analysis

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In this work, the charge plasma (CP) technique is employed to induce carriers in the undoped channel region of a Silicon-on-Insulator (SOI) trigate MOSFET, eliminating the need for conventional doping and reducing variability at nanoscale dimensions. A metal layer with a suitably engineered work function (WK) is incorporated beneath the channel to electrostatically induce carriers in the intrinsic silicon region, enabling efficient channel formation. The device performance is analyzed in terms of carrier distribution, surface potential profile, current–voltage (*I-V*) characteristics, and transconductance, along with circuit-level evaluation through Voltage Transfer Characteristics (VTC) of inverter configurations and stability assessment of 6T SRAM cells for a channel length of 10 nm. Simulations are carried out using Sentaurus TCAD with advanced physical models, including the Lombardi mobility model to account for surface scattering, Shockley–Read–Hall (SRH) and Auger recombination models for carrier recombination, and the Density-Gradient model to capture quantum confinement effects. The incorporation of a high-k dielectric significantly reduces leakage current and enhances electrostatic control. It is observed that Drain-Induced Barrier Lowering (DIBL) can be effectively suppressed and tuned by optimizing the work function of the metal layer beneath the channel. As a result of the CP implementation, the proposed device demonstrates a 16 % improvement in drain current compared to the conventional SOI MOSFET. Furthermore, the implemented 6T SRAM circuits exhibit a 28 % enhancement in hold static noise margin, indicating improved stability and reliability, thereby making the proposed CP-based SOI trigate MOSFET a strong candidate for future low-power and high-performance applications.

Keywords: MOSFET, Plasma, SRAM, TCAD.

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1. INTRODUCTION

It is challenging to scale down the conventional MOSFET transistor to the nano scale while maintaining the same output current and control the short channel effects (SCE). Even though different gate structures implemented to control the leakage current, the SOI Tri gate MOSFET is still superior in gate control, leakage reduction and scalability improvement than conventional MOSFETs [1-3]. Another reason for an increase in leakage current is due to chemical doping in the semiconductor devices and also when the device is scaled down to nanodevices, it is a complex issue to perform chemical doping. By using intrinsic channel and electrostatic doping meth-od, chemical doping can be avoided in nano scale devices [4]. The intrinsic channel improves carrier mobility, reduces leakage and enhances electrostatic control, leading to better performance in device. When a channel is an intrinsic, the body scattering effect gets reduced and drift current improved in the device [5-9]. CP is one of the methods of electrostatic doping, in which electron and hole carriers are induced in the intrinsic semiconductor by placing metal over intrinsic semiconductor [10-11]. CP has been implemented in PN diode, TFET, BJT and it proves as one of the best alternative methods for chemical doping.

In all the above-mentioned devices, CP is performed in the source and drain region not in the channel region. As the device is scaled down, the I_{ON}/I_{OFF} ratio will steadily decrease and the leakage current will increase due to the SCE. High-*k* dielectrics are therefore among the best candidates for reducing leakage current and increasing the I_{ON}/I_{OFF} ratio [12-14]. Because high-k dielectric materials have a higher surface area, they seem to have better properties when nano sized than SiO_2. In this article charge plasma concept is used in channel region of SOI Trigate Un doped MOSFET to induce carriers by placing metal layer between Box and channel region mean while HfO_2 is used to control the leakage current. The rest of the article is divided into proposed device structure, results and discussion and conclusion sections.

2. DEVICE STRUCTURE

The device structure created in Sentaurus TCAD is illustrated in Fig. 1(a), with parameters taken from [1].

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The potential results obtained from TCAD align well with those reported in [1], as shown in Fig. 2. In [1], SiO_2 is employed as the gate oxide with a mid-gap gate material, and the channel is nearly un-doped. In the proposed device the same structure channel length has been reduced to 10 nm and analysis has been done by incorporating metal layer (CP Method) in between box and channel region which is used to induce carriers in the channel region. Under equilibrium conditions, the metal placed beneath the channel in-duces carriers based on its work function states that when the metal work function is higher than that of intrinsic silicon, it induces hole accumulation in the channel, whereas a lower metal work function induces electron accumulation.

To analyses the CP concept in the channel region, work functions of 3 eV, 4 eV, and 5 eV are utilized for the channel metal contact positioned beneath the channel. A metal semiconductor contact with a gate length of 0.5 nm from the source to the channel is introduced to minimize the likelihood of silicide formation.

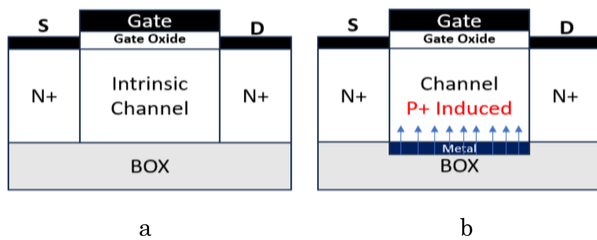

Fig. 1 – a) Conventional device b) Proposed device

The device architecture, shown in Fig. 1, is simulated using the Lombardi mobility model along with Shockley Read Hall (SRH) and Auger recombination models to account for minority carrier re-combination. Additionally, the Density-Gradient model is incorporated to capture quantum confinement effects [15]. The same modelling approach is adopted in this work, as the proposed device also exhibits quantum effects at shorter gate lengths.

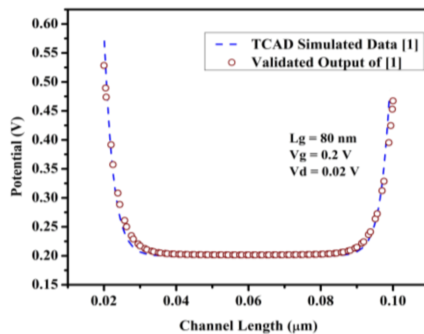

Fig. 2 – Validation of conventional structure [1]

3. RESULTS AND DISCUSSION

The output characteristics depicted in the Fig. 3 for different metal work functions to compare the ID with drain voltage of the conventional SOI MOSFET and CP SOI MOSFET. With constant device dimensions (channel length = 10 nm, channel thickness = 5 nm, oxide thickness = 1 nm, metal thickness = 1 nm, and channel width = 5 nm), the simulations are run with VG =1 V and VD = 1 V. Under the same biasing conditions, moreover the CP SOI MOSFET has a higher drain current than the SOI MOSFET. The device with the lowest metal work function (WK = 3 eV) among the CP SOI MOSFETs exhibits the maximum drain current, but raising the work function to 5 eV causes a distinct decrease in drain current. This behaviour can be attributed to the modulation of the carrier concentration and potential barrier in the charge plasma channel region. A lower work function metal induces a higher concentration of electrons in the channel region, effectively lowering the threshold voltage and enhancing the carrier injection from the source to the drain. Consequently, the current conduction improves, and the CP SOI MOSFET achieves superior drive capability. The higher metal work function increases holes density and suppresses drain current by raising the channel potential barrier. The charge plasma device has an intrinsic channel with lower impurity scattering and higher carrier mobility than the traditional doped SOI MOSFET. The CP SOI MOSFET exhibits better electrostatic control and current drivability, particularly for optimal metal work function values. The enhanced cur-rent performance demonstrates the charge plasma approach to be potential for the upcoming nano scale device applications that has a low threshold voltages and high drive currents. The IOFF current for the SOI MOSFET is 2.6×10^{-13} A, while for the CP SOI MOSFET it is 1.24×10^{-14} A. The inclusion of the CP structure effectively reduces the leakage current in the CP SOI MOSFET.

The Fig. 4 compares the DIBL characteristics of a CP SOI MOSFET with a conventional SOI MOSFET for various metal WK. Enhanced electrostatic control over the channel and better immunity to short-channel effects are shown by the CP SOI MOSFET's noticeably lower DIBL when compared to the conventional SOI MOSFET. The Fig. 5 shows the trans conductance (gm) characteristics of CP and conventional SOI MOSFETs with various metal work functions (WK = 3 eV, 4 eV, and 5 eV) at a channel length of 10 nm and a drain voltage VD = 1 V. Among all the de-vices, the CP SOI MOSFET with a metal work function of 3 eV has the greatest peak trans conductance, followed by WK = 4 eV and WK = 5 eV.

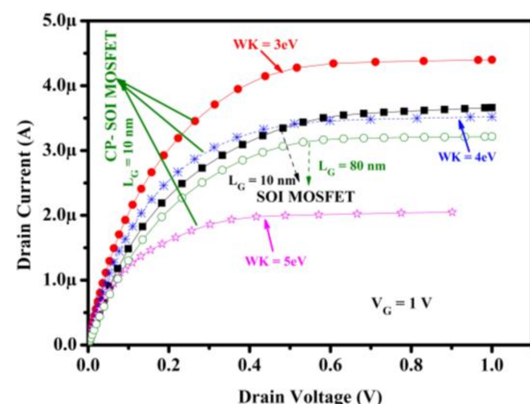

Fig. 3 – Output Characteristics of SOI MOSFET and CP-SOI MOSFET with different work function

In contrast, the conventional SOI MOSFET exhibits relatively lower trans conductance. This indicates that lowering the metal work function enhances the carrier concentration in the channel region, thereby improving gate control and channel conductivity. As a result, the CP SOI MOSFET achieves higher trans conductance, signifying greater current-driving capability and faster switching performance. Conversely, as the work function increases, the induced electron density decreases and hole density increases, leading to reduced trans conductance.

The Fig. 6 shows the performance of a Charge Plasma SOI MOSFET and a conventional SOI MOSFET using transient response characteristics. The CP SOI MOSFET and conventional SOI MOSFET curves illustrate the output responses of both devices, while the input waveform, displays a typical square wave signal. In comparison to the conventional SOI MOSFET, the CP SOI MOSFET exhibits faster transitions at both the rising and falling edges, suggesting a decreased propagation delay and improved switching speed. The metal creates a high-density carriers, low-resistance channel free of impurity dispersion when the charge-plasma idea is used in the channel area. This greatly reduces the inverter delay by increasing the driving current and enabling the output node capacitance to charge and discharge more quickly. Fig. 7 shows the 6T SRAM circuit build using SOI MOSFET and CP SOI MOSFET. The Static Noise Margin (SNM) comparison of SOI MOSFET and CP SOI MOSFET based 6T SRAM cells during hold operations is represented by the butterfly curves in Fig. 8.

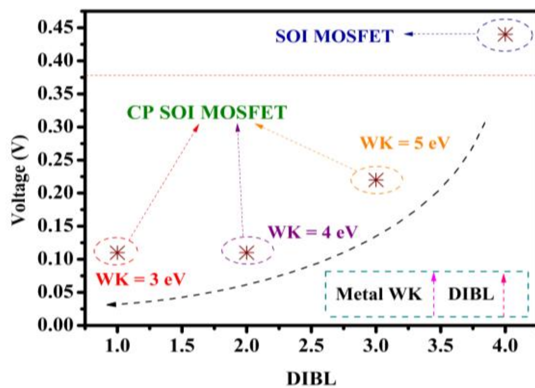

Fig. 4 – DIBL analysis of SOI MOSFET and CP-SOI MOSFET

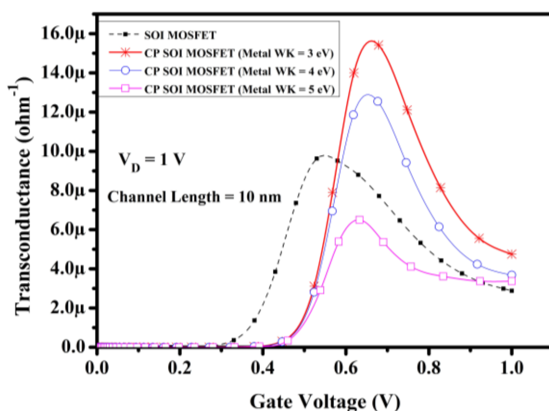

Fig. 5 – Transconductance analysis of SOI MOSFET and CP-SOI MOSFET

When compared to the traditional SOI MOSFET based SRAM, the CP SOI MOSFET-based SRAM displays higher SNM values (SNM1 and SNM2) in both graphs. This suggests that during both hold and read modes, CP SOI MOSFET cells have greater stability and a more robust resistance to noise disturbances. The higher SNM during the hold mode indicates better data retention capacity, which means stored data is more resilient to noise and leakage. The improved SNM of the CP SOI MOSFET-based cell indicates higher read stability and less read disturb effects during the read mode, ensuring reliable access without unintended bit flipping. Table 1 also assures the same.

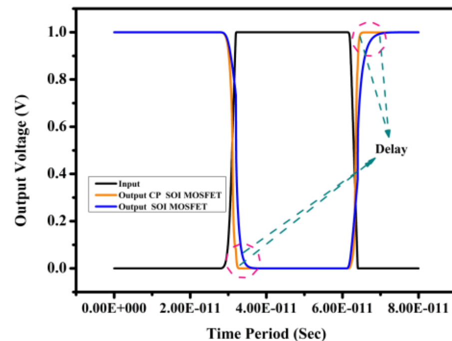

Fig. 6 – Delay response of SOI MOSFET and CP SOI MOSFET

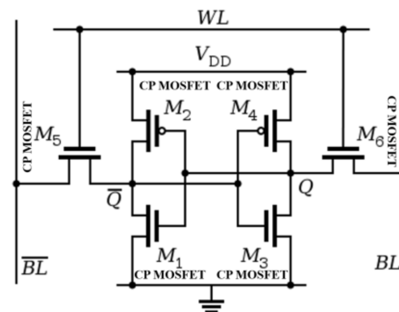

Fig. 7 – 6T SRAM Circuit

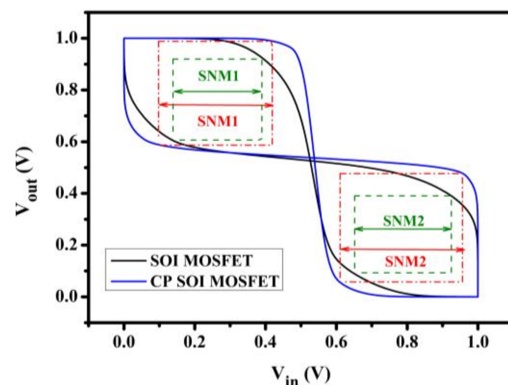

Fig. 8 – SRAM hold analysis of SOI MOSFET and CP SOI MOSFET

Table 1

	SOI MOSFET		CP SOI MOSFET	
	SNM1 (V)	SNM2 (V)	SNM1 (V)	SNM2 (V)

HOLD	0.26	0.28	0.33	0.36
READ	0.08	0.08	0.22	0.16
WRITE	0.04	0.10	0.06	0.12

4. CONCLUSION

In the proposed work, charge plasma is introduced within the intrinsic channel of an SOI Trigate MOSFET, addressing the limitations associated with the conventional doping techniques at the nano level. The results indicate the proposed CP-SOI Trigate MOSFET demonstrates a notable enhancement in device performance metrics, like increased drain current, high hole density, and control of leakage current. The electrostatic potential and band diagrams indicate that the incorporation of charge plasma significantly lowers the potential barrier between the source and channel, thereby enhancing carrier transport efficiency. Around 75% DIBL is reduced while using CP SOI MOSFET compared with conventional device. Additionally, the leakage current is significantly reduced, making the device perfect for low-power applications like SRAMs with 50% write noise stability compare with conventional SOI MOSFET.

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Вплив щільності отворів на тригейтний MOSFET на основі КНІ розміром менше 10 нм з використанням методу зарядової плазми з аналізом на рівні схеми

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У цій роботі використовується метод зарядової плазми (ЗП) для індукції носіїв заряду в нелегованій області каналу тригейтного MOSFET-транзистора типу «кремній на ізоляторі» (КНІ), що усуває необхідність традиційного легування та зменшує мінливість у нанорозмірах. Металевий шар з відповідно розробленою роботою виходу (РВ) вбудований під канал для електростатичного індукування носіїв заряду у власній області кремнію, що забезпечує ефективне формування каналу. Характеристики пристрою аналізуються з точки зору розподілу носіїв, профілю поверхневого потенціалу, вольт-амперних (ВАХ) характеристик та крутизни, а також оцінки на рівні схеми за допомогою характеристик передачі напруги (ХПН) конфігурацій інвертора та оцінки стабільності 6T SRAM-комірок для довжини каналу 10 нм. Моделювання проводиться за допомогою Sentaurus TCAD з використанням передових фізичних моделей, включаючи модель рухливості Ломбарді для врахування поверхневого розсіювання, моделі рекомбінації Шоклі-Ріда-Холла (ШРХ) та Оже для рекомбінації носіїв, а також модель градієнта густини для

врахування ефектів квантового обмеження. Включення діелектрика з високим k значно зменшує струм витоку та покращує електростатичний контроль. Спостерігається, що зниження бар'єру, індукованого стоком (DIBL), може бути ефективно придушене та налаштоване шляхом оптимізації роботи виходу металевого шару під каналом. В результаті реалізації ЗП, запропонований пристрій демонструє 16 % покращення струму стоку порівняно зі звичайним КНІ MOSFET. Крім того, реалізовані схеми 6T SRAM демонструють 28 % покращення запасу статичного шуму утримання, що свідчить про покращену стабільність та надійність, тим самим роблячи запропонований КНІ тригейтовий MOSFET на основі ЗП сильним кандидатом для майбутніх низькоенергетичних та високопродуктивних застосувань.

Ключові слова: MOSFET, Плазма, SRAM, TCAD.