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REGULAR ARTICLE

# Leveraging Gate and Channel Engineering in Graphene Tunnel FET (GTFET) at Nano-Scale for Better Device Performance

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This research work mainly focuses on various gate and channel engineering performed on typical tunnel field effect transistors (TFETs) at nano scale. This step-by-step development of typical nano device TFET model is showcased in this research work, in pursuit of better device performance. At first single gated homogenous dielectric i.e., $SiO_2$ is used as oxide material, which further modified to dual gated heterogenous dielectric i.e. $HfO_2$ – $SiO_2$ combination in pursuit of better drive current ($I_{ON}$), and switching ratio ($I_{ON}/I_{OFF}$). During this process simulation the intrinsic channel is developed as heterogeneous (InAs-Si) throughout the simulation. This results in considerable changes at surface potential distribution along the channel due to band-to-band-tunneling effect (BTBT). Secondly, this dual gated heterogeneous dielectric TFET is modified with 0-2 nm thin graphene layer, deployed over intrinsic channel. This nano-scaled graphene layer is introduced as nano-ribbon architecture, in order to reduce the tunable energy band gap. This expedites the BTBT tunneling across the junction and brings the turn on voltage ($V_{ON}$) much earlier, resulting fast digital switching. Lastly, this structure of TFET is further updated with dual metal, dual gated structure to investigate its $I_{ON}/I_{OFF}$ ratio and leakage current control. Silvaco TCAD is used to generate all related simulation work. Better drive current ($I_{ON}$) is achieved at $3.55 \times 10^{-6}$ A/μm with minimum leakage current ($I_{OFF}$) of $2.16 \times 10^{-16}$ A/μm at 0.5 supply voltage ($V_{DD}$) with minimum sub-threshold swing (SS) of 33.07 mV/decade.

**Keywords**: GTFET, TCAD, Nano-Ribbon, Quantum tunneling.

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## 1. INTRODUCTION

Device scaling from medium scale to nano scale and from nano scale to micro scale has been challenging as far as chip fabrication is concerned. Starting from the Moore's law, we have seen how number of transistors on a nano-chip doubles approximately in every two years, resulting exponential growth in computing power and efficiency [1-2].

The quantum tunneling mechanism outplays the orthodox classical approach of carrier transport by introducing band-to-band tunneling (BTBT) as shown in Fig. 1. In classical approach, current flows by thermionic emission, gets limited subthreshold slope (SS) by 60 mV/decade [3].

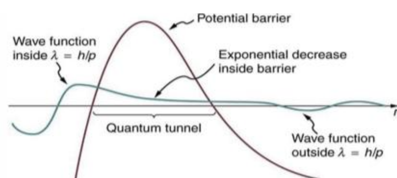


**Fig. 1** – Quantum tunneling mechanism resulting Quantum Tunnel for ultra-fast carrier transport

Whereas, quantum tunneling utilizes the Heisenberg uncertainty principle results high on-state current ($I_{ON}$) at low threshold voltage ($V_{th}$). Instead of overcoming the barrier, in this approach electrons quantum mechanically tunnel from valence band to conduction band of the channel.

## 2. PROPOSED DEVICE MODEL AT NANO SCALE (STEP BY STEP APPROACH)

At first a thorough literature survey related to different physical TFET device structures, starting from base level homogeneous to typical symmetric, asymmetric, homo and heterogeneous structures is performed [4-10]. We have applied different gate and channel engineering to our established device model. At first single gated device model with homogenous dielectric as $SiO_2$ (i.e. Silicon Di Oxide) is developed.

### 2.1 Single Gated Homogeneous Dielectric

At this stage single metal, single gated homogeneous dielectric ($SiO_2$) is used throughout the channel. The channel is intrinsic and heterogenous i.e. InAs-Si based channel. Reason behind this is to develop better current transfer ratio between source – channel junction region for forward bias, and channel – drain junction for reverse bias of gate voltage ($V_G$). The device model is showcased in Fig. 2 (a) below. Indium – Arsenide (In-As) having smaller effective mass avoids scattering and supports high electron mobility, compared to Silicon material [11].

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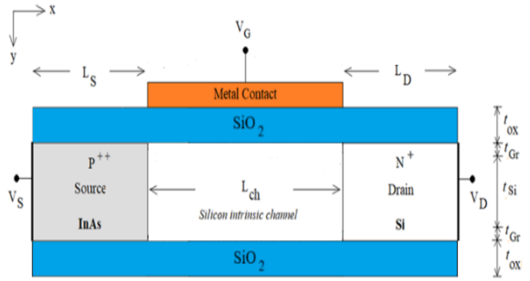


**Fig. 2** (a) – Single gated homogeneous dielectric TFET (SG-Ho-TFET)

## 2.2 Dual Gated Heterogeneous Dielectric

In order to witness better control over intrinsic channel and reduced leakage current, the single gated structure is further updated with dual gate i.e. top gate and bottom gate, as shown in Fig. 2 (b). By introducing top and bottom gate to the device model, eventually provides stronger control over electrostatic potential across the channel region. These results improved subthreshold slope and better switching performance.

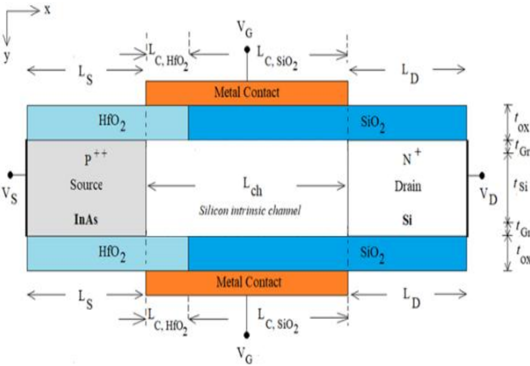


**Fig. 2** (b) – Dual gated heterogeneous dielectric TFET (DG-He-TFET)

In this situation, the band to band tunneling (BTBT) increases as tunneling barrier height and width can be modulated more effectively with top and bottom gates. But real challenge comes when the design to be fabricated at nano-scale i.e. 0 to 20 nm range. As at nano-scale regime, short channel effects (SCE) are more dominant, therefore a proper balance in selecting W/L ratio between $HfO_2 – SiO_2$ is essential.

## 2.3 Dual Gated (Single Metal / Dual Metal) Heterogeneous Dielectric with Graphene Layered Channel (0-2 nm width)

The earlier device models discussed in previous sections exhibit few limitations like limited SS swing and leakage current issue. To address these drawbacks, a carbon-based nanomaterial i.e. graphene is implanted as an ultra-thin nano-sheet of having 0-2 nm width over intrinsic channel. This nano-sheet is actually deployed as nano-ribbon in order to achieve better BTBT ratio. Our modified device models are showcased in Fig. 3.

As we can see at Fig. 4, that the energy band gap can actually be tuned according to the deployment of 2 nm thick graphene nano-ribbon at lower and upper

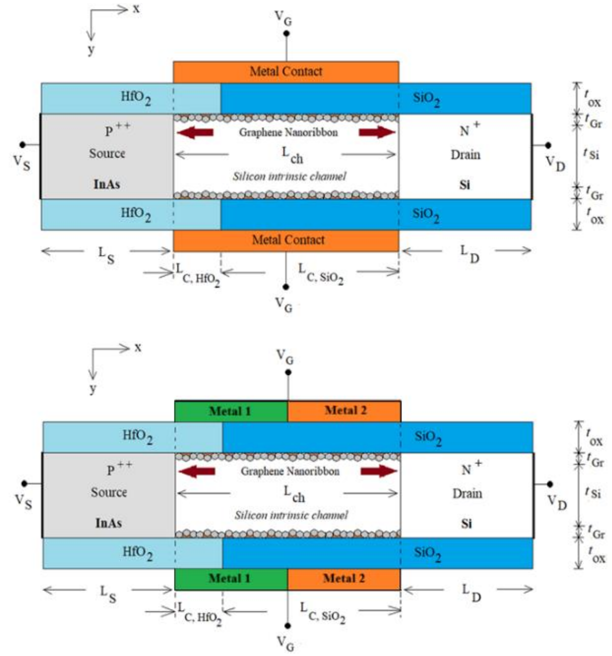


**Fig. 3** – Dual gated heterogeneous dielectric (a) single metal (DG-SM-He-GTFET) and (b) dual metal TFET with Graphene Layered Channel (DG-DM-He-GTFET)

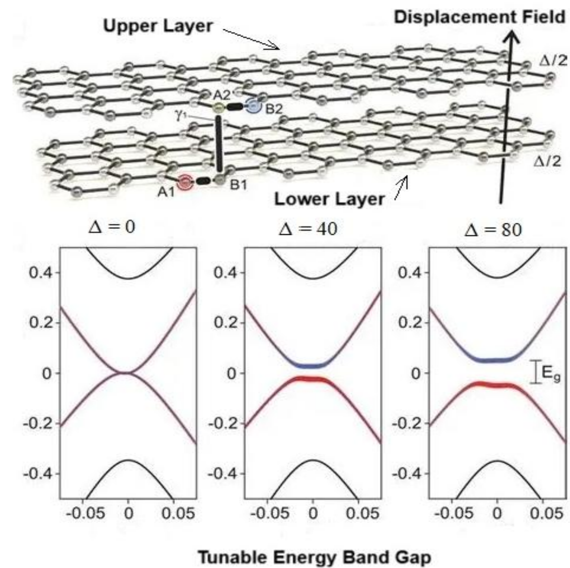


**Fig. 4** – Tunable Energy Band Gap created by Graphene Nanoribbon

layer of silicon channel. As we rotate the nano-sheet in order to use as nano-ribbon structure across the channel, the band gap also started getting reduced, and at time we see that the maxima and minima of valence and conduction bands meet together. This results considerable rise in BTBT which further draws turn ON voltage much quicker compared to any existing device models [12-15] in TFET family.

## 2.4 Physical and Electrical Parameters Used for our Proposed Model

The device modelling needs a proper balancing between the parameter selection both for physical and

electrical. Table 1 shows the typical device parameters that are considered for simulation work.

**Table 1** – Physical & electrical parameters used in this model

| Sl. No. | Physical & Electrical parameters | Unit(s) |
|---|---|---|
| 1. | Source Doping | $8.8 \times 10^{17}$ atoms/cm$^3$ |
| 2. | Drain Doping | $2.5 \times 10^{14}$ atoms/cm$^3$ |
| 3. | Channel Doping | $6 \times 10^{13}$ atoms/cm$^3$ |
| 4. | Channel Length (Gate: $L_{ch}$) | 0-20 nm |
| 5. | Thickness (Body: $t_{Si}$), (Oxide: $t_{ox}$) and (Graphene: $t_{Gr}$) | 10, 2 and 0.5 (nm) |
| 6. | Supply voltage ($V_{DD}$) | 0.5 V |

The length ($L$) and width ($W$) of any physical parameter play pivotal role in determining proper ON state / OFF state current. Table 1 displays the specific parameters used in our software models for simulation. Silvaco TCAD Version 1.8.27 is used for the simulation work.

## 3. SIMULATION RESULTS

Our paper mainly focuses on its low power application in terms of better device performance at nano-scale level. Therefore, following sub-sections describes the comparison analysis to establish our proposed work.

### 3.1 Better Drive Current ($I_{ON}$) and Sub-threshold Swing (SS)

Fig. 5 showcases the $I_D$ vs $V_G$ characteristics curve where $I_D$ is scaled at logarithmic scale. Here all four combinations of TFET model described earlier is examined at positive gate voltage keeping $V_{DS} = 0$ to 1 V and $V_{DD} = 0.5$ V. The highest drive current is recorded at $3.55 \times 10^{-6}$ A/μm offered by our proposed model i.e. DG-DM-He-GTFET. Major improvement in minimum sub-threshold swing (SS) is achieved at 33.07 mV/decade which is far less than traditional limit of 60 mV/decade.

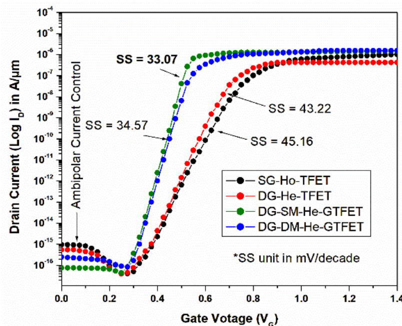


**Fig. 5** – $I_D$ vs $V_G$ characteristics

### 3.2 Ambipolar Current ($I_{OFF}$) Control

As we increase the forward gate bias the switching is triggered by the TFET models but the rise in ambipolar current i.e. $I_{OFF}$ also concern the modelling approach. Therefore, proper $W/L$ ratio need to be maintained at nano-scale level, which further results limited rise in ambipolar conduction. In Fig. 5 it is evident that device model using graphene nano-ribbon eventually helps to achieve this target. $2.16 \times 10^{-16}$ A/μm is recorded as minimum $I_{OFF}$ i.e. leakage or ambipolar current offered by DG-SM-He-TFET. Here proposed dual metal structure offers a little higher $I_{OFF}$ compared to single metal structure.

### 3.3 Electric Field Distribution

Fig. 6 clearly shows the contour plot of electric field distribution obtained by Silvaco TCAD. The maximum peak at source – gate junction is traced for our proposed DG-DM-He-GTFET device model at forward bias. The top and bottom gate actively involved in better BTBT tunnelling across the junction. The black color vertical solid line is marked where maximum BTBT tunnelling is occurring (Source – Gate Junction) for our proposed model.

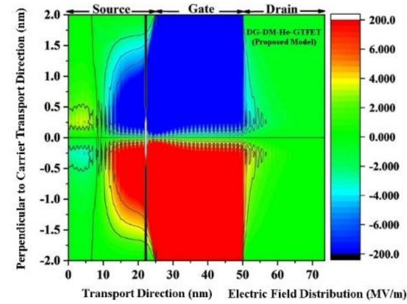


**Fig. 6** – Electric field distribution analysis

### 3.4 Switching Ratio with Respect to Channel Length (0-25 nm) in Nano-Scale

As we have witnessed a sudden spike in surface potential in lateral direction across the channel shown above in Fig. 6, this proposed device model can be suitable for fast switching at minimum Turn ON voltage i.e. below 0.3 V. To establish this point, we further analyzed the $I_{ON}/I_{OFF}$ switching ratio for proposed model (DG-DM-He-GTFET) with respect to varied intrinsic channel length at nano-scale i.e. 0 nm to 25 nm.

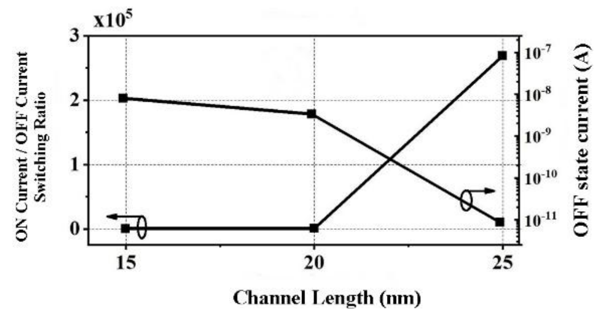


**Fig. 7** – Switching Ratio and OFF state current analysis w.r.t. varied channel length (0-25 nm)

Fig. 7 clearly depicts the sharp rise in the $I_{ON}/I_{OFF}$ switching ratio as the channel length gets shorten from 25 nm to 20 nm range. Further reduction in channel length results gradual rise in switching ratio, but limited due to rise in leakage current i.e. $I_{OFF}$.

### 3.5 BTBT and Electric Field Comparison Analysis

As our paper mainly focuses on deployment of carbon-based nano-material i.e. graphene over entire 0-20 nm length intrinsic channel, therefore the quantum tunnelling (BTBT) comparison is a must task for researchers. Secondly along with variation in BTBT, along *X*-axis the changes in electric field are also observed considerably. To showcase these crucial comparison analysis, Fig. 8 demonstrates a bar-graph comparison, where it is clearly evident that the BTBT rate is largely visible ($8.34 \times 10^{28}$) for our proposed device model i.e. DG-DM-He-GTFET, so as the electric field ($1.12 \times 10^{8}$). The comparison is taken at very low supply voltage of 0.5 V ($V_{DD}$) keeping $V_G$ ranging between 0 to 1.5 V.

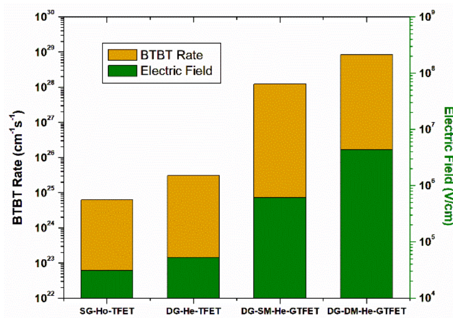


**Fig. 8** – Tunneling rate and *E*-field comparison

## 4. CONCLUSION AND FUTURE SCOPE

This research work mainly focuses on different homo and hetero structures of existing tunnel FET devices along with our proposed modified device model, in order to achieve better device performance at nano-scale infrastructure. In today's modern VLSI technology, practical layout build-up and step by step IC (Integrated Circuit) fabrication at such nano-scale is a real challenge for all of us. Keeping this in mind, we approached simple hetero-structure model with single and dual metal contacts along with 0-2 nm thick graphene nanomaterial placed over channel.

Better drive current ($I_{ON}$) is achieved at $3.55 \times 10^{-6}$ A/μm with minimum leakage current ($I_{OFF}$) of $2.16 \times 10^{-16}$ A/μm at 0.5 supply voltage ($V_{DD}$). Minimum sub-threshold swing (SS) is achieved at 33.07 mV/decade which is far less than traditional limit of 60 mV/decade. This results better and fast switching as digital switch as well as low power applications.

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# Використання затворів та каналів у графеновому тунельному польовому транзистори (GTFET) у наномасштабі для покращення продуктивності пристроїв

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Ця робота зосереджена на різних інженерних схемах затворів та каналів, виконаних на типових тунельних польових транзисторах (TFET) у наномасштабі. У цій дослідницькій роботі продемонстровано покрокову розробку типової моделі TFET на нанопристрої з метою покращення продуктивності пристрою. Спочатку як оксидний матеріал використовується однозатворний гомогенний діелектрик, тобто $SiO_2$, який потім модифікується до двозатворного гетерогенного діелектрика, тобто комбінації $HfO_2$ – $SiO_2$, з метою покращення струму керування ($I_{ON}$) та коефіцієнта перемикання ($I_{ON}/I_{OFF}$). Під час моделювання цього процесу власний канал розвивається як гетерогенний (InAs-Si) протягом усього моделювання. Це призводить до значних змін розподілу поверхневого потенціалу вздовж каналу через ефект міжзонного тунелювання (BTBT). По-друге, цей двозатворний гетерогенний діелектричний TFET модифікується тонким шаром графену товщиною 0-2 нм, розгорнутим поверх власного каналу. Цей наномасштабний шар графену введено як нанострічкову архітектуру, щоб зменшити ширину забороненої зони, що налаштовується. Це пришвидшує тунелювання BTBT через перехід і приводить до значно ранішого виникнення напруги ввімкнення ($V_{ON}$), що призводить до швидкого цифрового перемикання. Нарешті, ця структура TFET додатково оновлена за допомогою подвійної металевої, подвійної затворної структури для дослідження її співвідношення $I_{ON}/I_{OFF}$ та контролю струму витоку. Для створення всіх пов'язаних симуляційних робіт використовується Silvaco TCAD. Кращий струм керування ($I_{ON}$) досягається при $3,55 \times 10^{-6}$ А/мм з мінімальним струмом витоку ($I_{OFF}$) $2,16 \times 10^{-16}$ А/мм при напрузі живлення 0,5 ($V_{DD}$) з мінімальним підпороговим розмахом (SS) 33,07 мВ/декаду.

**Ключові слова**: GTFET, TCAD, Нанострічка, Квантове тунелювання.