Journal of Nano- and Electronic Physics
Vol. **18** No 1, 01020(5pp) (2026)

Журнал нано- та електронної фізики
Том **18** № 1, 01020(5cc) (2026)

REGULAR ARTICLE

Design and Analysis of an Energy-Efficient Voltage Level Shifter for Low-Power Applications

Pulyala Vasundhara*, V. Shankar†

Department of Electronics and Communication Engineering, G. Narayanamma Institute of Technology and Science (For Women) Shaikpet, 500104 Hyderabad, India

(Received 10 December 2025; revised manuscript received 15 February 2026; published online 25 February 2026)

This describes a low-energy voltage level shifter (LS) architecture. We further introduce a regulated cross-coupled (RCC) pull-up network to achieve a considerable reduction in dynamic power consumption with higher switching speed. The suggested LS can switch very low voltage signals below the input MOS device threshold up to the nominal supply voltage. A fast and very low power voltage level shifter (LS) is presented. By using a new regulated cross coupled (RCC) pull-up network, the switching speed is boosted and the dynamic power consumption is highly reduced. The proposed LS has the ability to convert input signals with voltage levels much lower than the threshold voltage of an MOS device to higher nominal supply voltage levels. The presented LS occupies a small silicon area owing to its very low number of elements and is ultra-low-power, making it suitable for low-power applications such as implantable medical devices and wireless sensor networks. Results of the post-layout simulation in a standard CMOS technology This LS is particularly appealing for low-power application fields, including implanted medical devices and wireless sensor networks, as it makes very little use of components and dissipation has been minimized. Benefiting from the use of sub-1V CMOS technology, it can convert as low input voltage level as 80 mV according to the post-layout simulation results. This LS gives the power dissipation of 123.1 nW with 23.7 ns propagation delay at supply voltages of 0.4/1.8 V (Low/High) and of input frequency of 1 MHz.

Keywords: Dual-supply, Level shifter, Differential cascade Voltage switch (DCVS), Subthreshold circuit, Low-power.

DOI: 10.21272/jnep.18(1).01020 PACS numbers: 84.30.Jc

1. INTRODUCTION

In low-power and energy-efficient digital and mixed-mode circuits, supply voltage reduction decreases circuit dynamic power and short-circuit currents. However, reducing the supply voltage is detrimental to the efficiency and the speed of analog circuits. For systems that have a range of speeds across the circuit blocks, multiple or dual supply voltages can help alleviate this problem. This approach is widely applied in low-data-rate applications, including wireless sensor networks, small medical devices, and environmental monitoring systems. In multi-voltage applications, the signal levels need to be level shifter and aligned appropriately for interfacing between sub-blocks. This requires a level shifter (LS) to transfer low logic levels (sub-threshold voltage signals) to higher values on logic levels that can be used in subsequent stages. As LS circuits are commonly used in different systems, one of the important task of designing such a circuit is to reduce the power consumption, propagation delay and silicon area.

Voltage level shifters (VLS) are essential components in integrated circuits (ICs) that facilitate communication between the interlinked sub-circuits operating at various voltage levels, especially suitable for low-power applications like system-on-chip (SoC) designs and microcontrollers. Standard level shifters work, yet frequently they have high power utilization, slower exchanging paces, and affected activity at low supply voltages.

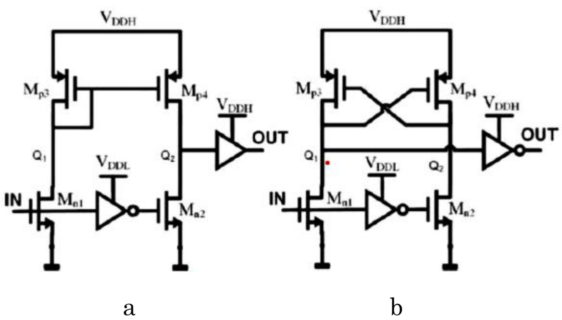

Fig. 1 – Two types of conventional level shifters, (a) current mirror (CM) based archirecture, (b) differential cascode voltage switch (DCVS) architecture [1]

This work presents a new voltage level shifter (VLS) design that employs a regulated cross-coupled pull-up (RCCPU) which optimizes the trade-off between

* vasundarareddy156@gmail.com
† vshankar33@gnits.ac.in

improved switching performance and reduced static power dissipation. The architecture is designed to operate robustly at low supply voltage [1] and is ideal for modern low-power systems.

Through drastic reductions in delay, improved robustness, and increased energy efficiency, this design provides greater both power efficiency and operational velocity than conventional approaches. This research presents comparative analysis that proves the effectiveness of the RCCPU-based level shifter in influencing low power demand and high working speed in state-of-the-art integrated circuit designs due to the extent of enhanced performance achieved.

2. LITERATURE REVIEW

The simplest CM type (Fig. 1a) which has a low speed, high static power of one branch, and no regenerative behavior between pull-up and pull-down networks. In contrast, the DCVS design (Fig. 1b) provides an equivalent cross-coupled pull-up network for defining high-speed switching behaviour through a regenerative mechanism. For DCVS systems, however, as long as the supply (e.g., VDD brings the supply) voltages are below the nominal threshold voltage, the pull-down transistors are less than (pull up transistors thus degrade performance.

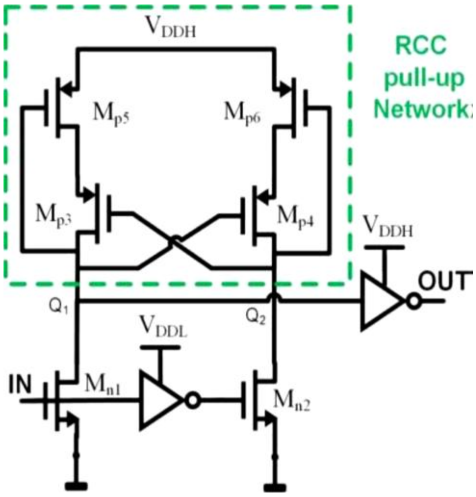

Fig. 2 – Simplified schematic of the proposed level shifter

Hence, we need to increase the pull-down transistor size, which pulls up the pull-down network at the expense of reduced overall efficiency towards increased delay and power.

Several LS topologies have been proposed in previous studies to get beyond the limitations of the traditional LSs that operate in the subthreshold range. [3] through [8] make advantage of the CM-based architecture. The design proposed in [3] uses a level shifting capacitor which is often recharged to differences in VDDH and VDDL voltages to minimize low-to-high transition latency. The conversion speed can be improved with an extra circuit in the pull-down device, and an optimized pull-up device current during the pull-down of the output node [4]. The LS in [5], also aimed to increase a voltage conversion range, has been based on a hybrid structure of modified Wilson current mirrors and standard CMOS logic gates. The circuits in 6] utilize a self-controlled current limiter to minimize static power consumption.

The levels of output are achieved by the design of [7] that makes use of two stage standard comparator. The topologies in [9-13] are based on the DCVS design [1]. Limiting their currents has been attempted in [9] and [12] to lessen the pull-up device's power. In order to decrease dynamic power and improve speed, we employed a split-input inverting buffer and a self-adjusting pull-up network [10]. However, to increase the circuit delay, works [11] and [13] adopt the multi-threshold CMOS technics which used the three types of different threshold voltage.

Voltage level shifters (VLS) are essential in mixed-signal integrated circuits, facilitating communication between different voltage domains as modern electronic systems operate at varying supply voltages. By employing a differential transistor pair, the DCVS level shifter enhances switching speed, lowers static power dissipation, and provides improved noise immunity over traditional CMOS implementations. At ultra-low supply voltages, however, its performance deteriorates because of the differential pair's limits. In order to overcome these obstacles, the RCCPU level shifter combines adaptive and conventional design concepts, using a control circuit to dynamically modify pull-up strength for increased effectiveness. A major issue is still power consumption, especially for battery-operated devices where traditional CMOS shifters have a high static power dissipation. A potential option for contemporary low-power applications, RCCPU further maximizes energy economy and performance while DCVS minimizes static current flow to reduce power consumption.

3. PROPOSED LEVEL SHIFTER

These features in the new level shifter (LS) involve adding an RCC pair in the pull-up network and using a modified DCVS topology that improves switching speed and lowers dynamic power consumption. When transitioning from low to high, the LS operates across three stages. At the first point, transistors Mp4 and Mp5 are off, and Mp3 and Mp6 remain in the on state. Q1 is at VH and Q2 is at Vlow at this point.

As the input goes from low to high, Mn1 gets turned on while Mn2 gets turned off and Q1 gets discharged quickly with the weak pull-up current. As Q1 approaches VDDH−Vth, Mp4 and Mp5 activate, causing Q2 to rise quickly and turning off Mp3 and Mp6, thereby maintaining Q2 at VH while reducing dynamic power. The pull-up network is not turned off completely, it goes into deep subthreshold so that state change happens faster which benefits speed. At the final step, when Mp3 turns off, Mn1 further lowers Q1's voltage, ensuring no static current flows. This RCC-based design significantly reduces power dissipation and transition times. Voltage level shifting is a critical requirement in multi-power-supply systems like wireless sensor networks, medical devices, environmental monitoring systems, etc., where multiple blocks are active at totally different voltages. Efficient LS designs must optimize power consumption, propagation delay, and silicon area, as these systems often require numerous LSs to ensure proper signal interconnection across voltage domains.

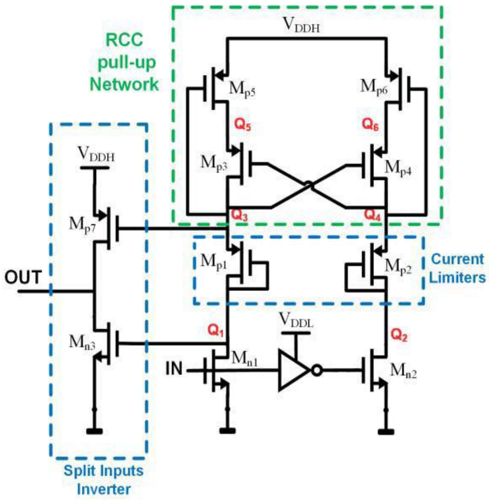

Fig. 4 – Circuit of the complete proposed level shifter

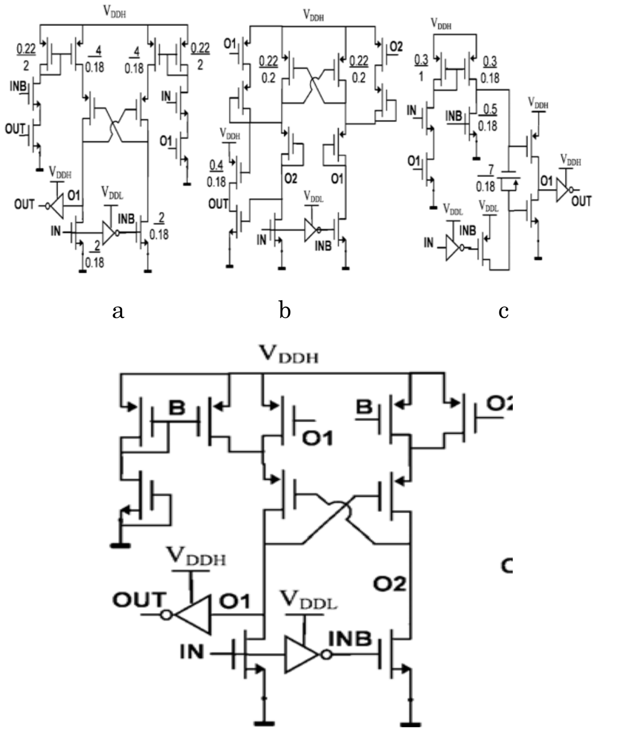

Fig. 5 – (a) Voltage level shifter, (b) Ultralow-Voltage Energy-Efficient Level Shifter (c) limited-contention cross-coupled level shifter reported Al other remaining transistors are minimum sized

Compared with the conventional DCVS topology, the proposed LS with a RCC pull-up network consumes[1] lower supply current and achieves nearly 3 times lower time delay than conventional LS structure. The LS may function faster and draw significantly less current from the supply voltage (VDDH) thanks to the RCC. Pull-up network in 0.6 V (VDDL) and 1.8 V (VDDH) simulations where the minimum transistor size for both configurations is identical. The complete circuit diagram of the proposed LS [1] is illustrated in Fig. 4. To achieve lower power consumption, the pull-down network is arranged in series with two *p*-MOS diodes [8]. Also, a split-inputs inverter is used to reduce the output inverters short-circuit current[1] through the transit [7].

A voltage differential between nodes Q1 and Q3 is produced in the suggested level shifter (LS) architecture by *p*-MOS diodes (Mp1 and Mp2) raising the voltages at nodes Q3 and Q4 above zero. This distinction, however, decreases the short-circuit current and prevents the pull-up (Mn3) and pull-down (Mp7) transistors in the output inverter [1] from switching on simultaneously.

4. SIMULATION DESIGNS AND RESULTS

Conventional level shifters translate signals between different voltage domains in electronic circuits. A common type, the current mirror-based level shifter, operates by replicating a current from one circuit branch to another. The input signal from a low-voltage domain is applied to the gate of the input transistor, which controls a current mirrored by the output transistor, thereby shifting the voltage level.

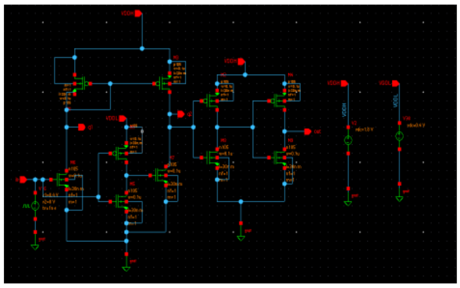

Fig. 6 – Circuit diagram current mirror

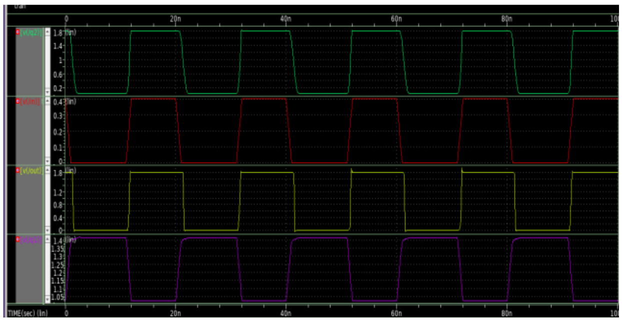

Fig. 7 – Output waveform of current mirror

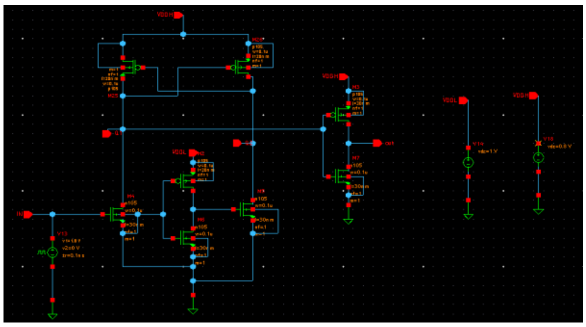

Fig. 8 – Circuit diagram differential cascode voltage switch (DCVS) architecture

A dynamic logic architecture frequently seen in high-performance digital circuits, especially in Very Large Scale Integration (VLSI) designs, is the DCVS.

The proposed level shifter is intended to provide better performance in terms of speed, power consumption, footprint and reliable function over a wide voltage range.

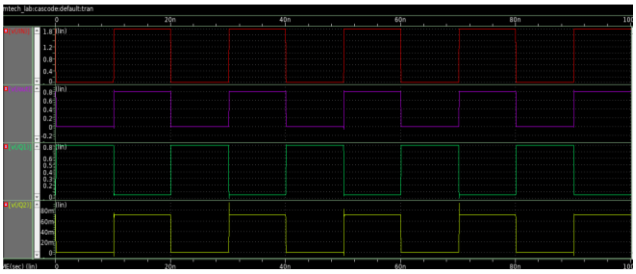

Fig. 9 – Output waveform of differential cascode voltage switch (DCVS) architecture

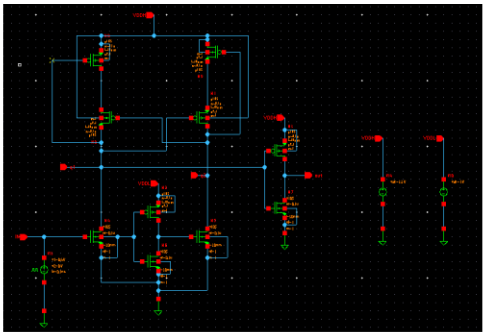

Fig. 10 – Circuit diagram is Simplified of the proposed level shifter

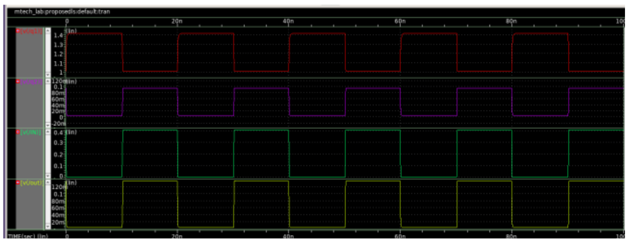

Fig. 11 – Output waveform of Simplified schematic of the proposed level shifter

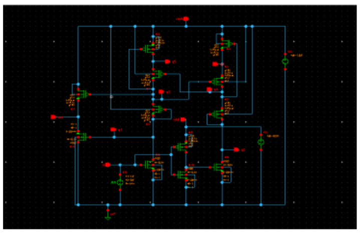

Fig. 12 – Circuit diagram of the complete proposed level shifter

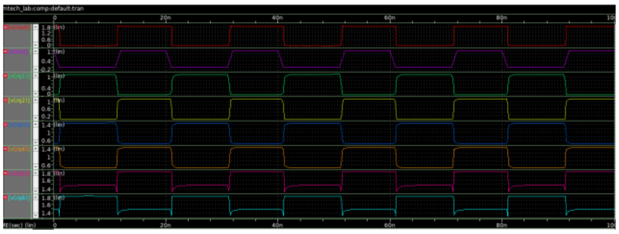

Fig. 13 – Output Waveform of the complete proposed level shifter

Table 1 – Comparison table with voltage level shifter

Design Name	Rise Time (ns)	Fall Time (ns)	Delay (ns)	Power (μ)
CM	21.8	0.0912	19.7	8.91
DCVS	20	0.0155	9.32	7.03
Proposed (LS)	93.5	0.555	0.0935	4.50
VLS	9.92	10.1	10.1	8.91

The purpose of this suggested level shifter is to close the voltage differential between the high-voltage and low-voltage domains in contemporary electronic circuits their slow speed, excessive power consumption, and inefficiency across a broad voltage range.

5. CONCLUSION

The cross-coupled regulated pull-up-based level shifter proposed here achieves low power, delay and area overhead by ensuring minimum input signal swings when transitioning from deep subthreshold voltages to high supply and nominal supply voltage levels. Post-layout simulations in 45 μm. CMOS technology shows that it can translate input signals from a mere 80 mV to 1.8 V with the minimum power-delay product. Although the regulated design introduces some complexity and power overhead, it significantly enhances power efficiency, switching speed, and robustness, making it ideal for power-sensitive applications like portable devices, microprocessors, and SoCs. This approach effectively balances trade-offs between speed, power, and reliability, offering an optimal solution for next-generation semiconductor designs as power management and system complexity continue to evolve.

REFERENCES

1. S. Kabirpour, M. Jalali, *IEEE Trans. Circ. Systems II: Express Briefs* **66** No 6, 909 (2019).
2. M. Alioto, *IEEE Trans. Circuits Syst. I, Reg. Papers* **59** No 1, 3 (2012).
3. E. Maghsoudloo, M. Rezaei, M. Sawan, B. Gosselin, *IEEE Trans. Circuits Syst. I, Reg. Papers* **64** No 5, 1164 (2017).
4. S.R. Hosseini, M. Saberi, R. Lotfi, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **25** No 3, 1154 (2017).
5. S.-C. Luo, C.-J. Huang, Y.-H. Chu, *IEEE Trans. Circuits Syst. I, Reg. Papers* **61** No 6, 1656 (2014).
6. R. Lotfi, M. Saberi, S.R. Hosseini, A.R. Ahmadi-Mehr, R.B. Staszewski, *IEEE Solid-State Circ. Lett.* **1** No 2, 34 (2018).
7. Y. Osaki, T. Hirose, N. Kuroki, M. Numa, *IEEE J. Solid-State Circ.* **47** No 7, 1776 (2012).
8. L. Wen, X. Cheng, S. Tian, H. Wen, X. Zeng, *IEEE Trans. Circ. Syst. II, Exp. Briefs* **63** No 4, 346 (2016).
9. S.R. Hosseini, M. Saberi, R. Lotfi, *IEEE Trans. Circ. Syst. II, Exp. Briefs* **61** No 10, 753 (2014).
10. M. Lanuzza et al., *IEEE Trans. Circuits Syst. II, Exp. Briefs* **64** No 1, 61 (2017).
11. M. Lanuzza, P. Corsonello, S. Perri, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **23** No 2, 388 (2015).
12. C.-R. Huang, L.-Y. Chiou, *Proc. SoC Design Conf. (ISOCC)*, 142 (2014).
13. M. Lanuzza, P. Corsonello, S. Perri, *IEEE Trans. Circ. Syst. II, Exp. Briefs* **59** No 12, 922 (2012).

Розробка та аналіз енергоефективного перемикача рівнів напруги для низькопотужних застосувань

Pulyala Vasundhara, V. Shankar

Department of Electronics and Communication Engineering, G. Narayanamma Institute of Technology and Science (For Women) Shaikpet, 500104 Hyderabad, India

У цій статті описано архітектуру зсуву рівнів напруги (LS) з низьким енергоспоживанням. Далі ми представляємо регульовану перехресно зв'язану (RCC) підтягувальну мережу для досягнення значного зниження динамічного споживання енергії з вищою швидкістю перемикання. Запропонований LS може перемикати сигнали дуже низької напруги нижче порогу вхідного МОН-транзистора аж до номінальної напруги живлення. Представлено швидкий та дуже низькопотужний зсув рівнів напруги (LS). Завдяки використанню нової регульованої перехресно зв'язаної (RCC) підтягувальної мережі, швидкість перемикання підвищується, а динамічне споживання енергії значно знижується. Запропонований LS має здатність перетворювати вхідні сигнали з рівнями напруги, значно нижчими за порогову напругу МОН-транзистора, на вищі номінальні рівні напруги живлення. Представлений LS займає невелику площу кремнію завдяки дуже малій кількості елементів та є наднизькоенергетичним, що робить його придатним для застосувань з низьким енергоспоживанням, таких як імплантовані медичні пристрої та бездротові сенсорні мережі. Результати моделювання після розмітки за стандартною КМОП-технологією. Цей LS особливо привабливий для застосувань з низьким енергоспоживанням, включаючи імплантовані медичні пристрої та бездротові сенсорні мережі, оскільки він використовує дуже мало компонентів, а розсіювання енергії мінімізовано. Завдяки використанню КМОП-технології з напругою менше 1 В, він може перетворювати вхідну напругу на низький рівень до 80 мВ, згідно з результатами моделювання після розмітки. Цей LS забезпечує розсіювання потужності 123,1 нВт із затримкою поширення 23,7 нс при напрузі живлення 0,4/1,8 В (низька/висока) та вхідній частоті 1 МГц.

Ключові слова: Подвійне живлення, Зсув рівнів, Диференціальний каскадний перемикач напруги (DCVS), Підпорогова схема, Малопорогове живлення.