



REGULAR ARTICLE

Development of Compact, Low-Power CMOS Toggle Flip-Flops for High-Speed Applications

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A New True single-phase clock transistor using T flipflop (TSPC-T) is introduced to operate efficiently at low supply voltages (VDD) while ensuring high speed and reliability. T Flip-flop significantly minimizes unnecessary power consumption by disabling clock signals when they are unnecessary. The present flip-flop design has two different designs, i.e., Static Toggle Flip-Flop (STFF) design and Modified Clocked CMOS design (M-C<sup>2</sup>MOS). STFF is used to reduce the power consumption, by 0.08412  $\mu$ W, which is energy-efficient and better than designs like S<sup>2</sup>CFF (0.11621  $\mu$ W) and TGFF (0.1736  $\mu$ W), whereas M-C<sup>2</sup>MOS is used to minimize the PDP by (0.7746 fJ), outperforming existing designs like TGFF (3.0537 fJ) and S<sup>2</sup>CFF (1.0214 fJ). It reduces redundant transitions in the circuit while enhancing overall energy efficiency. Additionally, updating the flip-flop operation lowers the required devices and decreases power usage. In the present work, a comparative analysis of five existing flip-flop designs (TGFF, C<sup>2</sup>MOS, S<sup>2</sup>CFF, 18TSPC, 18TSPC\_T) and the proposed design (STFF, M-C<sup>2</sup>MOS) is made. The proposed design (STFF, M-C<sup>2</sup>MOS) has better power and delay when compared to existing high-speed flip-flops. The design and analysis are carried out by using 32 nm CMOS technology. Simulation results demonstrate that the STFF design significantly improves energy efficiency, with a 10.3% reduction in power consumption at 1 V. These results highlight the importance of STFF and M-C<sup>2</sup>MOS in optimizing both power and speed, making them highly effective for modern low-power, high-performance digital applications.

**Keywords:** Low-power, High performance, Delay reduction, Flip-flops.

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1. INTRODUCTION

The area, power, and speed were the primary goals in a VLSI circuit design. Modern high-speed ICs are highly dependent on the use of high-performance flip-flops. The most promising power minimization method is the reduction of VDD because of the strong quadratic dependence of dynamic power from VDD in VLSI circuits. In the paper, we are using edge-triggered flip-flop [1].

Flip-flops and latches are the fundamental components on which digital circuits rely when making changes in storage and synchronizing data [2]. Flip-flop design demands high performance to maintain the timing of the crucial circuit, which directly contributes to the speed of system operation. Thousands to millions of flip-flops or latches may be present in a high-performance system, which also means it can easily account for significant power consumption on an overall chip. As the circuit transitions increase, the circuit consumes more power [2, 3]. The minimization of power and delay has to be balanced, which is a big task for high-speed designs.

The TGFF is a fundamental circuit mainly used in synchronous circuits, which operates on the master-slave concept in Fig. 1. Master-slave flipflop (MSFF) [4, 5], has

two latches, master and slave latch, which hold the previous value for one clock period. Only one latch works, i.e., either master or slave, which will be determined by a clock signal. The concept is that when the clock is low, the master latch will be in the ON state and start sampling [5]. Then, the slave latch holds previous data when the clock is high; the slave latch will be in the ON state, and the master will be in the hold state [5]. In TGFF, one latch will be active at every clock cycle, which incurs more power consumption, circuit area, and delay. The major drawbacks of TGFF are more clock-Q delay and increased power consumption [6].

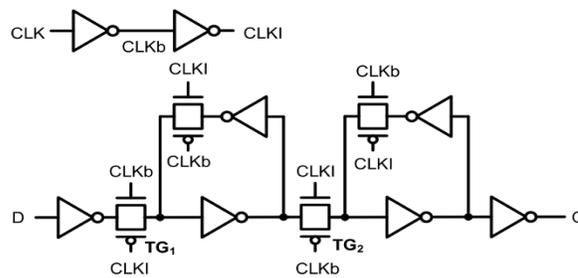


Fig. 1 – Transmission gate-based flip-flop

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**2. EXISTING FLIP-FLOP DESIGNS**

To overcome the issues of TGFF, a Clocked CMOS circuit is designed. In the Clocked CMOS circuit, dynamic logic is used to synchronize the logic circuit with the clock signal. It supports dual clock-controlled transistor configuration, where the Clocked NMOS and Clocked PMOS configurations [5, 7]. At the master stage, PMOS is controlled by a Clocked PMOS signal, and Clocked NMOS is controlled by the inverse of the Clocked signal. C2MOS circuit changes its state during specific phases of the clock signal that are controlled dynamically, which reduces the redundant transitions and average power consumption. The circuit diagram is illustrated in Fig. 2. To overcome the issues of clocked CMOS circuit delay.

The “18 TSPC (True Single-Phase Clock) Flip-Flop is a dynamic logic circuit” used predominantly in high-speed and low-power applications [9, 10]. The “18T” denotes its implementation in 18 transistors. TSPC is a design methodology for digital circuits, specifically in implementing flip-flops and other sequential logic, wherein a single clock signal steers the whole circuit. The sequential function of this flip-flop is realized using a dynamic latch that eliminates the need for complementary clock signals. Almost all of the TSPC-flip-flop-enhanced designs studied in the literature use complementary or inverted clock pulse configurations for master-slave triggering on various digital and computation circuits.

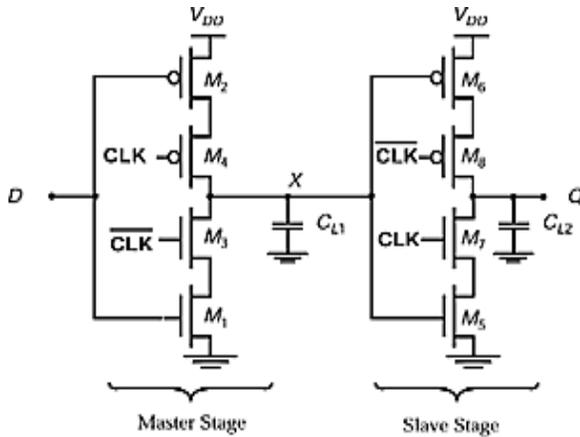


Fig. 2 – Circuit diagram of C2MOS [7]

Dynamic TSPCL (True Single-Phase Clock Logic) flip-flops have been developed for area and power saving. These designs are compact for the low transistor count, while the reduction in internal switching at some nodes increases their efficiency substantially. Edge-triggered D flip-flop, a key part of TSPC designs, alternates with n-blocks and p-blocks driven from the same clock signal [9, 10]. In the evaluation phase, input data is active and being evaluated and propagated; in the precharge phase, the circuit is prepared for the next evaluation phase [10] by pre-charging some nodes to known voltages. In turn, the global clock system avoids synchronization and integrates

design complexity. Positive-edge-triggered TSPC flip-flops, for instance, isolate the input from the output while the clock signal is LOW, then latch input data to output at a LOW-to-HIGH clock transition, whereas timing small capacitance helps in blocking static latch.

Designing a new flip-flop design using T flip-flop. By incorporating the “18 TSPC using T flip-flop” [10], once a triggering local clock edge always results in a flip-flop output toggling as described above, “not using a DFF but using a toggle flip-flop (TFF)” is enough [12]. As is well known, a “TFF can be easily implemented from a DFF” by simply using an inverted output to its input [10]. The operation of 18 TSPC using T flip-flop is when the clock is changing transitions from 0 to 1, 1 to 0, and the output Q is toggling [11]. During clock low, the output Q is in the previous state, i.e., high or low. When the clock is high, the output Q toggles from high too low for edge-triggered flip-flops, and when the clock is low, the Q toggles from low to high, respectively as illustrated in Fig. 3.

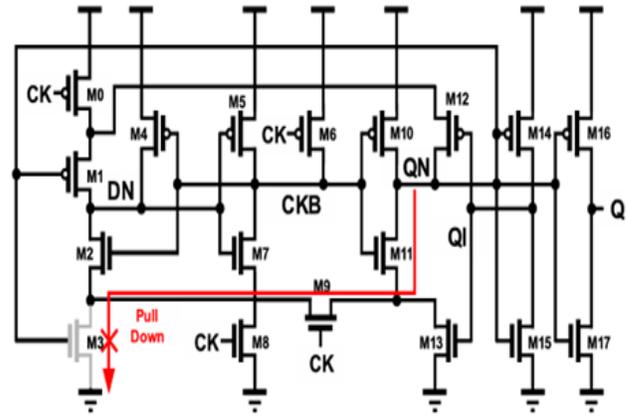


Fig. 3 – Circuit diagram of 18 TSPC\_T [10]

The major drawbacks of 18TSPC are increased power consumption and delay of the circuit compared to the clocked CMOS circuit, as 18TSPC design does not support direct connections between input and output, which could contribute to increased propagation delay leading to suboptimal flip-flop performance in high-speed operations [11].

**3. PROPOSED FLIP-FLOP DESIGN**

**3.1 Static Toggle Flip-Flop Design**

To overcome the limitations of the 18TSPC flip-flop, the “Static Toggle Flip-Flop (STFF)” and “Modified C<sup>2</sup>MOS Flip-Flop (M-C<sup>2</sup>MOS)” [12] designs are introduced, where the operation can be made with the efficient use of a single signal. The 16-transistor Static Toggle Flip-Flop (16STFF) configuration is shown in Fig. 4(a). Here, the primary driver transistors-M0 to M3, M6 to M8, and M10, M11, M14, M15-are responsible for data transfer, while keeper transistors-M4, M5, M9, M12, and M13-maintain data stability [12]. Toggle action is achieved by controlling the main drivers through the

clock signal (CK). In keeping with enhanced stability, the gate input of M13 is made to follow Q instead of DN. This ensures stability during clock transitions [12].

The operation of 16 STFF is as follows: When CK goes low while QN is pulled high by the M12 transistor, DN is pulled low by the M3 transistor, and the output Q will be 0. When CK is high, M8 and M11 are turned ON letting the slave stage active, and “master is in the hold state, the output at the master stage is transferred to the output Q”, when CK is rising, the output node QN is pulled low by M11 transistor, and the output Q will be 1. Moreover, the STFF design overcomes unnecessary dynamic power consumption due to redundant transitions, especially under high switching activities. Contentions are eliminated through optimized transistor sizing; hence, charge sharing and signal degradation problems are alleviated, ensuring reliable operation even under lower supply voltage conditions [12]. The output waveforms are illustrated in Fig. 4(b).

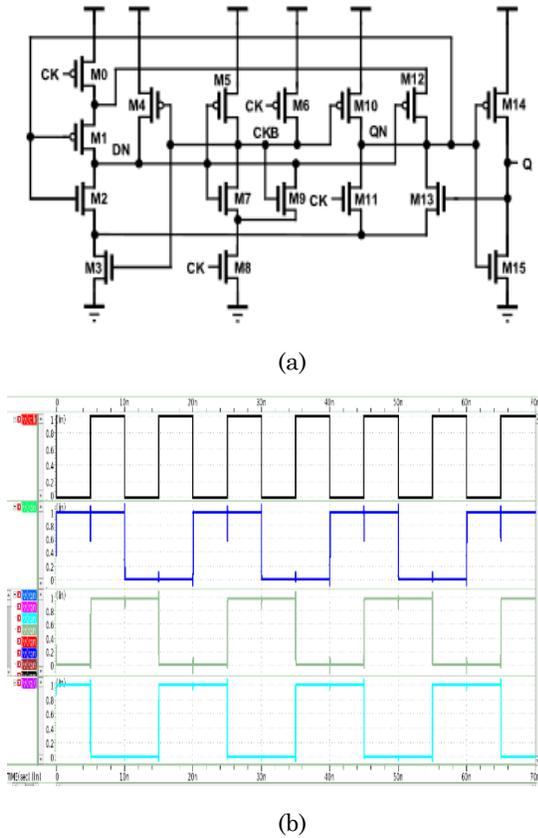


Fig. 4 – (a) Circuit diagram of STFF, (b) Output waveforms of STFF [12]

3.2 Modified C<sup>2</sup>MOS Flip-Flop Design

The design of M-C<sup>2</sup>MOS is equally applicable to the C<sup>2</sup>MOS The design of M-C<sup>2</sup>MOS is equally applicable to the C<sup>2</sup>MOS flip-flop. This transistor count is increased by three by integrating transistors M6 and M9, as shown in Fig. 5. Similar to the 16STFF, the M-C<sup>2</sup>MOS flip-flop contains “primary drivers (M0-M3, M6-M9, M14, M15)

[12] and keeper transistors (I0, I1, M4, M5, M10-M13) [6]”. Internal clock signals CKB and CKD are generated using inverters I2 and I3, respectively [12].

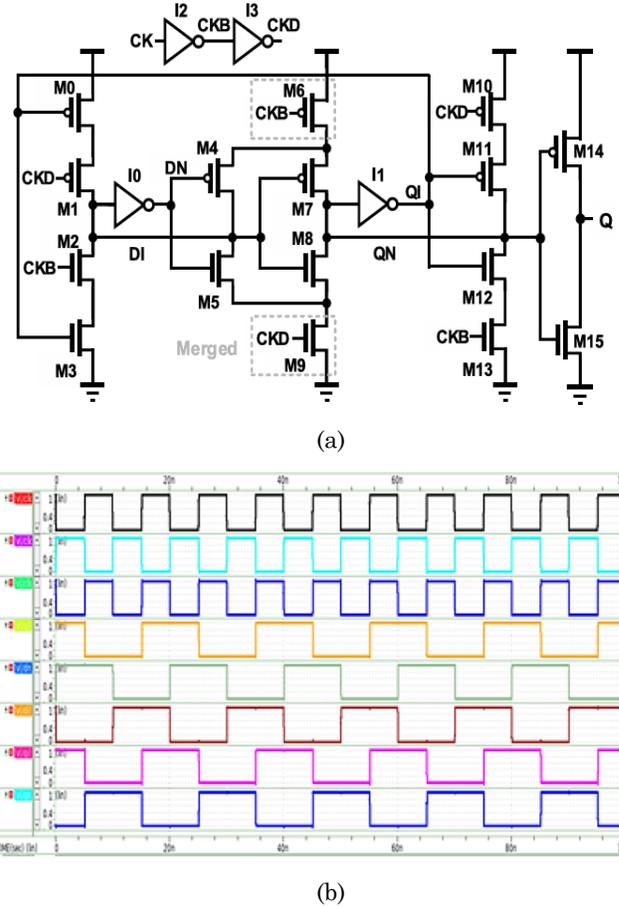


Fig.5 – (a) circuit diagram of M-C<sup>2</sup>MOS, (b) output waveforms of M-C<sup>2</sup>MOS

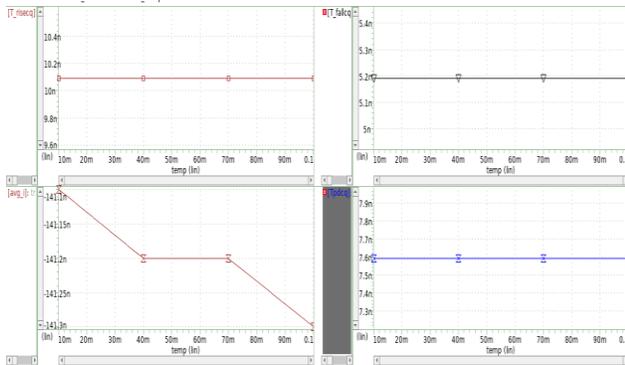
When the clock signal is low, the master stage driver M0-M3 routes the output QI to DI, and the slave stage keeper I1, M10-M13 sustains the output QN with M6 and M9 deactivated. When CK transitions to a high state, the slave stage is turned on, allowing the slave stage main driver M6- M9 [12] to toggle the output. The master stage keeper (I0, M4, M5) takes care of state preservation of DI during the whole operation [12]. The circuit diagram and output waveforms are demonstrated in Fig. 5(b).

4. SIMULATION RESULTS

By analyzing the implementation of various flip-flops that are summarized in Table 1. From Table 1, we have seen that in the case of TGFF, high-power consumption arises as compared to S<sup>2</sup>CFF [5, 6]. There is a special variation of these optimized designs among which STFF and M-C<sup>2</sup>MOS reported the smallest values of Power-Delay Product, as 0.6327 fJ and 0.7746 fJ, respectively. Therefore, these designs should balance power consumption and speed so that STFF is the most efficient

due to its compact architecture and reduced Clock-Q delay. The 18TSPC\_T design well performed with the PDP at 0.6941 fJ by capitalizing on the high speed combined with moderate power consumption. TGFF stands out by offering the largest value of PDP, with a value of 3.0537 fJ, to correspond to the very slow speeds and higher powers that it employs.

The Clock-Q delay is mainly minimized in 18TSPC using T flip-flop design due to optimized toggle-based design, efficient usage of the transistors, and minimization of critical path delay. The 18TSPC\_T is designed as a toggle flip-flop that eliminates the possibility of redundant toggling operations from it compared to 18TSPC\_D, S<sup>2</sup>CFF. The use of static logic has reduced power consumption in the proposed flip-flop design (16STFF), which decreases the leakage power of the circuit, hence reducing power consumption. STFF uses only one clock signal; hence, redundant transitions are reduced compared to all other designs of flip-flops. The C<sup>2</sup>MOS design is compact in terms of transistor count with just 8, but has the highest delay, 10.75 ns, as compared to STFF and M-C<sup>2</sup>MOS; however, it makes up for the lowest power consumption, which is 0.07051  $\mu$ W. Therefore, this is very much suited for ultra-low-power environments. On the other hand, TGFF and 18TSPC\_D have much higher delays of 17.59 ns and 17.57 ns, respectively, which, along with their increased power requirements, render them less suited for performance-sensitive environments.



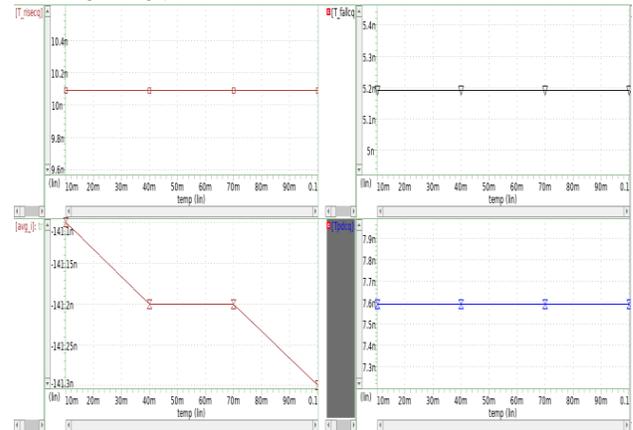
**Fig. 6** – Sweep analysis of STFF

The rise and fall times further confirm the benefits of STFF and M-C<sup>2</sup>MOS. STFF reaches the shortest rise time of 5.0 ns and the shortest fall time of 5.048 ns, which results in its best speed and performance.

Similarly, M-C<sup>2</sup>MOS exhibits a competitive rise time of 10.09 ns and a fall time of 5.188 ns. The design of TGFF has the largest fall time (94.63 ns), and hence, this is a reflection of its relatively slow switching characteristics. Other designs,

like 18TSPC\_T and C<sup>2</sup>MOS, achieve fall times below 5.1 ns, making them better. The results, therefore, indicate that STFF and M-C<sup>2</sup>MOS are the most versatile, with a trade-off between power, speed, and robustness,

and can be used for applications in energy-efficient and high-performance digital systems.



**Fig. 7** – Sweep analysis of M-C<sup>2</sup>MOS

The rise time and fall time, along with Clock-Q delay, are similar to the calculations of the circuit in sweep measure analysis of the STFF and MC<sup>2</sup>MOS, as shown in Fig. 6 and Fig. 7, respectively.

**Table 1** – The performance evaluation of different flip-flop circuits with a supply voltage of 1 V, using 32 nm CMOS technology

Design name	TGFF [6]	C <sup>2</sup> MOS [7]	S <sup>2</sup> CFF [8]	18TSPC_D [10]	18TSPC_T [10]	STFF [12]	M-C <sup>2</sup> MOS [12]
No of transistors	24	8	24	18	18	16	24
Clock-Q delay (ns)	17.59	10.75	8.79	17.57	7.53	7.52	7.025
Power consumption ( $\mu$ W)	0.1736	0.07051	0.11621	0.086	0.09223	0.08412	0.11025
T <sub>rise</sub> (ns)	10.08	5.001	10.08	10.08	10.07	5.0	10.09
T <sub>fall</sub> (ns)	94.63	5.016	25.19	20.15	5.036	5.04	5.18
PDP (fJ)	3.0537	0.75798	1.0214	1.5110	0.694	0.6327	0.7746

## 5. CONCLUSION

The novel flip-flop architectures, namely the Static Toggle Flip-Flop (STFF) and Modified C<sup>2</sup>MOS (M-C<sup>2</sup>MOS), demonstrate substantial improvements in speed, power efficiency, and area utilization compared to conventional designs like the Transmission Gate flip-flop, Clocked CMOS, and 18TSPC. The 16-transistor STFF resolves stability concerns inherent in traditional configurations such as the 18TSPC flip-flop [12], while the M-C<sup>2</sup>MOS architecture optimizes propagation delay reduction [12]. Simulations in a 32-nm CMOS process reveal that the proposed designs achieve a speed enhancement of up to 42% and a 28% improvement in power-delay product efficiency compared to existing counterparts. These evaluations, conducted against five flip-flop topologies in 32-nm technology, underscore the suitability of the STFF and M-C<sup>2</sup>MOS for low-power integrated systems, offering marked advancements in both performance and energy efficiency.

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### Розробка компактних, низькоенергетичних КМОП-тригерів для високошвидкісних застосувань

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Новий справжній однофазний тактовий транзистор з використанням Т-тригера (TSPC-T) представлений для ефективної роботи за низьких напруг живлення (VDD), забезпечуючи при цьому високу швидкість та надійність. Т-тригер значно мінімізує непотрібне споживання енергії, відключаючи тактові сигнали, коли вони непотрібні. Сучасна конструкція тригера має два різні варіанти виконання, а саме статичний перемикальний тригер (STFF) та модифікований тактовий КМОП-транзистор (M-C<sup>2</sup>MOS). STFF використовується для зменшення споживання енергії на 0,08412 мкВт, що є енергоефективним та кращим, ніж у таких конструкцій, як S<sup>2</sup>CFF (0,11621 мкВт) та TGFF (0,1736 мкВт), тоді як M-C<sup>2</sup>MOS використовується для мінімізації PDP на (0,7746 фДж), перевершуючи існуючі конструкції, такі як TGFF (3,0537 фДж) та S<sup>2</sup>CFF (1,0214 фДж). Це зменшує надлишкові переходи в схемі, одночасно підвищуючи загальну енергоефективність. Крім того, оновлення роботи тригера зменшує кількість необхідних пристроїв та зменшує споживання енергії. У цій роботі проведено порівняльний аналіз п'яти існуючих конструкцій тригерів (TGFF, C<sup>2</sup>MOS, S<sup>2</sup>CFF, 18TSPC, 18TSPC\_T) та запропонованої конструкції (STFF, M-C<sup>2</sup>MOS). Запропонована конструкція (STFF, M-C<sup>2</sup>MOS) має кращу потужність та затримку порівняно з існуючими високошвидкісними тригерами. Проектування та аналіз виконані з використанням 32-нм КМОП-технології. Результати моделювання показують, що конструкція STFF значно підвищує енергоефективність, зменшуючи споживання енергії на 10,3% при 1 В. Ці результати підкреслюють важливість STFF та M-C<sup>2</sup>MOS в оптимізації як потужності, так і швидкості, що робить їх дуже ефективними для сучасних малопотужних, високопродуктивних цифрових застосувань.

**Ключові слова:** Низьке енергоспоживання, Висока продуктивність, Зменшення затримки, Тригери.