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REGULAR ARTICLE

Transient Analysis and Comparison of Various Voltage and Current Mode Sense Amplifiers

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Sense amplifiers play an important role in the process of reading data stored in a memory bit. Their performance affects the power consumption and speed of the memory core. For greater performance, analysis of different sense amplifiers is necessary. The design and experimental quantitative study of a sense amplifier in voltage and current mode for SRAM is presented. This article presents a comparative analysis of research results for different sense amplifiers in voltage and current mode. The purpose of the study was to simulate a sense amplifier in voltage and current mode, as well as a comparison for analyzing the performance of parameters such as power and energy. The simulation tool is LT-spice using 180 nm technology.

Keywords: CMOS SRAMs, Sense Amplifier, Bit line, Voltage mode, Current mode

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1. INTRODUCTION

Sense Amplifier circuit design is becoming a major interest of modern designers in CMOS IC and low power VLSI technology.Static-Random-Access Memory (SRAM) is a non-volatile memory which can store data as long as power is supplied to the circuit [1-3]. The sense amplifier (SA) is a part of SRAM cell that operates only when there is need of data to be read from the memory [4]. SA is used to determine and amplify small difference voltage levels present at bit-line and bit line bar so, it can reach to its full digital voltage levels before the bit line's capacitances get completely charged or discharged .Since the circuitry doesn't wait for the bit line capacitances to get completely discharged or charged to detect its voltage levels either it is'0' or '1', hence shortening the time taken to read the data from the SRAM cells which in result increases the speed of operation. Since only one row of content is accessible per read cycle, each SRAM column requires only one sense amplifier [5]. Even if there is a very small voltage level or glitch present at bit- line and bit line bar, SA may decide its state and the memory quickly conclude the state whether it is at logic 1 or logic 0 instead of trying to calculate or wait for its complete voltage change, thus saving time in read operation of the SRAM cells [6]. SRAM can perform operations with low power consumption and at high speed. Yet its peripheral circuit can severely impact the speed and power of the system. Mainly performance of memory depends on the performance of SA such as delay and power dissipation. In the present era, the memory size is reducing, and the storage capability is rising. As the storing efficiency is rising, the time effect of reading and writing of data from the memory would be extremely fast. Also, SA affects the operational frequency for the memory; Thus, to achieve this motive various SAs are used. In this paper two SA topologies that have been selected are Basic differential voltage mode SA, Current Mirror Differential SA, Latch based and Current latched SA.

These SAs are designed for 180nm technology node with the help of LT Spice software tool with VDD taken at 1.8V [7]. In this technology SA are differentiated based on their energy and power consumption.

The paper is structured in following manner, firstly in introduction section a brief explanation of Voltage mode and Current SA is described, in section 2 schematic diversity of different sense amplifier topologies is elaborated. While, in section 3 results and analysis for sense amplifier topologies is presented. Section 4 suggests applications based on results. Section 5 concludes the finding of the paper.

2. SCHEMATIC DIVERSITY OF SENSE AMPLFIER

At present, voltage-mode Sense amplifier (VMSA) is widely used because of simplicity and robustness, most of which are based on cross- coupled invertors. The delay of SAs is small because of positive feedback of cross-coupled invertors while a voltage difference between a pair of bit lines is required due to the offset of voltage-mode SAs. The small bit cell must drive large capacitive bit lines

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resulting in large delay [8]. To overcome the problem, decreasing the capacitance of bit lines may be used by divided bit lines and two-level sensing technique. The local bit line connects fewer bit cells, resulting in low bit line discharge delay, but large energy is consumed because of full voltage swing on the bit lines, thus reducing the sensing delay and rendering current-mode SAs may have more advantages because of no extra intermediate voltage [9]. A current conveyor composed of four PMOS transistors was proposed in 1991, which presented a virtual short circuit to it insensitive to the bit line capacitance. Subsequently, most research on current-mode SAs focus on circuit improvement based on the current conveyor and the clamped bit line technique for higher speed and lower energy consumption.

2.1 Basic Differential Voltage Mode Sense Amplifier

Fig. 1 shows The Basic differential voltage mode sense amplifier (BDVMSA), it comprises of three resistors R1, R2 and R3 and a pair of NMOS transistors M1 and M2. This SA converts the small variation present at bit lines into complete swing at output junctions. Its function includes taking all small signal variations present at inputs and amplifying it into a large signal output level [10]. Its capability to discard common noise and amplifying true variation present between the signals characterizes the effectiveness of amplifier. Due to its slow speed of reading data, considerably high-power dissipation, and intrinsic high offset, basic VMSA is not used in SRAMs.

2.2 Current Mirror based Differential SA

The Current Mirror based Differential SA (CMDSA) as shown in Fig. 2 comprises of two NMOS Transistors M1 and M2 having an active current mirror load (PMOS Transistors M3 and M4) and an additional NMOS transistor (M5) acting as current source for biasing. The SA senses the point variation between the BL and BLB voltages as quickly as EN goes high and produces a desired output voltage [11].

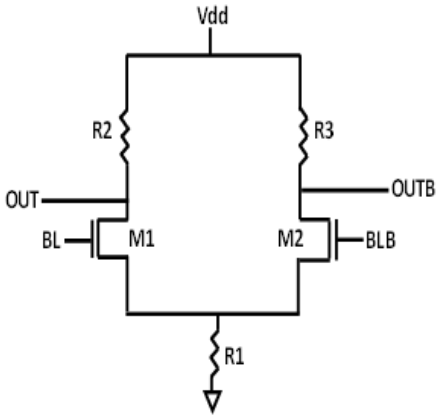

Fig. 1 – Basic differential voltage mode sense amplifier

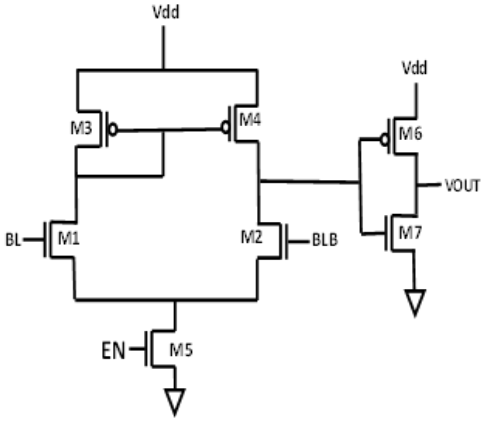

Fig. 2 – Current mirror based Differential Sense amplifier

The time taken by SA from commencement of the read operation till the output, primarily depends on the performance of the SA that is why the architecture of the SA is the prime measure in designing of CMOS memories.

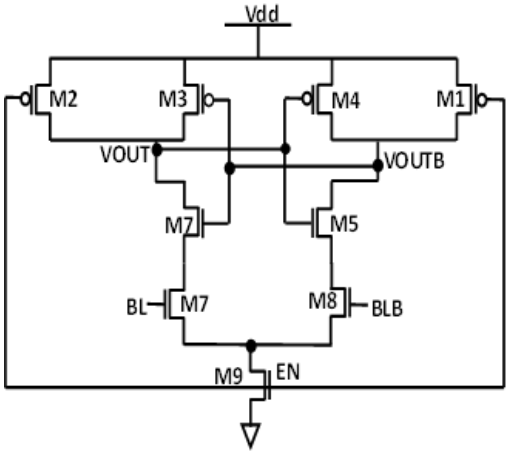

Fig. 3 – Current Latched sense amplifier

2.3 Latch Based Sense Amplifier

Topology of Latch Based SA (LBSA), during first phase of sensing the nodes should be pre-charged to V_{dd} before the sensing starts while EN is set to LOW [10, 11]. When considerable differential voltage sets up between the bit lines, BL and BLB, EN signal goes to active HIGH. The transistor M9 is switched ON, which tries to discharge the node N from HIGH to LOW once the sensing starts. While in second phase of sensing, because of the feedback action between M1, M4, and M2, M3, the small differential voltage between bit lines, BL and BLB, will get amplified to full swing i.e., HIGH, and LOW depending on the data stored on BL and BLB. It is apparent that there is still no isolation between the internal nodes and the bit lines, BL and BLB, of the memory in the proposed topology.

Current Latched SA (CLSA) as shown in Fig. 3. Comprises of five NMOS transistors and four PMOS transistors. When biasing signal SE is at LOW, the

voltage level at the output is set to LOW, and the PMOS M2, M4 pre- charge output junctions to V_{dd}. When the sensing signal SE changes to HIGH, M9 gets on and the node S is turned down to LOW [12]. Undergoing this, M6 and M8 the pair forming common source differential amplifier transfers the voltage variation present at BL and BLB to the output junctions that are output and output bar. After the completion of above step, the cross-coupled amplifier, that is formed by M5, M7, M3 and M1 amplifies the voltage difference between output and output bar to a full swingvoltage level [13]. That is why we can determine and amplify the BL voltage level without any kind of current drifting from BL to output junction [14-15]. It concludes with the working of current Latch SA.

3. RESULT AND ANALYSIS

This Section presents the simulation results of basic differential VMSA, current mirror differential SA, latch-based SA, and current latch SA. The simulations are performed using LT Spice tool at 180nm technology node with power supply of 1.8 V to compare circuits on basis of dynamic power and energy [16]. The simulation results are clarified in sub section

In Fig. 4 output waveform of basic differential SA is shown where output V(out) follows BLB and in Fig. 5. Waveform of current mirror SA is shown. When EN is High V(out) follows BLB.

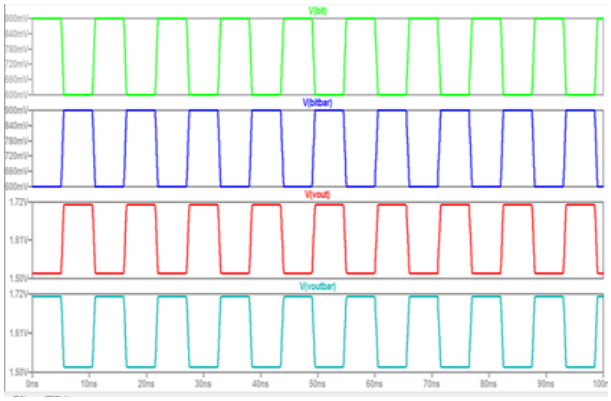

Fig. 4 – output waveform of basic differential SA

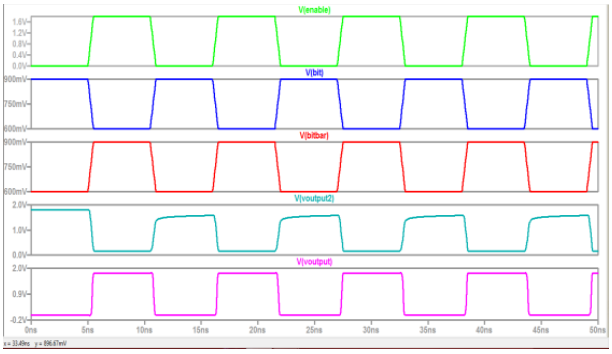

Fig. 5 – Output waveform of current mirror differential SA

In Fig. 6 waveform of latch- based SA is shown. When EN is High V(out) follows BLB and when EN is LOW the V(out) is HIGH and in Fig. 7 waveform of current latch-based SA is shown. When EN is High V(out) follows BLB and when EN is LOW the V(out) is high.

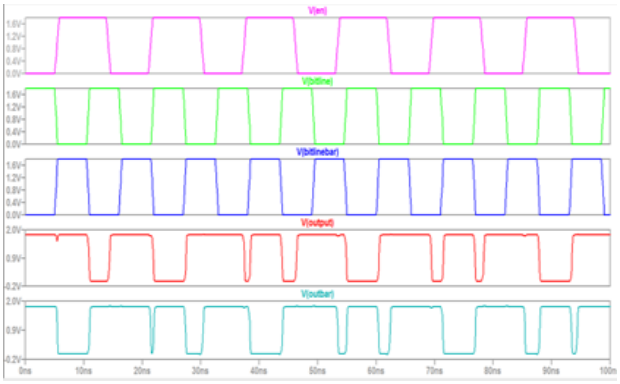

Fig. 6 – Output waveform of latch- based SA

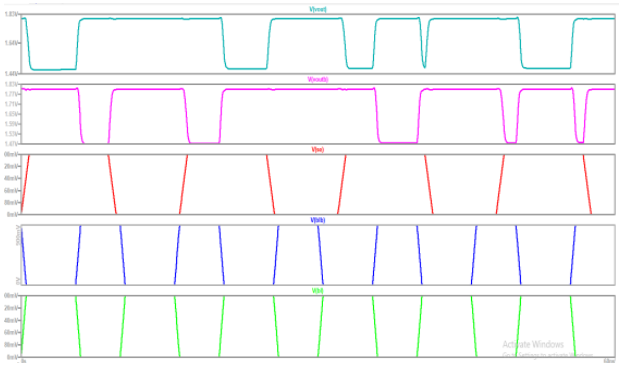

Fig. 7 – Output waveform of current latch-based SA

3.1 Power and Energy Analysis

For obtaining better results while designing the memory cell, performance of parameters like energy and power are important [17]. While designing the SA power dissipation should remain minimal. this action takes place when the circuit is not active. It means circuits behave in quiescent mode [18-19].

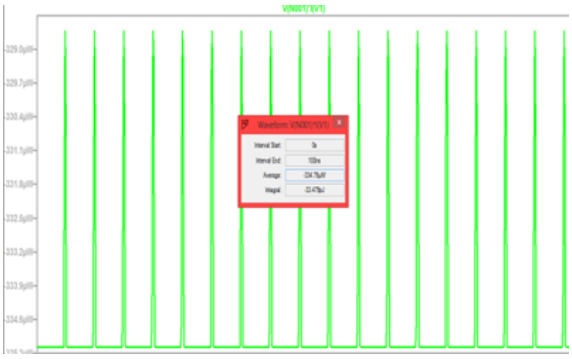

Fig. 8 – Power and Energy of basic differential SA

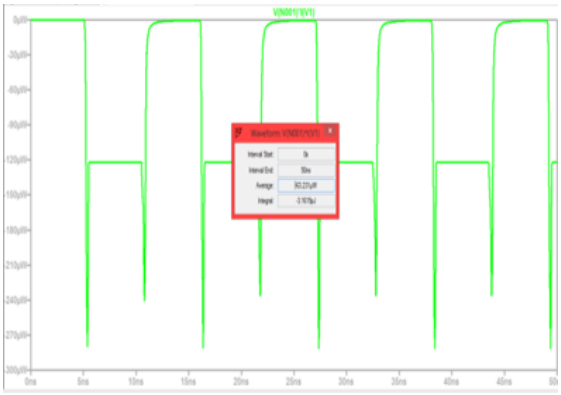

Fig. 9 – Power and Energy of current mirror differential SA

Fig. 10 – Power and Energy of latch- based SA

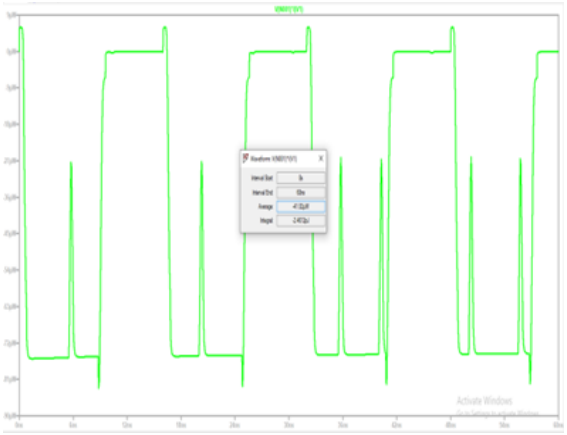

Fig. 11 – Power and Energy of current latch-based SA

The overall power consumption within the circuit is shown. Figs. 8-11 shows power and energy analysis of BDVMSA, CMDSA, LBSA and CLSA respectively.

Table 1 – Comparison of different sense amplifiers

Sense Amplifier	Power (μW)	Energy (pJ)	No. of transistor
BDVMSA	334.77	33.47	2
CMDSA	63.231	3.165	5
LBSA	19.54	1.939	9
CLSA	41.02	2.462	9

It can be theorized from Table 1. that latch based SA consumes least power and energy. i.e., 19.54 μW and 1.939 pJ respectively. Basic SA consumes highest power and least area, as it contains comparable resistances. Moreover, current based latch consumes a little more power and energy as compared to latch-based amplifier for 180nm technology and 1.8 V power supply.

4. CONCLUSION

In this paper a comparative transient analysis of different configuration of sense amplifiers are presented. They are simulated in Lt spice at 180 nm technology node. The result comparison of various parameters of the two topologies is shown in Table 1. power and energy consumptions of different sense amplifiers are found out in which latch sense amplifier has the lowest power consumption that is almost 1/18 times of power consumption of basic differential voltage sense amplifier. As the power requirements are less hence, they are turning out to be the best for smartphones and laptops because they reduce the power consumption and enhances the speed of operation which in result increases the battery backup and speed of the system [20-22]. Hence it can be concluded that the performance of SA has increased remarkably over time to time and can be improved further for better results. According to analysis, uses of the amplifiers are defined in the application section.

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Аналіз перехідних процесів та порівняння різних підсилювачів вимірювання напруги та струму

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Підсилювачі зчитування відіграють важливу роль в процесі зчитуванні даних, які зберігаються в біті пам'яті. Їх продуктивність впливає на споживання енергії та швидкість ядра пам'яті. Для більшої продуктивності необхідні аналіз різних підсилювачів зчитування. Представлено проектування та експериментальне кількісне дослідження підсилювача зчитування в режимі напруги та струму для SRAM. У цій статті представлено порівняльний аналіз результатів досліджень для різних підсилювачів зчитування напруги та струму. Мета дослідження полягала у моделюванні підсилювача зчитування в режимі напруги та струму, а також порівняння для аналізу продуктивності таких параметрів, як потужність та енергія. Інструментом для моделювання є LT-spice з використанням технології 180 нм.

Ключові слова: CMOS SRAMs, Підсилювач зчитування, Бітова лінія, Режим напруги, Режим струму.