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REGULAR ARTICLE

A Novel Energy-Efficient Approach for RT-Free TSPC Dual-Edge Triggered Flip-Flops Using STC

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Power consumption reduction in both static and dynamic forms is essential in digital circuits, especially in clocking networks and flip-flops used in GPUs and AI processors. Dual-edge-triggered flip-flops (DET-FFs) improve efficiency by capturing data on both clock edges, enabling lower clock frequency operation and reducing dynamic power consumption. However, conventional DET-FFs suffer from excessive switching activity and redundant transitions, leading to unnecessary power dissipation. To address this, a Single-Transistor-Clocked Dual-Edge-Triggered Flip-Flop (STC-DET-FF) is proposed, integrating True Single-Phase Clocking (TSPC) with Single-Transistor-Clocked Buffers (STCBs) to eliminate redundant transitions and optimize power efficiency. Designed using 32 nm CMOS technology, the STC-DET-FF is evaluated based on power consumption, propagation delay, and Power-Delay Product (PDP). Simulation results show that the proposed design achieves a significant reduction in power consumption, outperforming FN_C-DET by 14 % at 0.4 V and 9.5 % at 0.8 V. Additionally, it exhibits the lowest PDP of 0.6879 fJ, which is a major improvement compared to FN_C-DET (4.364 fJ) and TGFF (8.807 fJ). These results demonstrate the STC-DET-FF's effectiveness in minimizing power dissipation while maintaining performance, making it a viable solution for low-power and high-performance computing applications.

Keywords: DET, Low power consumption, PDP, Flip-flop.

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1. INTRODUCTION

Power consumption is a critical challenge in CMOS digital circuit design, driven by the increasing computational demands of technologies such as Graphics Processing Units (GPUs) and AI neural network processors. The computing power required for AI training has doubled approximately every 3.4 months [1], making efficient power management essential. Clocking circuitry, including flip-flops (FFs) and clock distribution networks, accounts for over 50% of total power consumption in modern [2] processors. Therefore, optimizing power dissipation in these systems is crucial.

Flip-flops play a fundamental role in processor data storage and timing. Traditional single-phase clocked FFs utilize only one clock edge (rising or falling) per cycle, leading to inefficient power usage. DET-FFs [1] address this limitation by utilizing both clock edges, effectively reducing the required clock frequency while maintaining the same throughput. This approach significantly enhances energy efficiency, making DET-FFs a promising solution for high-performance, low-power processors.

A novel DET-FF topology combined with a True Single-Phase Clock (TSPC) mechanism further improves power efficiency by addressing two major sources of power loss:

1. Elimination of Redundant Clock Switching: This design completely removes unnecessary transitions in both the clock signal and internal flip-flop components, reducing energy waste.

2. Integration of Single-Transistor-Clocked Buffers (STCBs): The proposed design incorporates STCBs that eliminate redundant transitions, further minimizing power consumption in both the flip-flop and clocking network.

These advancements contribute to substantial power savings, making the design ideal for energy-efficient, high-performance processors. The proposed hybrid logic-based DET-FF was evaluated using 32 nm CMOS technology to assess its speed, power efficiency, and delay characteristics under various conditions. Simulations were conducted using the Custom Compiler tool at a 1 V power supply and 500 MHz clock frequency, ensuring accurate real-world performance representation. The key performance metrics analyzed included power consumption, propagation delay, and process corner variations across different voltage and temperature conditions. The results demonstrated significant improvements in energy efficiency, reduced power dissipation, and enhanced switching performance, making the design suitable for high-speed, low-power applications.

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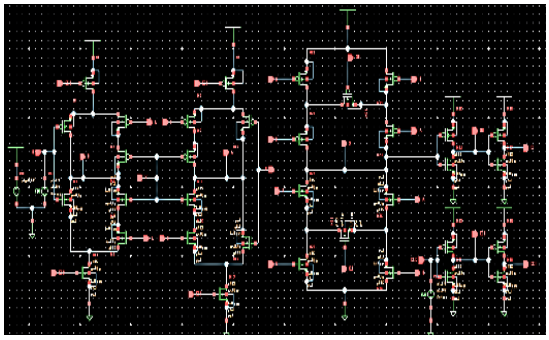
2. EXSISTING METHODES

Early efforts in energy-efficient Dual-Edge Triggered Flip-Flops (DET-FFs) primarily aimed at reducing switching activity to lower power consumption. Some approaches simplified circuit structures, while others focused on lowering clock frequencies. However, these designs faced limitations such as redundant transitions and conflicting internal interactions, reducing overall efficiency. With advancements in flip-flop technology, newer methods have emerged to enhance power and speed efficiency.

Some designs introduced multiple C-elements [3] to eliminate glitches, while others evaluated single-edge versus dual-edge pulsed flip-flops. Although dynamic DET-FFs [6] improved energy efficiency through pulse-labeling techniques, they still suffered from high power-delay product (PDP), restricting their usability. True Single-Phase Clock (TSPC) architectures addressed clocking efficiency but retained redundant transitions. Recent research has explored Single-Transistor-Clocked Buffers (STCBs) [4], leading to the development of the STC DET-FF [5]. By eliminating unnecessary transitions and optimizing data propagation, these designs significantly reduced PDP, enhancing power efficiency.

The FN_C-DET flip-flop [3] is a conventional DET-FF that employs C-elements and floating nodes to process data on both clock edges, achieving high throughput without requiring high-frequency clocks. The C-element synchronizes data sampling in asynchronous circuits, outputting a logic high or low state only when both inputs match, ensuring robust operation. Floating nodes temporarily store logic states using circuit capacitance, reducing dynamic power consumption. However, these nodes are susceptible to noise, leakage currents, and power dissipation. To mitigate these challenges, controlled charge retention and leakage minimization techniques were implemented.

FN_C-DET operates using a two-phase clocking scheme, generating complementary clock signals (CKB and CKI) to control transistor switching. Fig 1(a) shows that these signals facilitate efficient data sampling on both clock edges, maintaining timing consistency and minimizing glitches. The waveform in Fig 1(b) illustrates this transition process. When CLK is high, the master latch is activated, allowing input data (D) to [1] propagate through intermediate nodes. The C-element ensures asynchronous data transfer while preventing errors.



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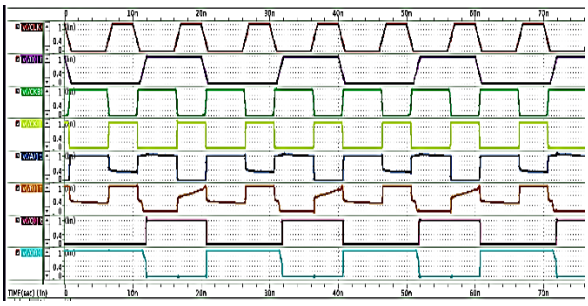


(b)

Fig. 1 – (a) Circuit diagram of FN_C-DET [3]. (b) Waveform

The slave latch remains disabled to maintain output stability. When CLK is low, the slave latch captures and transfers the master latch state to the output (*Q*). Clocked transistors sustain the slave latch until the next clock pulse, ensuring stability. The C-element minimizes unnecessary transitions, improving efficiency.

A major drawback of FN_C-DET is redundant clock-induced transitions, leading to power dissipation even when input data remains unchanged. These transitions cause contention between *C*-elements, generating transient short circuits and increasing power loss. Optimization strategies, including controlled charge conservation and selective transistor activation, help mitigate switching activity while preserving efficiency.

3. PROPOSED TSPC STC-DET

Conventional dual-edge-triggered flip-flops (DET-FFs) suffer from redundant transitions between clocked transistors, leading to excessive power consumption. To overcome this limitation, a novel low-power True Single-Phase Clock (TSPC) DET-FF design [7] is proposed [1]. The design incorporates an optimized Single-Transistor-Clocked Buffer (STCB) topology, which effectively eliminates redundant switching activities, improving overall efficiency. Fig 2(a) illustrates the proposed STC-DET flip-flop, while Fig 2(b) presents its schematic diagram based on a master-slave latch configuration. This flip-flop comprises two key components: an upper flip-flop that captures data on the rising edge of the clock and a lower flip-flop that captures input on the falling [1] edge. This dual-edge-triggering mechanism ensures efficient data sampling while significantly reducing power dissipation.

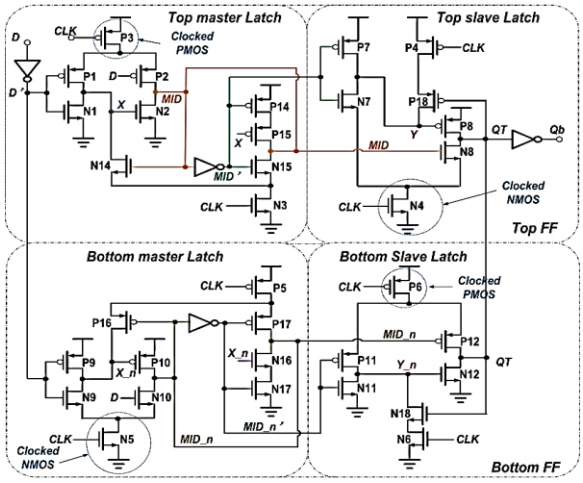
3.1 Functionality of the Upper Flip-Flop

When the clock signal (CLK) is low, the clocked PMOS transistor (P3) in the master latch of the upper flip-flop is enabled, allowing node X to retain the logic state of *D′′*. Since *D′′* is equivalent to *D*, transistors P2 and N2 form a virtual inverter, facilitating signal propagation to the MID node. Simultaneously, the clocked NMOS transistor (N4) in the slave latch remains off, preventing unnecessary power dissipation. Consequently, output node QT remains stable, avoiding redundant transitions. In the data sampling path, “transistors N1, N2, P1, P2, and P3 establish a negative-triggered STCB, employing only a single clocked PMOS transistor (P3)” [1], thereby eliminating redundant transitions

present in conventional DET-FF architectures like FN_C DET [3] and FS-TSPC designs [7]. Additionally, transistor contention is entirely avoided [5]. While NMOS transistor N3 is also clocked, it primarily functions as part of the keeper circuit rather than data sampling. The key clocked transistors – P3, N4, N5, and P6 – are marked in Fig 2(a). A positive-triggered STCB, formed by N4, N7, N8, P7, and P8, ensures smooth data propagation in the slave latch. When CLK transitions high, P3 is turned off, disabling the conduction paths associated with P1 and N2 while preserving the MID node state via a keeper circuit composed of N3, N15, P14, and P15. If X holds a low state (0), a pull-down keeper circuit (N14 and N3) maintains it. Concurrently, the activation of clocked NMOS transistor N4 allows Y to acquire the value of MID", which is then transferred to QT via a virtual inverter formed by N8 and P8. This enables the upper flip-flop to operate synchronously with the rising clock edge.

3.2 Functionality of the Lower Flip-Flop

When CLK is low, the clocked NMOS transistor (N5) in the bottom master latch is disabled, preventing conduction through N9 and P10. The MIDn state is maintained by a keeper circuit comprising N16, N17, P5, and P17. If Xn holds a high state (1), a pull-up keeper circuit (P16 and P5) sustains it. In the bottom slave latch, the clocked PMOS transistor (P6) activates when CLK is low, allowing Yn to assume the value of MIDn". Transistors P12 and N12 form a virtual inverter, ensuring accurate transfer of MIDn to QT just before the falling clock edge, synchronizing the lower flip-flop with CLK's falling edge. Redundant transitions are eliminated when the input signal D remains unchanged, reducing unnecessary switching activity. Two additional STCBs, composed of N5, N9, N10, P9, and P10, and P6, N11, N12, P11, and P12, further enhance efficiency. When CLK transitions high, NMOS transistor N5 activates, allowing Xn to acquire the logic state of D". Transistors P10 and N10 form a virtual inverter, ensuring precise propagation of D to MIDn. Simultaneously, PMOS transistor P6 in the bottom slave latch is deactivated, disconnecting conductive paths associated with P11 and N12. As a result, QT remains stable, maintaining data integrity throughout the clock cycle.



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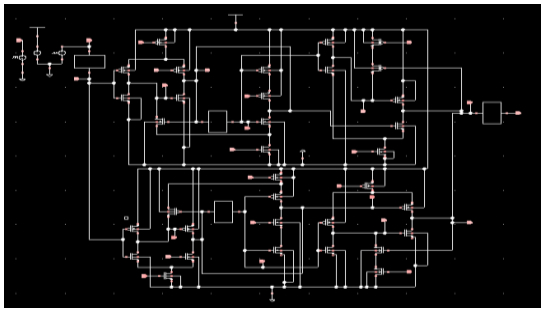

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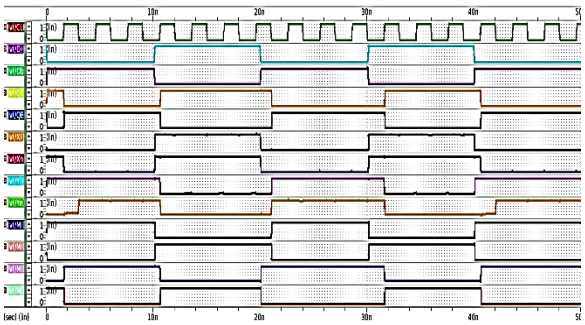


(c)

Fig. 2 – (a) Circuit Diagram of TSPC single transistor clocked DET, STC-DET [1]. (b) Schematic diagram. (c) Output waveform with internal nodes

The STC-DET flip-flop achieves dual-edge triggering by activating the upper and lower slave latches on opposite clock edges. The upper slave latch operates on the rising edge, while the lower slave latch functions on the falling edge. This dual-edge sampling effectively doubles the data throughput. The complementary operation of the slave latches ensures that one remains transparent while the other remains opaque, enabling seamless data transfer to QT without contention, thereby enhancing reliability.

A critical design feature is ensuring that no node is left floating, maintaining stable voltage levels and improving speed. This makes the STC-DET flip-flop well-suited for high-performance, low-power applications. Additionally, the design includes a scan enable signal and scan input within the master latches for improved testability. The architecture is scalable and can be adapted into a Set-Reset (SET) flip-flop by integrating appropriate keeper circuits within either the top or bottom sections.

4. SIMULATION RESULTS

The proposed Single-Transistor-Clocked (STC) DET flip-flop demonstrates superior speed, power efficiency, and energy optimization, making it highly suitable for low-power VLSI applications.

The designed STC-DET flip-flophas been analyzed and compared with state-of-the-art dual-edge-triggered (DET) flip-flops, including TGFF, CBS_IP, S-TSPC_DET, and FN_C_DET [1]. The comparison evaluates key parameters such as transistor count, clock-to-Q delay (C-Q delay), rise time, fall time, power dissipation, and power-delay product (PDP). Table 1 provides

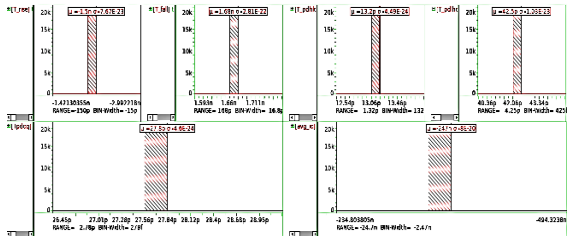
a summary of these comparisons.

Fig 2(b) provides a detailed schematic representation, illustrating a master-slave latch configuration. The design features two distinct flip-flops: The upper flip-flop samples data on the rising edge of the clock, ensuring synchronized data retention. The lower flip-flop captures input on the falling edge, facilitating continuous data propagation without unnecessary transitions. This dual-edge-triggered operation minimizes power dissipation while maintaining high-speed performance, making the STC-DET highly suitable for low-power applications. Fig 2(c) depicts the output waveform, highlighting the internal node voltages to demonstrate stable and synchronized switching behavior. The well-regulated voltage levels confirm power-efficient operation, ensuring minimal energy loss.

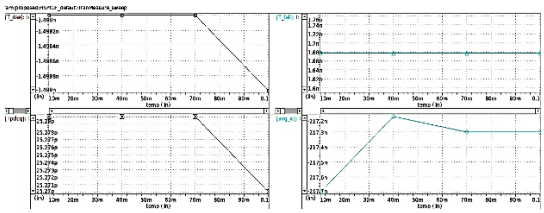
The STC-DET flip-flop consists of 42 transistors, the highest among the evaluated designs. However, it exhibits the best power efficiency and lowest PDP, making it an attractive choice for low-power circuit design [7]. The measured C-Q delay is 0.02784 ns, significantly lower than FN_C_DET (12.82 ns) and TGFF (17.59 ns). This improvement in propagation delay enhances overall system performance and reduces clock latency. The rise and fall times of STC-DET are recorded as 1.496 ns and 1.677 ns, respectively. While these values are slightly higher than those observed in S-TSPC_DET and CBS_IP, their impact on system performance is minimal due to reduced power consumption and fewer redundant switching activities. Among all the flip-flops evaluated, STC-DET exhibits the lowest power dissipation [7], consuming only 0.2472 μW – significantly lower than TGFF (0.5008 μW) and FN_C_DET (3.404 μW).

The substantial reduction in power consumption can be attributed to three primary factors: Elimination of redundant switching activity. Minimization of internal contention. Reduction in the number of clocked transistors (eight), improving energy efficiency. PDP is a critical metric for power efficiency, and the STC-DET achieves the lowest recorded value of 0.6879 fJ, significantly outperforming FN_C_DET (4.364 fJ), TGFF (8.807 fJ), and CBS_IP (2.781 fJ). This considerable reduction in PDP highlights the efficiency of the proposed design in achieving both high speed and low power dissipation.

Fig 3(a) illustrates the Monte Carlo analysis results for key performance parameters of the STC-DET flip-flop, including rise time (T_rise), fall time (T_fall), clock-to-Q delay (T_pdcq), and power dissipation. The histograms show statistical variations, ensuring that the design remains stable across process variations. The minimal standard deviation in measured values confirms the robustness and reliability of the STC-DET design under different operating conditions. Fig 3(b) presents the process and temperature sweep results, demonstrating the impact of temperature variations on the STC-DET flip-flop. The graphs highlight the stability of key timing parameters, such as rise time, fall time, and propagation delay, over a wide temperature range. The results confirm that STC-DET maintains consistent performance across different process corners and temperature fluctuations, making it highly suitable for low-power, high-performance applications.



(a)



(b)

Fig 3. – (a) Monte Carlo analysis at 20k samples. (b) Sweep results

Table 1 – The performance evaluation of different flip-flop circuits was conducted at a 500 MHz operating frequency, with a supply voltage of 1 V, at 25 °C, using 32 nm CMOS technology

Design Name	Transistor-Count	C-to-Q Delay (ns)	Rise Time (ns)	Fall Time (ns)	Power(μW)	PDP_CQ (fJ)
TGFF [6]	24	17.59	10.08	0.0946	0.500	8.807
CBS_IP [4]	21	0.3618	0.88	0.7344	7.689	2.781
S-TSPC_DET [5]	36	0.0045	1.98	0.0412	0.497	2.267
FN_C_DET [3]	34	12.82	5.83	20.63	3.404	4.364
Proposed STC [1]	**42**	**0.0278**	**1.49**	**1.677**	**0.247**	**0.687**

Power consumption in STC-DET was analyzed under varying switching activity conditions. The results indicate that STC-DET is 14 % and 9.5 % more power-efficient than FN_C-DET at operating voltages of 0.4 V and 0.8 V, respectively. This advantage is more pronounced at lower switching activity levels (5 %-15 %), which are typical in modern processors. However, at switching activity levels exceeding 20%, FN_C-DET approaches the power efficiency of STC-DET. This is primarily due to STC-DET's effective elimination of redundant transitions, which contributes to reduced overall power dissipation. Ensuring reliable flip-flop operation requires adherence to setup and hold time constraints. The setup time in STC-DET is dictated by the propagation delay from D to MID_n, while the hold time is determined by the settling behavior of QT [1] following a "clock transition. The worst-case hold time scenario arises when D transitions too close to the rising clock edge" [1], potentially affecting QT's charging

characteristics. Despite these factors, the overall timing constraints remain within acceptable limits, ensuring robust performance and suitability for high-speed, low-power applications.

5. CONCLUSION

This work introduces a novel low-power dual-edge-triggered flip-flop (STC-DET) designed to significantly reduce power consumption by utilizing a Single-Transistor-Clocked Buffer (STCB). Unlike conventional DET flip-flops, STC-DET eliminates redundant transitions (RTs) and minimizes contention, leading to enhanced energy efficiency. Performance evaluation demonstrates that STC-DET achieves notable power savings, reducing consumption by 14 % at 0.4 V and 9.5% at 0.8 V compared to FN_C-DET. Additionally, it achieves the lowest power-delay product (PDP) among the analyzed DET designs, measuring just 0.6879 fJ – an improvement over FN_C-DET (4.364 fJ) and TGFF (8.807 fJ). These findings highlight the superior power efficiency and performance optimization of the proposed architecture. With its reduced clocked transistor count and elimination of redundant switching activity, STC-DET strikes an optimal balance between power consumption and performance.

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Новий енергоефективний підхід для створення TSPC-тригерів з двостороннім спрацьовуванням без постійного струму з використанням STC

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Зниження споживання енергії як у статичній, так і в динамічній формах є важливим у цифрових схемах, особливо в мережах тактування та тригерах, що використовуються в графічних процесорах та процесорах штучного інтелекту. Тригери з подвійним фронтом спрацьовування (DET-FF) підвищують ефективність, захоплюючи дані на обох фронтах тактового сигналу, що дозволяє працювати з нижчою тактовою частотою та зменшує динамічне споживання енергії. Однак звичайні DET-FF страждають від надмірної активності перемикання та надлишкових переходів, що призводить до непотрібного розсіювання потужності. Для вирішення цієї проблеми пропонується тригер з подвійним фронтом спрацьовування (STC-DET-FF) та однотранзисторним тактовим сигналом, який інтегрує справжнє однофазне тактування (TSPC) з однотранзисторними буферами тактування (STCB) для усунення надлишкових переходів та оптимізації енергоефективності. Розроблений з використанням 32-нм CMOS-технології, STC-DET-FF оцінюється на основі споживання енергії, затримки поширення та добутку затримки потужності (PDP). Результати моделювання показують, що запропонована конструкція досягає значного зниження споживання енергії, перевершуючи FN_C-DET на 14% при 0,4 В та на 9,5% при 0,8 В. Крім того, вона демонструє найнижчий PDP 0,6879 фДж, що є значним покращенням порівняно з FN_C-DET (4,364 фДж) та TGFF (8,807 фДж). Ці результати демонструють ефективність STC-DET-FF у мінімізації розсіювання потужності при збереженні продуктивності, що робить її життєздатним рішенням для застосувань з низьким енергоспоживанням та високою продуктивністю.

Ключові слова: DET, Низьке енергоспоживання, PDP, Тригер.