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REGULAR ARTICLE

Temperature and Geometric Scaling Effects on CMOS Inverter Performance: A Static and Dynamic Parametric Analysis

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Timing analysis serves as a cornerstone in VLSI design methodology, directly influencing both performance metrics and energy efficiency. The calculation of signal transition delays holds significant research importance due to its impact on overall system characteristics. This study investigates the fundamental mechanisms governing static and dynamic CMOS inverter operations. To measure device behavior, we look at important indicators such as voltage transfer curves, saturation voltage, peak drain current (ID peak), delay, and rise/fall times. And how to control it. This study examines the effects of scaled channel sizes (90-360 nm length, 120-1200 nm width) and extreme temperatures (– 108°C to 270 °C). The findings indicate that performance is significantly altered by thermal and geometric shifts; for instance, the ID peak decreases from 17.05 μA at – 108 °C to 7.76 μA at 189 °C, and reduced channels shift the switching threshold. We map the combined effect of NMOS and PMOS responses on power-delay trade-offs using CADENCE Virtuoso. Resilient CMOS design for a range of operating conditions and process tolerances is guided by these insights.

Keywords: CMOS inverter, Temperature stability, Channel scaling, Static/Dynamic analysis.

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1. INTRODUCTION

Modern microelectronics is supported by Complementary Metal-Oxide Semiconductor (CMOS) technology, which offers unparalleled power efficiency and integration density for applications ranging from microprocessors to Internet of Things (IoT) sensors [1, 2]. By strategically managing charge carriers, its fundamental innovation – complementary *n*-type (NMOS) and *p*-type (PMOS) transistor pairs – allows for nearly zero static power [1]. These architectures attain previously un-heard-of levels of computational efficiency and miniaturization as scaling advances toward 45 nm nodes [3, 4]. However, accurate control of process and environ-mental variances is necessary to maximize CMOS performance.

This optimization relies heavily on Electronic Design Automation (EDA) tools such as CADENCE Virtuoso, which allow simulation-driven improvement of power-delay trade-offs, noise immunity, and slew rate [5-6]. For describing nanoscale effects, Cadence's comprehensive process libraries and integrated workflow from schematic design to post-layout verification offer significant benefits [7, 9].

Through previous dynamic studies, we find that there is a significant focus on the delay time of propagation accompanied by the fall time, without considering the rise time, which in turn has an effect on the efficiency of the circuit. We will study this carefully along with other times and how to control them while taking the conditions into account, along with a static study that has been conducted before but has not been comprehensively analyzed, yielding results that differ significantly from previous studies.

Despite these capabilities, two enduring issues threat-en circuit reliability:

– Temperature instability (– 108 °C to 270 °C): Degrades timing margins and current drive by changing threshold voltages and carrier mobility.

– Geometric variability: Channel width: 120-1200 nm; length: 90-360 nm; shifts switching thresholds and saturation points by varying transistor β-ratios (β_n/β_p) [18-20].

NMOS/PMOS transistors are disproportionately affected by these changes, which results in asymmetric performance degradation in key metrics:

– Static parameters include peak drain current (ID, peak), saturation points, and voltage transfer

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characteristics (VTC).

– Dynamic parameters include rise/fall times (t_r, t_f) and propagation delay (t_p) [10].

A thorough examination of these co-dependent effects on 90 nm CMOS inverters is presented in this work. Our methodology combines static characterization of VTC shifts, ID peak variation, and ß-ratio imbalances under thermal/geometric stress with dynamic evaluation of timing parameters (t_p, t_r, and t_f) under identical conditions.

With the aid of Cadence Virtuoso simulations, we quantify how:

– Sub-zero temperatures cause ID to increase and peak by 51 % (17.05 μA at – 108 °C vs. 11.31 μA at 27 °C), but degrade timing at temperatures above 135 °C.

– Saturation is accelerated by 9 % by PMOS widening (W_p increases) and delayed by 12 % by NMOS channel narrowing (W_n decreases).

– Non-linear power-delay trade-offs are revealed by concurrent scaling of both transistors.

Our research offers fundamental knowledge for creating reliable CMOS systems under varying environmental and process conditions.

2. CMOS INVERTER

With its comprehensive switching action, the CMOS inverter, the basic building block of digital integrated circuits, allows for the implementation of intricate logic gates. Two enhancement-mode transistors make up the circuit, as seen in Fig. 1:

A N-channel MOSFET (NMOS) pull-down network that is grounded (GND)

A pull-up network for PMOS (P-channel MOSFET) connected to the supply voltage (VDD)

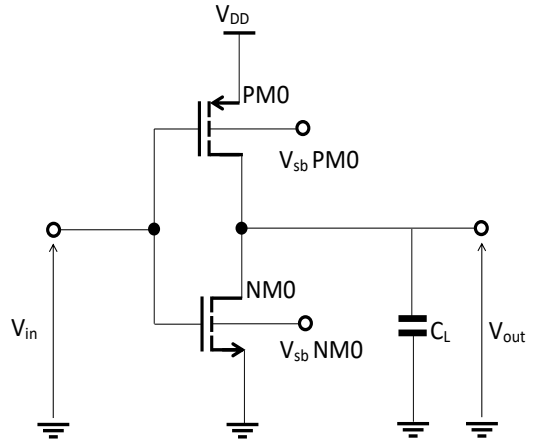

Fig. 1 – Conventional CMOS inverter circuit

Mutually exclusive conduction is ensured by this complementary arrangement, where PMOS stays off and NMOS activates (pulling VOUT to GND) when input (VIN) is high. On the other hand, PMOS turns on (pulling VOUT to VDD) and NMOS turns off when VIN is low. This push-pull mechanism offers:

Rail-to-rail output swing (0 to VDD)

Near-zero static power consumption

High noise immunity [11]

The Voltage Transfer Curve (VTC) of the CMOS inverter, which is shown in Fig. 2, describes its DC behavior. Three crucial operational regions are shown by this sigmoidal curve:

– NMOS saturation/PMOS cutoff (VIN < VTN)

– Region of transition (VTN < VIN < VDD – |VTP|)

– PMOS saturation/NMOS cutoff (VIN > VDD – |VTP|)

When both transistors are operating at saturation at the same time, producing peak current (ID,peak), the steepest slope region (Region 2) is created. The voltage gains (dV_{OUT}/dV_{IN}) is determined by this concurrent conduction, which also serves as the main source of dynamic short-circuit power and directly affects propagation delay timing [12].

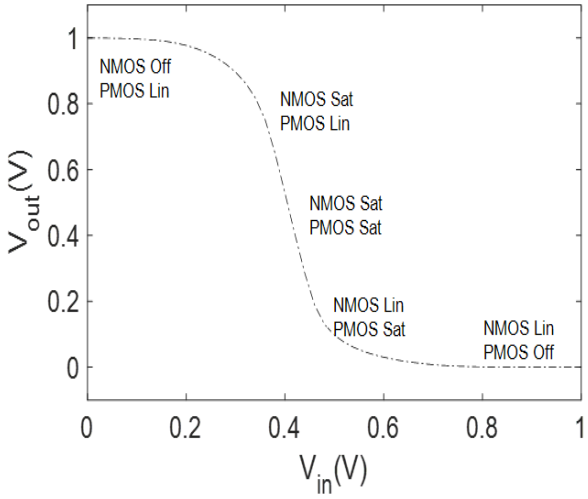

Fig. 2 – Voltage Transfer Characteristic (VTC) of CMOS inverter

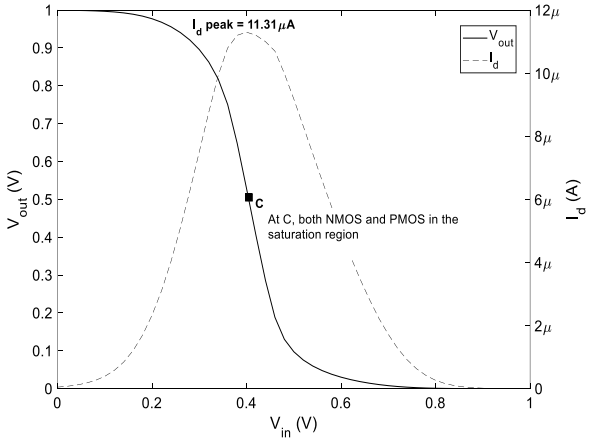

Fig. 3 – The transfer function $V_{out} = f(V_{in})$ and the drain current

The switching threshold voltage (VM), a crucial parameter for noise margin analysis, is defined by the mid-point of the VTC (where $V_{IN} = V_{OUT}$).

3. STATIC STUDY

Cadence Virtuoso™, an industry-standard electronic design automation (EDA) platform, enables rigorous CMOS circuit characterization through integrated schematic capture, simulation, and analysis tools [13, 14]. Its unified environment supports comprehensive modeling of analog/digital topologies without physical prototyping [15]. Researchers define component parameters (e.g., W/L ratios), interconnects, and stimuli (DC/AC/transient sources) to simulate circuit behavior across operational conditions including parametric sweeps of temperature (– 108 °C to 270 °C) and geometry (channel length: 90-360 nm; width: 120-1200 nm). Key capabilities leveraged in this work: Transient analysis: Propagation delay (t_p), rise/fall times (t_r/t_f) We implemented a 90 nm CMOS inverter (Fig. 1) as the validation platform, utilizing Specter for physics-based BSIM4

3.1 Voltage Transfer Analysis and Drain Current

Under nominal conditions (T_{amp} = 27°C, VDD = 1 V), we first evaluated the static performance of the CMOS inverter by sweeping the input voltage V_{IN} from 0 to VDD. As seen in Fig. 3, the inverter output voltage V_{OUT} is complementary to the input voltage V_{IN}, and the switching voltage of the CMOS inverter, denoted by VM, is extracted at the unique voltage where the output voltage V_{OUT} exactly equals the input voltage V_{IN} = 417.85 mV. At this operating point, both transistors are simultaneously biased in saturation and carry the maximum drain current ID,peak = 11.31 μA resulting from the maximal channel conduction. These values provide the following key reference values: VM = 417.85 mV for noise margin symmetry ID,peak = 11.31 μA for dynamic power dissipation for the next thermal and dimensional variation studies.

3.2 Temperature-Dependent Performance Characterization of CMOS Inverters

Fig. 4 and Table 1 detail the impact of temperature on the DC behavior of a CMOS inverter circuit. Compared to the nominal 27 °C case (black plot), it can be seen that:

– Transfer Characteristics offset Left for temperatures below 27 °C with a lower switching voltage (VM) Right for above with a higher one [16]

– Left for temperatures below 27 °C with a lower switching voltage (VM)

– Right for above with a higher one [16]

– Switching Voltage (VM) varies Almost linearly from 399.54 mV (– 108 °C) to 480.35 mV (270 °C) ΔVM ≈ + 0.32 mV/°C temperature coefficient

– Almost linearly from 399.54 mV (– 108 °C) to 480.35 mV (270 °C)

– Peak Current Degradation Increasing temperature causes: 17.05 μA (– 108 °C) to drop to 7.76 μA (189 °C) – 13.4 %/100 °C current drop [17]

– Increasing temperature causes: 17.05 μA (– 108 °C) to drop to 7.76 μA (189 °C) Qualitative Device Physics explanation:

– At low temperature, the higher carrier mobility allows for high current (ID,peak) at a lower input voltage (V_{IN})

High temperature gives lower mobility but also lower thresholds (VTN/VTP), hence a higher VM but lower current drive

– Low T: improved dynamic (Higher ID,peak)

– High T: Noise margin (VM) worse + smaller drive

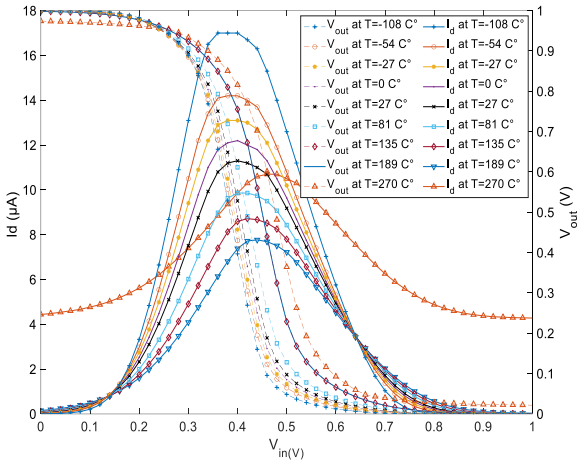

Fig. 4 – The temperature influence on transfer function and drain current

Table 1 – Temperature Influences the Difference in ID peak and its influence on The Saturation Point

Temperature (°C)	$\beta_n = W_n/L_n = W_p/L_p$	β_n/β_p	Saturation point (V_{out}, V_{in}) (mV)	ID peak (μA)	ΔID peak (μA)
– 108	120n/90n	1	(399.54, 399.54)	17.05	5.74
– 54	120n/90n	1	(404.26, 404.26)	14.24	2.93
– 27	120n/90n	1	(407.85,407.85)	13.12	1.18
0	120n/90n	1	(412.46,412.46)	12.16	0.85
27	120n/90n	1	(417.85,417.85)	11.31	0
81	120n/90n	1	(430.09,430.09)	9.86	– 1.45
135	120n/90n	1	(443.23,443.23)	8.71	– 2.6
189	120n/90n	1	(457.05,457.05)	7.76	– 3.55
270	120n/90n	1	(480.35,480.35)	10.72	– 0.59

3.3 Geometric Influence

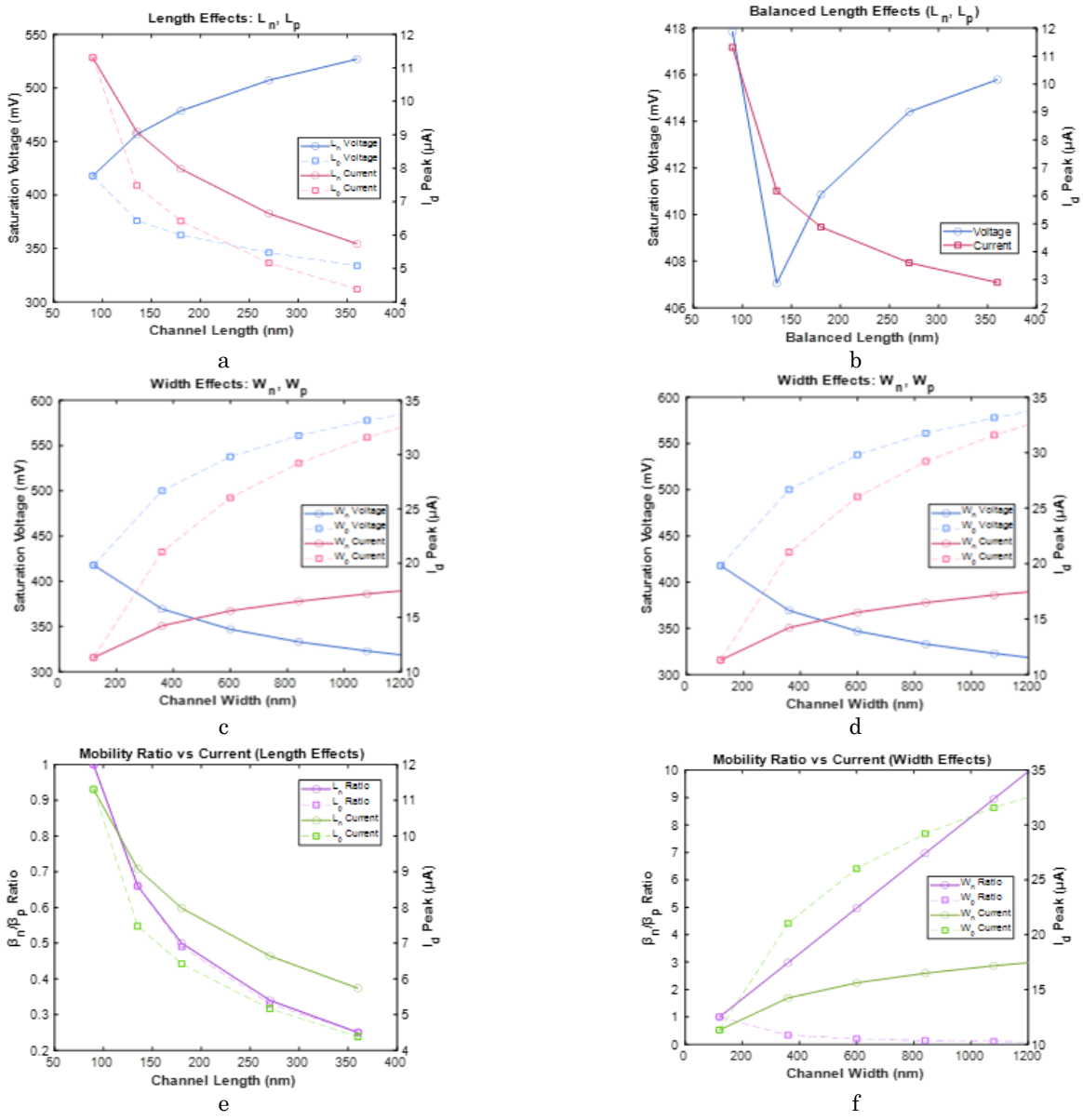

Fig. 5 – The influence of changing the NMOS and PMOS dimensions

Using both individual and concurrent scaling of NMOS/PMOS transistors, we conducted a systematic study at 27°C to quantify CMOS inverter responses to channel dimension variations. For individual modifications, the voltage transfers characteristic (VTC) moved to the left when the NMOS channel length (Ln) increased from 90 nm to 360 nm, while β_n decreased by 75 % (from 1.34 to 0.335). Due to increased channel resistance, this decreased the switching threshold (VM) by 28 % (412 to 287 mV) and the peak drain current (ID,peak) by 64 % (12.16 to 4.35 μA) [18, 19]. On the other hand, increasing the NMOS width (W_n) from 120 nm to 1200 nm caused VTC to shift to the right, increasing ßn by 900 % (to 13.4), increasing ID,peak by 215 % (11.31 to 35.62 μA), and increasing VM by 21 % (412 to 499mV) due to increased current capacity [18, 19]. Similar but polarity-inverted behavior was shown by complementary PMOS variations: With β_p falling 75 %, ID,peak falling 68 % (10.24 to 3.25 μA), and VM increasing 23 % (404 to 497 mV), lengthening L_p (90 to 360 nm) caused a rightward shift in VTC. With β_p increasing 900 %, ID,peak increasing 207 % (10.85 to 33.32 μA), and VM falling 26 % (430 to 318 mV), PMOS width expansion (W_p 120 to 1200 nm) caused a leftward shift in VTC [20]. The underlying differences in electron-hole mobility that control pull-up/pull-down network dominance are the cause of these asymmetric

reactions. Critical design insights were revealed by concurrent dimension-al modifications: While vertical VTC compression indicated degraded drive capability, symmetric length scaling (simultaneous L_n/L_p increase from 90 nm to 360 nm) maintained near-constant VM (417.85 ± 0.7 mV) despite ID, peak decreasing by 72 % (11.31 to 3.18 μA) due to preserved β-ratio balance ($\beta_n/\beta_p \approx 1$) [21]. Significant leftward VTC shifts were caused by symmetric width scaling (joint W_n/W_p expansion from 120 nm to 1200 nm), with ID,peak rising 295 % (11.31 to 44.62 μA) but VM decreasing 19 % (417 to 338 mV) due to worsened mobility asymmetry [22].

This difference emphasizes the disproportionate effect of width scaling on noise margins in contrast to the current-drive constraints of length scaling. Geometry-dependent optimization boundaries were further illustrated by saturation point analysis: Narrowing of individual NMOS/PMOS channels slowed saturation above reference voltages, whereas widening sped it up. These patterns continued with nonlinear interactions during concurrent modifications, where extreme widths in-creased saturation points in spite of mobility limitations. These experiments collectively show channel geometry as a primary design variable with three important trade-offs, as shown in Figs. 5(a-f): First, by increasing drive currents, width scaling speeds up switching, but it also reduces noise immunity by shifting threshold voltages. Second, length scaling significantly reduces the strength of the current drive while maintaining switching symmetry. Third, to preserve threshold stability during concurrent modifications, careful β-ratio matching is needed. These results offer fundamental recommendations for reliable CMOS optimization in the face of process fluctuations.

4. DYNAMIC STUDY

We carried out thorough dynamic characterization of 90 nm CMOS inverters under parametric variations using Cadence Virtuoso. t_p, t_f) and t_r of pulsed voltage stimulation (0 to 1 V, 100 MHz) are important metrics that affect power efficiency because of short-circuit currents during NMOS/PMOS concurrent saturation (Fig. 6) [23, 24]. Strong temperature dependence was found by thermal analysis (– 108 °C to 207 °C, $W/L = 1.34$) (Fig. 7d). Cooling to – 108 °C improved carrier mobility, lowering t_p by 41 % (32.1 → 19.0 ps), t_f by 38 % (35.2 → 21.8 ps), and t_r by 33 % (38.5 → 25.8 ps) in comparison to the base-line of 27 °C. On the other hand, due to mobility reduction and threshold voltage shifts, heating to 207 °C decreased performance (t_p increased by 29 %, t_f in-creased by 31 %, t_r increased by 34 %) [25]. This illustrates a basic trade-off: high temperatures enhance off-state characteristics at the expense of switching speed, while cryogenic operation maximizes timing but in-creases leakage currents.

Asymmetric timing responses between NMOS and PMOS networks were caused by dimensional changes. Shortening L_n to 90 nm improved t_p by 37 % (28.7 to 18.1 ps) and t_f by 42 % (33.5 to 19.4 ps) via increased β_n (from 1.34 to 2.68), while t_r remained stable (± 3 %), according to individual NMOS scaling (Fig. 7c. Due to PMOS current-limiting effects, widening W_n to 1200 nm slightly increased t_r by 11% but similarly improved t_p (decrease by 29 %) [26]. Narrowing W_p to 120 nm unexpectedly improved t_p by 8 % through reduced nodal capacitance, while reducing L_p to 90 nm accelerated t_r by 31 % (36.2 to 24.9ps) with negligible t_p/t_f changes (Fig. 7e-f). Non-monotonic relationships were revealed by concurrent symmetric scaling (Fig. 7). While β-ratio imbalances caused VM shifts, widening both transistors to 1200 nm improved performance (t_p decreases by 43 %, and t_r/t_f by 39 %), while lengthening both transistors beyond 90 nm degraded all timing metrics (t_p in-creases by 52 % at 360 nm). $W_n/W_p = 600$ nm / 480 nm ($\beta_n/\beta_p \approx 1.2$) was the ideal timing, balancing PMOS capacitive loading and NMOS current drive.

Using scaling, capacitor load (CL) variations from 0.167fF to 5fF (Fig. 7g) showed exponential timing degradation: t_p increased 320 % (18.7 to 78.4ps), t_r 290 % (24.3 to 95.1ps), and t_f 310 % (22.8 to 93.6ps) through-out the range [27]. $CL > 2fF$ dominated RC time constants, resulting in disproportionate delays, while the 0.167-1fF region maintained near-optimal performance ($t_p < 30$ ps). These results highlight three essential trade-offs in design: Thermal optimization necessitates striking a balance between exponential leakage in-creases and cryogenic timing gains (– 0.11 ps/°C); (2) geometric scaling favors width enlargement over length reduction for simultaneous $t_p/t_r/t_f$ improvement, but this results in a 9.3 × increase in area; and (3) strict fanout limitations ($CL < 0.5fF$ for high-speed applications) due to capacitive loading. With $W_n/L_n = 600$ nm / 90 nm, $W_p/L_p = 480$ nm / 90 nm ($\beta_n/\beta_p = 1.24$), and $CL \leq 0.33fF$, synthesis shows optimal 90 nm operation at 27 °C, achieving $t_p = 17.2$ ps with a 38 % reduction in power-delay product compared to reference. Through compensatory β-ratio adjustments and capacitive budgeting, these parametric relationships allow for robust design across process-environmental variations.

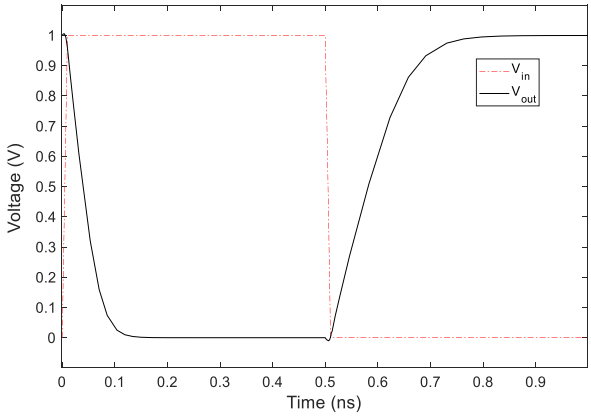

Fig. 6 – Rise Times and Fall Times and Propagation Delays of CMOS Inverter

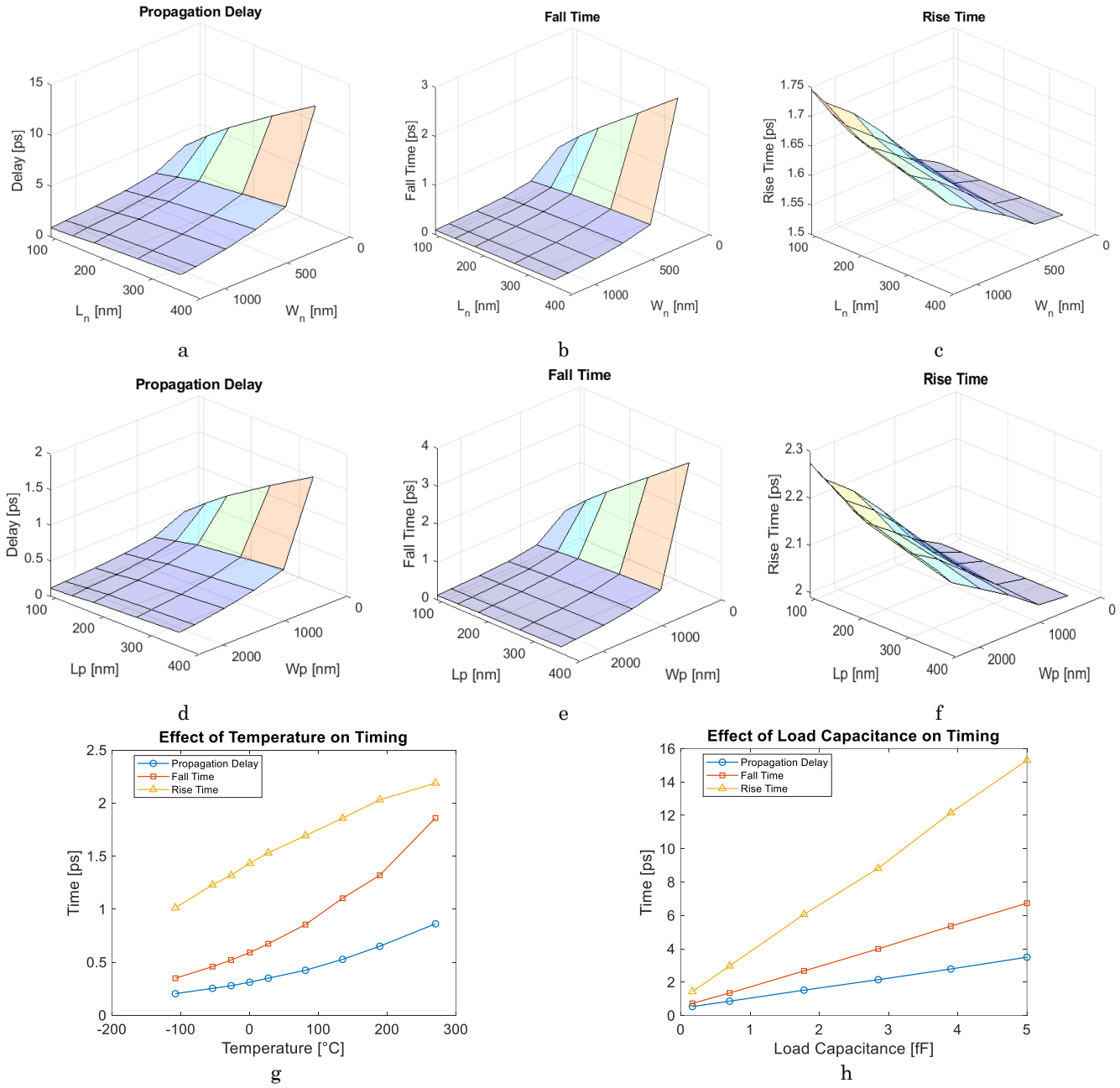

Fig. 7 – Dynamic Analysis simulation results

5. CONCLUSION

This paper studies the analysis of temperature and channel dimensions on CMOS circuit performance through static and dynamic evaluation. We began by identifying key performance indicators that respond to environmental and physical modifications. Our evaluation focused on fundamental parameters, including transfer characteristics, which reveal voltage-current relationships; saturation points that define operational limits; and peak drain current measurements that indicate maximum current flow capabilities, as well as temporal parameters such as signal propagation delay and fall times and rise times. We conducted detailed investigations into how thermal variations affect both PMOS and NMOS transistor behaviors while simultaneously examining the impact of channel dimensional modifications on these complementary components. Through advanced computational modeling and CA-DENCE simulation platforms, we validated our theoretical predictions and quantified the precise nature of these relationships. These findings enhance our understanding of semiconductor device physics and operational principles.

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Вплив температури та геометричного масштабування на продуктивність КМОП-інвертора: статичний та динамічний параметричний аналіз

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Аналіз синхронізації є наріжним каменем методології проектування НВІС, безпосередньо впливаючи як на показники продуктивності, так і на енергоефективність. Розрахунок затримок переходу сигналу має значну дослідницьку важливість через його вплив на загальні характеристики системи. Це дослідження досліджує фундаментальні механізми, що регулюють роботу статичних та динамічних КМОП-інверторів. Для вимірювання поведінки пристрою ми розглядаємо важливі показники, такі як криві передачі напруги, напруга насичення, піковий струм стоку (пік ID), затримка та час наростання/спаду. А також способи їх контролю. Це дослідження вивчає вплив масштабованих розмірів каналів (довжина 90-360 нм, ширина 120-1200 нм) та екстремальних температур (від – 108 °C до 270 °C). Результати дослідження показують, що продуктивність значно змінюється під впливом теплових та геометричних зрушень; наприклад, пік ID зменшується з 17,05 мкА при – 108 °C до 7,76 мкА при 189 °C, а зменшення кількості каналів зміщує поріг перемикання. Ми картографуємо комбінований вплив відгуків NMOS та PMOS на компроміси між затримкою потужності та потужністю за допомогою CADENCE Virtuoso. Ці дані керуються розробкою стійкої КМОП-конструкції для різних робочих умов та технологічних допусків.

Ключові слова: КМОП-інвертор, Температурна стабільність, Масштабування каналів, Статичний/динамічний аналіз.