Journal of Nano- and Electronic Physics
Vol. **17** No 5, 05008(4pp) (2025)

Журнал нано- та електронної фізики
Том **17** № 5, 05008(4cc) (2025)

OPEN ACCESS

REGULAR ARTICLE

An Analytical Method for Determination of Threshold Voltage of Surrounded Channel Junctionless Field Effect Transistor

N. Das* ✉, K.C.D. Sarma, R. Swargiary

Department of Instrumentation Engineering, Central Institute of Technology, Kokrajhar, India

(Received 04 September 2025; revised manuscript received 25 October 2025; published online 30 October 2025)

The advent of nanotechnology has significantly influenced the development of advanced transistor architectures, such as the Junctionless Field Effect Transistor (JLFET). Among various designs, mainly surrounded channel Junctionless field effect transistor (SCJLFET) is a structure without junction where the gate is placed inside the body of the device or in other words the gate is surrounded by the channel region. In a device based on MOS structure the most important parameter is the threshold voltage. This paper presents a comprehensive analytical method for determining the threshold voltage (Vth) of the surrounded channel Junctionless FET (SCJLFET). For a Junctionless field effect transistor (JLFET) the thresh-old voltage can be explained as the maximum value of gate voltage at which the value of the depletion width exactly equals to the thickness of the Si region. If the value of the gate voltage is above the value of the threshold voltage, the depletion width value is less than the thickness of the Si region then the device is turned on. The threshold voltage model for double gate JLT has also been obtained from the depletion width model. In this paper it is presented that the novel model SCJLFET exhibits much better characteristics compared to other conventional structure, incorporating key design parameters such as channel length, work function, drain voltage, gate oxide thickness, dielectric constant of gate dielectric and temperature. The threshold voltage model has been simulated in MATLAB simulation environment. Result obtained in the simulation work in MATLAB has been compared with the simulation result obtained from TCAD.

Keywords: JLFET, Surrounded channel, Threshold voltage, TCAD.

DOI: 10.21272/jnep.17(5).05008 PACS number: 85.30.Tv

1. INTRODUCTION

The ever-increasing demand for miniaturized and energy-efficient electronic devices has driven the development of novel transistor designs. JLFETs eliminate traditional source/drain junctions, simplifying fabrication and reducing short-channel effects. The surrounded channel JLFET, characterized by a channel encircling the gate, enhances gate control over the channel potential, making it a promising candidate for future technology nodes. The foundational insights into the proper-ties and design considerations of Junctionless nanowire transistors, highlighting their potential for scaling and reduced fabrication complexity in [1]. Further, [2] elaborated on the physics and operating principles of these devices, cementing their role in emerging low-power and high-performance nano systems. Different configurations studies of Junctionless transistors, including double-gate (DG) and surrounded-gate architectures. In [3] the analog and RF performance of surrounded-gate Junctionless graded-channel MOSFETs, demonstrating their improved stability and suitability for modern electronic applications are investigated. Analytical models for long channel DG JLFETs are developed in [4, 5], incorporating bulk current behavior and quantum effects in the sub threshold region. Short-channel effects, which challenge the scalability of transistors, have been a focus of several studies. In [6] A novel approach to model threshold voltage and subthreshold current of graded-doped junctionless-gate-all-around has been reported, while Chiang [7] proposed a quasi-two-dimensional threshold voltage model to account for these phenomena. Threshold-voltage variability in DG JLTs [8], emphasizing the impact of fabrication-induced variations. The sensitivity of device performance to structural parameters, such as nanowire width and doping profiles explored in [9, 10]. Further refinements in device modelling include the introduction of advanced doping profiles and material configurations. An analytical model for DGJLFETs with a vertical Gaussian-like doping profile [11], offering improved control over threshold voltage. Threshold voltage model development of N+ pocket vertical junctionless TFET (V-JL-TFET) as a label free biosensor analyzed in [12]. The threshold voltage of

* Correspondence e-mail: n.das@cit.ac.in

Cite this article as: N. Das et al., *J. Nano- Electron. Phys.* 17 No 5, 05008 (2025) https://doi.org/10.21272/jnep.17(5).05008

nanotube-based JLFETs, emphasizing the role of core-and-outer gate interactions examined in [13]. Research on surrounded-channel Junctionless field-effect transistors (SCJLFETs) has also progressed significantly. Extensively contribution [14-18] to this domain by modelling channel potential, resistance-based drain current, and depletion width, and analysing their high-power performance. SCJLFET exhibits comparatively higher I_{on}/I_{off} ratio, lower sub threshold swing and higher threshold voltage than a conventional JLFET. Their work demonstrated the versatility of SCJLFETs in power electronics and inverter circuits. These studies underscore the importance of surrounded-channel designs in enhancing device stability and scalability. Simulation studies have further validated these theoretical findings. The [19] conducted simulations on raised source-drain DGJLFETs, high-lighting their potential to mitigate short-channel effects and improve device reliability and [20] extended these investigations to analyze the performance of SCJLFETs in specific applications, such as full-bridge inverters. Collectively, this paper illustrates the advancements in modelling, design, and application of Junctionless transistors. The shift from traditional junction-based devices to Junctionless architectures, particularly in double-gate and surrounded-channel configurations, presents a promising avenue for next-generation electronic devices. Threshold voltage (V_{th}) plays a pivotal role in determining the device's switching characteristics and overall performance. Although numerical simulations provide accurate V_{th} estimates, analytical methods offer deeper physical insight and computational efficiency. This paper develops an analytical approach to determine the threshold voltage of the surrounded channel JLFET. The objective of the paper is to obtain a fully analytical mathematical model for the threshold voltage of a SCJLFET. The analytical model helps designers to design the required device with minimum time.

2. METHODOLOGY

This paper uses an analytical method to study the variation of threshold voltage with various parameters of proposed novel structure SCJLFET. SCJLFET offered multi threshold voltages such as low, regular and high threshold voltage as compared with the MOSFET. Conventional JLFET exhibits lower threshold voltage as compared to the surrounded channel JLFET.

3. SIMULATION SETUP

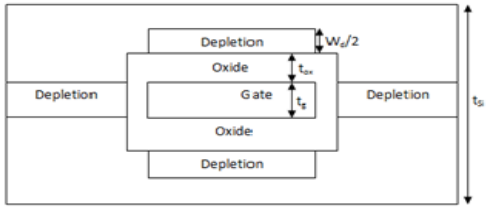

Fig. 1 – 2-D view of a SCJLFET

The surrounded channel JLFET features a cylindrical channel that is uniformly doped and entirely gate is encircled by a channel. It is a novel structure which is proposed to combine both single as well as double gate structure by placing the complete gate circuit inside the body as shown in the Fig. 1. This configuration pro-vides enhanced electrostatic control over the channel, making it particularly suitable for nanoscale device designs. The gate is separated from the channel by a thin oxide layer, which ensures effective modulation of the channel potential to simplify the analytical modeling. The device operates in full depletion mode near the threshold voltage, and quantum mechanical effects are neglected, which is a reasonable approximation for channel dimensions above a few nanometers. This structure which is termed as Surrounded channel JLFET offered multi threshold voltages such as low, regular and high threshold voltage as compared with the MOSFET. Conventional JLFET exhibits lower threshold voltage as compared to the surrounded channel JLFET. The SCJLFET model is valid for both short channel and long channel condition. The validation of threshold voltage indirectly validates the depletion region also.

4. DETERMINATION OF THRESHOLD VOLTAGE

The threshold voltage (V_{th}) is defined as the gate voltage required to induce complete depletion of the channel. At the threshold, the surface potential reaches a value that depletes the channel of free carriers. The boundary condition at the silicon-oxide interface is applied to determine the gate voltage. Threshold voltage of SCJLFET is higher for thinner gate oxide. For obtaining the threshold voltage of the device depletion width model considering depletion approximation has been taken as the reference. To obtain a suitable positive threshold voltage value at ultra-short channel length, high doping concentration is required and the gate oxide and channel region should be very thin. Validation of the depletion width model also depends on the validation of the threshold voltage model. Thus for SCJLFET the gate oxide should be thin for high thresh-old and thick for low threshold voltage.

5. RESULTS AND DISCUSSION

This paper illustrates a physics based model for threshold voltage of a Junctionless transistor which has been developed. The SCJLFET model developed has been simulated in Matlab simulation environment. The analytical model for determining the threshold voltage of the surrounded channel JLFET was evaluated and validated through comparison with TCAD simulation results. Result obtained in the simulation work has been compared with the simulation result obtained from Cogenda visual TCAD 2D device simulator. The model demonstrates high accuracy, with less than 5% deviation from the numerical simulations. The comparisons are shown in the figures as shown below.

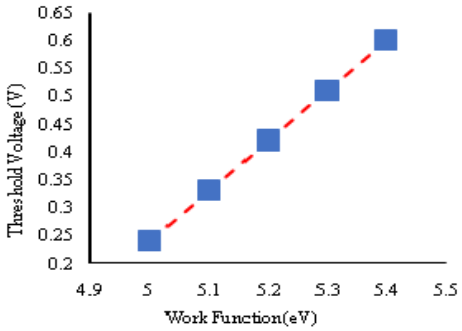

Fig. 2 – Variation of threshold voltage with work function

Fig. 2 shows the variation of threshold voltage with work function. In the figure it shows the threshold voltage increases almost linearly with work function. If value of the work function increases, then threshold voltage (V_{TH}) also increases with decrease in the drain voltage and increase of the gate to source voltage occurs. Fig. 3 shows the variation of threshold voltage with drain voltage. In the figure it is observed that threshold voltage decreases linearly with increase in the drain voltage and it is due to increase in the gate to source voltage.

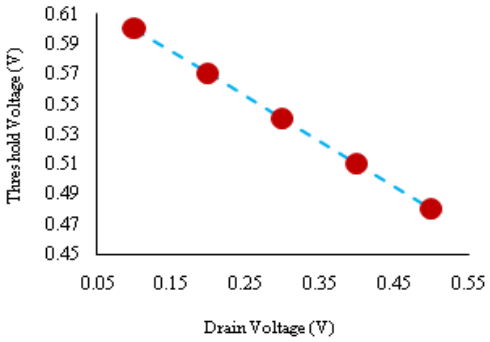

Fig. 3 – Variation of threshold voltage with drain voltage

Fig. 4 shows the variation of threshold voltage with gate oxide thickness. From the figure it is clear that gate loses control over the channel region for thicker gate oxide. To achieve a suitable positive threshold voltage value at a short channel the gate oxide and channel region should be very thin. The model is in close agreement with TCAD simulation results.

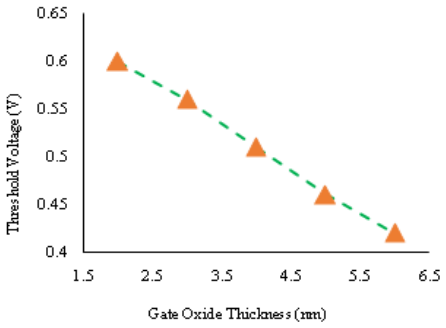

Fig. 4 – Variation of threshold voltage with gate oxide thickness

Fig. 5. shows the variation of threshold voltage with Dielectric constant of Gate Dielectric. It has been observed that the value of the dielectric constant of gate dielectric varies with different variables of the thresh-old voltage. According to the figure it seems that value of the threshold voltage increases as compare to the different values of the dielectric constant of Gate Dielectric. It further illustrates that the performance of the model is in true agreement with the TCAD simulation work results.

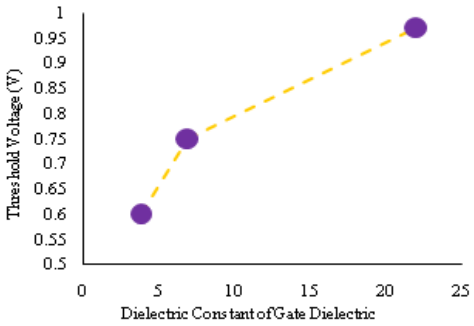

Fig. 5 – Variation of threshold voltage with Dielectric con-stant of Gate Dielectric

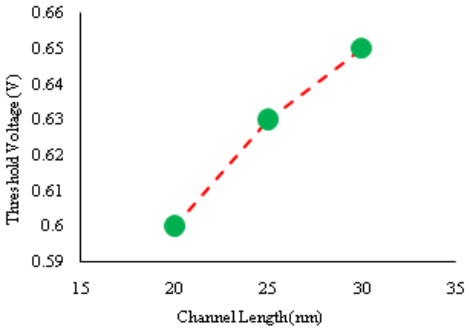

Fig. 6 – Variation of threshold voltage with channel length

Fig. 6 shows the variation of the threshold voltage with channel length of the device. From the figure it has been observed that for shorter device the threshold voltage is less and for long channel length threshold voltage increases.

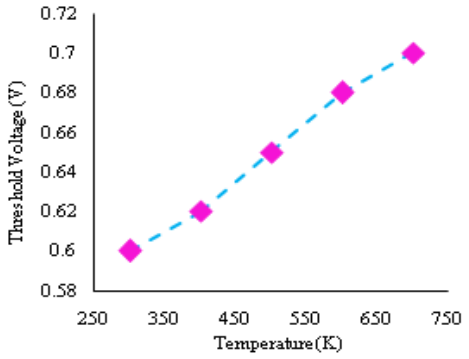

Fig. 7 – Variation of threshold voltage with different ranges of temperature

Fig. 7 shows the variation of threshold voltage with different ranges of temperature. From the figure it has been observed that with increase in temperature, threshold voltage also increases. Due to the changes in the value of the threshold voltage regardless changes in the gate to source voltage variation in the temperature occurs.

6. CONCLUSION

This paper presents a robust analytical method for determining the threshold voltage of surrounded channel JLFETs. This approaches offers a deeper under-standing about the behavior of threshold voltage variation with other parameters of surrounded channel JLFET, making it a valuable tool for device engineers and researchers. The study showed that SCJLFET exhibits higher threshold voltage as compared with the conventional transistor. By providing a reliable framework for threshold voltage estimation, this method lays a solid foundation for the optimization of these devices, ensuring their potential for low-power, high-performance applications in future semiconductor technologies. Result obtained has been compared with the simulation result obtained from Cogenda visual TCAD 2D device simulator.

REFERENCES

1. J.-P. Colinge, et al. *Solid-State Electron.* **65-66**, 33 (2011).
2. J.-P. Colinge, *Emerging Devices for Low-Power and High-Performance Nanosystems* (Jenny Stanford Publishing), 2 (2018).
3. S. Misra, et al., *Silicon* **14**, 6391 (2022).
4. J.-P. Duarte, et al., *IEEE Electron. Dev. Lett.* **32** No 6, 704 (2011).
5. J.-P. Duarte, et al., *IEEE Trans. Electron Dev.* **59** No 4, 1008 (2012).
6. V. Gupta, et al., *Silicon* **14**, 2989 (2022).
7. Te-K. Chiang, *IEEE Trans. Electron Dev.* **59** No 9, 2284 (2012).
8. C.-Yu Chen, J.-T. Lin, M.-H. Chiang, *Microelectron. Reliab.* **74**, 22 (2017).
9. S.-J. Choi, et al., *IEEE Electron Dev. Lett.* **32** No 2, 125 (2010).
10. R.D. Trevisoli, et al., *Semicond. Sci. Technol.* **26** No 10, 105009 (2011).
11. B. Singh, et al., *IEEE Trans. Electron Dev.* **63** No 6, 2299 (2016).
12. P. Raut, D.K. Panda, *Microelectron. J.* **151**, 106331 (2024).
13. N. Kumar, et al, *Microelectron. J.* **113**, 105104 (2021).
14. N. Das, K.C.D. Sarma, *J. Nano- Electron. Phys.* **16** No 5, 05004 (2024).
15. N. Das, K.C.D. Sarma, *J. Nano- Electron. Phys.* **16** No 4, 04002 (2024).
16. N. Das, K.C.D. Sarma, *J. Nanoelectron. Optoelectron.* **17** No 2, 211 (2022).
17. N. Das, K.C.D. Sarma, *2020 International Conference on Computational Performance Evaluation (ComPE)*, 608 (2020).
18. N. Das, K.C.D. Sarma, *2020 International Conference on Computational Performance Evaluation (ComPE)* (2020).
19. K.C.D. Sarma, D. Deka, R. Swargiary, *2023 4th International Conference on Computing and Communication Systems (I3CS)*, 1 (2023).
20. N. Das, K.C.D. Sarma, *Discov. Electron.* **1**, 12 (2024).

Аналітичний метод визначення порогової напруги на безперехідному польовому транзисторі із закритим каналом

N. Das, K.C.D. Sarma, R. Swargiary

Department of Instrumentation Engineering, Central Institute of Technology, Kokrajhar, India

Поява нанотехнологій суттєво вплинула на розвиток передових архітектур транзисторів, таких як безперехідний польовий транзистор (JLFET). Серед різних конструкцій, переважно оточений канальний безперехідний польовий транзистор (SCJLFET) – це структура без переходу, де затвор розміщений всередині корпусу пристрою або, іншими словами, затвор оточений областю каналу. У пристрої на основі МОН-структури найважливішим параметром є порогова напруга. У цій статті представлено комплексний аналітичний метод визначення порогової напруги (Vth) оточеного канального безперехідного польового транзистора (SCJLFET). Для безперехідного польового транзистора (JLFET) порогову напругу можна пояснити як максимальне значення напруги затвора, при якому ширина збіднення точно дорівнює товщині Si-області. Якщо значення напруги затвора вище значення порогової напруги, значення ширини збіднення менше товщини Si-області, тоді пристрій вмикається. Модель порогової напруги для подвійного затворного JLT також була отримана з моделі ширини збіднення. У цій статті представлено, що нова модель SCJLFET демонструє значно кращі характеристики порівняно з іншими традиційними структурами, включаючи ключові параметри конструкції, такі як довжина каналу, робота виходу, напруга стоку, товщина затворного оксиду, діелектрична проникність затворного діелектрика та температура. Модель порогової напруги була змодельована в середовищі моделювання MATLAB. Результати, отримані в результаті моделювання в MATLAB, були порівняні з результатами моделювання, отриманими за допомогою TCAD.

Ключові слова: JLFET, Закритий канал, Порогова напруга, TCAD.