Journal of Nano- and Electronic Physics
Vol. **17** No 4, 04035(5pp) (2025)

Журнал нано- та електронної фізики
Том **17** № 4, 04035(5cc) (2025)

OPEN ACCESS

REGULAR ARTICLE

Design and Implementation of Charge Plasma Based Dopingless MBCFET Using Ultrathin Ge for Low Power Application

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(Received 15 May 2025; revised manuscript received 21 August 2025; published online 29 August 2025)

This work introduces a novel strategy to enhance electron mobility by leveraging an Ultrathin Pure Si/Ge/Si Substrate within a Charge Plasma-Based Dopingless Multi-Bridge Channel MOSFET. By integrating ultra-thin pure Ge layers with charge plasma-driven multi-bridge channel architecture, the proposed approach maximizes carrier transport efficiency. By using charge plasma concept, the chemical doping difficulties are reduced for sub nano meter devices.The device design involves the direct deposition of ultra-thin Ge crystal layers onto a bulk Si wafer, integrated with multiple bridge channels to improve MOSFET performance. The findings highlight notable improvements, including enhanced electron mobility, minimized hysteresis, and superior *I-V* characteristics. This integrated methodology ensures precise gate control, optimized carrier dynamics, and overall superior transistor performance, paving the way for next-generation semiconductor advancements. Given that transistors serve as the cornerstone of semiconductor technology, their evolution has significantly contributed to the miniaturization and efficiency of modern electronic systems. A comprehensive analysis of carrier dynamics was conducted using the Lombardi mobility model, complemented by Shockley-Read-Hall (SRH) and Auger recombination mechanisms to account for minority carrier recombination. Inverter and 6T SRAM analysis have been done. The both inverter, read and write comparison results shows the better performance when Ge is incorporated in between silicon material.

Keywords: Charge Plasma, MBCFET, SRAM, Inverter.

DOI: 10.21272/jnep.17(4).04035 PACS numbers: 82.33.Xj, 85.40. – e

1. INTRODUCTION

The introduction serves as a gateway to the research, providing a broad perspective on semiconductor technology and its evolution. It traces the transition from conventional silicon-based devices to innovative material and structural advancements, highlighting the challenges that drive the search for alternative solutions. This section establishes the motivation behind the proposed system, emphasizing the necessity for continual progress in semiconductor technologies. A brief overview of the subsequent chapters is provided, setting the stage for an in-depth exploration of the research [1].

Semiconductor devices form the foundation of modern electronics, enabling the functionality of countless systems that define contemporary life. These devices, predominantly composed of silicon due to its availability and desirable electrical characteristics, exhibit the unique capability to selectively conduct electrical current – an essential trait that underpins their widespread applications [2-5]. At the core of semiconductor technology lies the transistor, a revolutionary component that amplifies and switches electronic signals. The advent of transistors marked a turning point in electronics, leading to the development of smaller, more efficient, and high-performance devices. Over the years, relentless advancements have fueled semiconductor innovation, driven by the pursuit of miniaturization, enhanced efficiency, and superior functionality. Semiconductor devices encompass a diverse range of components, including diodes, which permit unidirectional current flow; transistors, which serve as amplifiers or switches; and integrated circuits (ICs), which consolidate numerous components onto a single chip. Cutting-edge developments have given rise to sophisticated technologies such as field-effect transistors (FETs), metal-oxide-semiconductor field-effect transistors (MOSFETs), and complementary metal-oxide-semiconductor (CMOS) systems. These innovations continue to push the boundaries of semiconductor capabilities, propelling advancements in computing, communication, and various other fields [7-10].

The relentless drive for smaller, faster, and more energy-efficient semiconductor devices fuels ongoing research and development. As we navigate the complexities of semiconductor technology, we unveil the remarkable innovations that power the digital era, transforming industries and reshaping the technological landscape. From fundamental components like diodes and transistors to intricate ICs housing billions of transistors, semiconductor evolution remains at the forefront of modern electronics [11-15].

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Cite this article as: S.A. Kumar et al., *J. Nano- Electron. Phys.* 17 No 4, 04035 (2025) https://doi.org/10.21272/jnep.17(4).04035

2. DEVICE STRUCTURE

A junctionless transistor has been designed and simulated in Sentaurus TCAD using predefined parameters. During the evaluation, the gate-to-source voltage (V_{GS}) and drain-to-source voltage (V_{DS}) were maintained at 1.3 V and 1.5 V, respectively. The structure comprises a Junctionless (JL) Multi-Channel transistor with two channels, each having a width of 20 nm, a length of 1000 nm, and a thickness of 10 nm. An inter-oxide layer of 40 nm separates the stacked channels. The source, drain, and channel regions were uniformly doped with a concentration of 2×10^{17} cm^{-32}. Hafnium dioxide (HfO_2) was utilized as the gate oxide and inter-oxide material, while silicon dioxide (SiO_2) was used for the buried oxide layer [16].

The device architecture features two stacked channels divided by an inter-oxide layer. The presence of this inter-oxide layer leads to different gating effects: Channel 2 is surrounded on three sides, effectively forming a Tri-Gate structure, whereas Channel 1 is enclosed on only two sides, functioning as a Double-Gate configuration. Additionally, a buried metal layer (BML) is introduced between Channel 1 and the buried oxide layer, establishing a Schottky junction at the BML/*n*-Si interface, defined by the barrier height ΦBM > ΦSi,where ΦSi represents the work function of n-doped silicon. The barrier height is determined by the difference between the work function of the buried metal and the electron affinity of silicon, facilitating controlled charge carrier transport.

To enhance current drive while maintaining a compact footprint, multiple bridge channels can be vertically stacked within the same gate, source, and drain configuration. Multi-Bridge Channel MOSFETs (MBCFETs) leverage this design to optimize performance. Metal nitrides such as TiN, TiSiN, TaN, and TaCN are incorporated due to their high thermal stability. After high-temperature annealing, these materials exhibit work functions ranging from 4.4 eV to 4.7 eV, influenced by factors such as layer thickness, alloy composition, crystal orientation, and the gate dielectric. While metal nitrides are not optimal for planar CMOS, they prove highly suitable for low-power, multi-gate CMOS applications.This concept is closely linked to the photoelectric effect, where metal-semiconductor junctions play a crucial role. The work function of the metal, along with the semiconductor's electron affinity, determines the Schottky barrier height, directly influencing charge carrier flow across the interface. The integration of such material and structural innovations drives advancements in next-generation semiconductor technology[17-19].

Figure 1 illustrates the formation of the Buried Metal Layer (BML) within the semiconductor structure, achieved through the Charge Plasma concept by doping a p-type semiconductor material. This buried metal layer induces a depletion region at the bottom of the device, creating a Schottky junction with a carefully chosen work function (ΦBM). While the source–channel–drain path remains junctionless, the resulting architecture is termed the Buried-Metal-SOI Lateral Junctionless Transistor (BM-SOI-LJLT). The combined effect of the BML-induced bottom depletion region and the top-gate-controlled depletion ensures complete volume depletion in the OFF state, significantly enhancing device performance. The Mental Length is 1 nm, Source is 15 nm, Gate measures 30 nm and the Gate thickness is 4 nm, while the Oxide thickness is 1.5 nm. The Metal thickness is 5 nm, and finally, the Channel thickness is 0.5 nm.

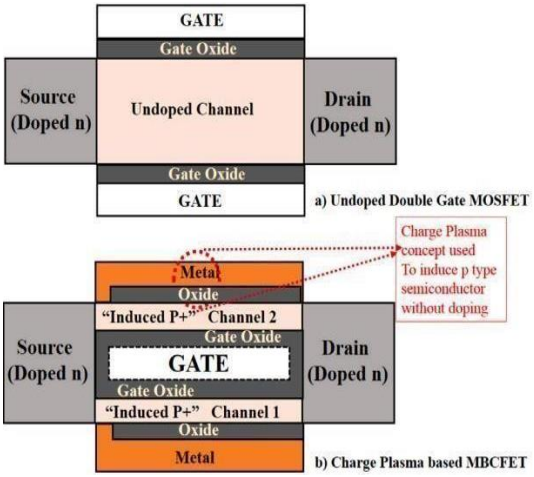

Fig. 1 – Multichannel in a junction-less thin film transistor

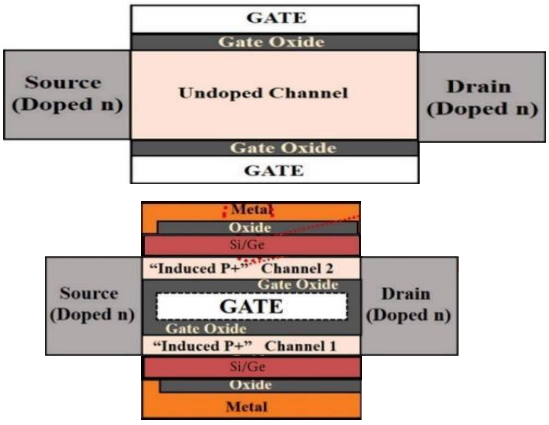

Fig. 2 – Proposed structure

The work functions of the metal materials used in the BML typically range between 4.4 eV and 4.7 eV after undergoing high-temperature annealing. This range is influenced by factors such as alloy composition, crystal orientation, gate dielectric material, and layer thickness.A crucial component of this device is the gate oxide, an insulating layer that electrically separates the gate terminal from the underlying source, drain, and conductive channel. This oxide layer is formed via thermal oxidation of the silicon channel, resulting in a thin (5-200 nm) layer of silicon dioxide (SiO_2). The oxidation process follows the Deal-Grove Model, which describes the self-limiting nature of SiO_2 growth. Once the gate oxide is established, a conductive gate material is deposited over it to complete the transistor structure. The gate oxide plays a pivotal role in modulating the channel's conductivity, sustaining transverse electric fields as high as 1 to 5 MV/cm to effectively control charge carrier flow. To assess the device's performance, semiconductor processing techniques were meticulously simulated, as illustrated in Figure 2. A comprehensive analysis of carrier dynamics was conducted using the Lombardi mobility model, complemented by Shockley-

Read-Hall (SRH) and Auger recombination mechanisms to account for minority carrier recombination. These simulations offer valuable insights into the electronic properties of the device, reinforcing its viability for next-generation semiconductor applications [20].

3. RESULTS AND DISCUSSION

The Sentaurus Visual plot illustrates the transient response of an inverter circuit, capturing the dynamic interplay between input and output voltage waveforms over time. The graph distinctly showcases the inversion behaviour, where the output voltage (depicted by the yellow and light blue curves) transitions in opposition to the input voltage (represented by the dark blue and purple curves). The input signals exhibit sharp transitions resembling a square wave, while the output signals display a slight delay along with characteristic rise and fall times – hallmarks of the inverter's switching properties. The presence of multiple input-output curves suggests variations in simulation parameters or device configurations, resulting in subtle differences in transition slopes and propagation delays. Despite these variations, the consistent inversion behaviour reinforces the inverter's core functionality, while the observed differences underscore the influence of specific parameters on the circuit's dynamic performance. This visualization effectively highlights the temporal relationship between input and output signals, offering valuable insights into the inverter's switching speed, signal propagation, and overall response characteristics.

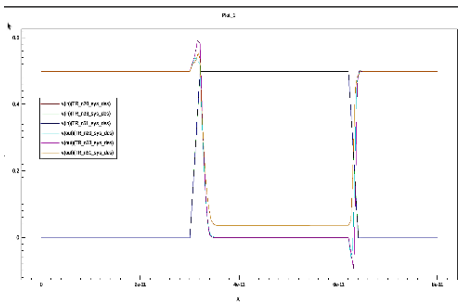

Fig. 3 – Transfer characteristics of MBCFET before and after the absorption of gas molecules

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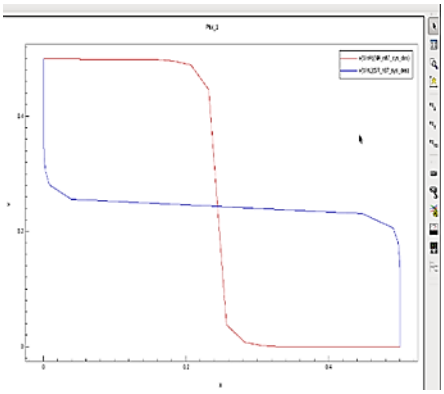

Fig. 4 – SRAM read circuit analysis

The provided graph illustrates the Voltage Transfer Characteristics (VTCs) during an SRAM read operation, highlighting the differential outputs v(VinR) and v(VinL). The distinct curves demonstrate the bistable behaviour inherent to an SRAM cell, where the outputs settle into two well-defined stable states corresponding to logic '0' and '1'.

The sharp transitions in the VTCs indicate high gain, a critical factor for robust switching and noise immunity. The separation between the two output curves, particularly in the transition region, underscores the cell's ability to generate a differential signal – essential for reliable read operations. Additionally, the graph pinpoints the switching threshold, marking the point at which the outputs shift between stable states. Beyond SRAM behaviour, the work function is a fundamental property influencing electron emission and absorption at metal-semiconductor interfaces. Defined as the energy difference between the Fermi level (which determines the probability of electron presence at a given energy in a metal at thermal equilibrium) and the vacuum level, it plays a pivotal role in establishing the energy barrier at these junctions. The Sentaurus Visual plot presents the Voltage Transfer Characteristics (VTCs) of an SRAM write operation, highlighting the differential outputs v(VinR) and v(VinL) throughout the writing process. The graph illustrates how the SRAM cell transitions from its initial state to a new state in response to input voltage variations. The distinct trajectories of v(VinR) and v(VinL) reflect the cell's ability to switch between two stable states, a fundamental aspect of binary data storage. The sharp transitions in the VTCs indicate high gain, enabling rapid state changes essential for fast and efficient write operations. The divergence of the curves in the transition region emphasizes the differential nature of the write process, where a voltage difference between the two outputs dictates the cell's final state.

Additionally, the observed slopes and transition points define the switching thresholds, providing insight into the write dynamics of the SRAM cell. This VTC analysis reinforces the cell's effectiveness in securely storing data

by shifting between distinct voltage levels, ensuring reliable performance in memory applications

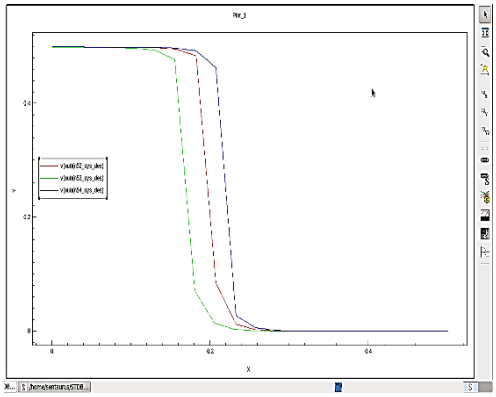

Fig. 5 – Inverter circuit

4. CONCLUSION

In conclusion, this study introduces an innovative approach to overcoming electron mobility challenges in metal-oxide-semiconductor field-effect transistors (MOSFETs). By integrating ultrathin pure germanium (Ge) layers onto a silicon (Si) substrate and implementing the Charge Plasma-Based Dopingless Multi-Bridge Channel MOSFET design, significant advancements have been achieved. The demonstrated improvement in electron mobility marks a crucial breakthrough with substantial implications for semiconductor device performance. Leveraging the superior electron transport properties of ultrathin Ge layers, this research successfully addresses the limitations of conventional silicon-based MOSFETs, paving the way for faster and more efficient electronic devices.

ACKNOWLEDGEMENTS

The Authors are grateful to the Kalasalingam Academy of Research and Education (KARE) management for providing TCAD laboratory facilities for this research.

REFERENCES

1. J.P. Colinge, C.W. Lee, A. Afzalian, N.D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'neill, A. Blake, M. White, A.M. Kelleher, *Nat. Nanotechnol.* **5** No 3, 225 (2010).
2. K.W.Ang, K.J. Chui, V. Bliznetsov, A. Du, N. Balasubramanian, M.F. Li, G. Samudra, Y.C. Yeo, *IEDM Technical Digest. IEEE International Electron Devices Meeting*, 1069 (2004).
3. Y. Liu, O. Gluschenkov, J. Li, A. Madan, A. Ozcan, B. Kim, T. Dyer, A. Chakravarti, K. Chan, C. Lavoie, I. Popova, *IEEE Symposium on VLSI Technology*, 44 (2007).
4. Z. Ren, G. Pei, J. Li, B.F. Yang, R. Takalkar, K. Chan, G. Xia, Z. Zhu, A. Madan, T. Pinto, T. Adam, *IEEE Symposium on VLSI Technology*, 172 (2008).
5. V.V. Kozlovski, A.E. Vasil'ev, V.V. Emtsev, G.A. Oganesyan, A.A. Lebedev, *J. Surf. Invest.* **13** No 6, 1155 (2019).
6. T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, *IEEE International Electron Devices Meeting*, 11 (2003).
7. T. Mizuno, N. Sugiyama, T. Tezuka, Y. Moriyama, S. Nakaharai, T. Maeda, S. Takagi, *IEEE Digest of Technical Papers. Symposium on VLSI Technology*, 202 (2004).
8. A.A. Toropov, O.G. Lyublinskaya, B.Y. Meltser, V.A. Solov'ev, A.A. Sitnikova, M.O. Nestoklon, O.V. Rykhova, S.V. Ivanov, K. Thonke, R. Sauer, *Phys. Rev. B: Condens. Matter.* **70** No 20, p205314 (2004).
9. C.H. Ge, C.C. Lin, C.H. Ko, C.C. Huang, Y.C. Huang, B.W. Chan, B.C. Perng, C.C. Sheu, P.Y. Tsai, L.G. Yao, C.L. Wu, *IEEE International Electron Devices Meeting*, 3 (2003).
10. M. Hasan, *PhD thesis* (2011).
11. A. Pal, A. Sarkar, *Eng. Sci. Technol. Int. J.* **17** No 4, 205 (2014).
12. G.V. Reddy, M.J. Kumar, *IEEE Trans. Nanotechnol.* **4** No 2, 260 (2015).
13. M.T.B. Kashem, S. Subrina, *Int. J. Numer. Modell. Electron. Networks. Dev. Field.* **32** No 1, e2476 (2019).
14. J.C. Pravin, D. Nirmal, P. Prajoon, J. Ajayan, *Physica E* **83**, 95 (2016).
15. S.A. Kumar, J.C. Pravin, *J. Nano- Electron. Phys.* **13** No 1, 01005 (2021).
16. H. Lou, L. Zhang, Y. Zhu, X. Lin, S. Yang, J. He, M. Chan, *IEEE Trans. Electron Dev.* **59** No 7, 1829 (2012).
17. V.R. Samoju, P.K. Tiwari, *Int. J. Numer. Modell. Electron. Networks Dev. Field.* **29** No 4, 695 (2016).
18. Y.R. Lin, Y.Y. Yang, Y.H. Lin, E.D. Kurniawan, M.S. Yeh, L.C. Chen, Y.C. Wu, *IEEE J. Electron Dev. Soc.* **6**, 1187 (2018).
19. S. Ashok Kumar, J.C. Pravin, *IETE J. Res.* **69** 2615 (2023).
20. http://www.sentaurus.dsod.pl/manuals/data/sdevice_ug.pdf.

Розробка та впровадження безлегуючого MBCFET на основі зарядової плазми з використанням надтонкого Ge для низькопотужних застосувань

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У цій роботі представлено нову стратегію підвищення рухливості електронів шляхом використання надтонкої чистої підкладки Si/Ge/Si в багатомостовому канальному MOSFET-транзистори на основі зарядової плазми без легування. Завдяки інтеграції надтонких шарів чистого Ge з багатомостовою архітектурою каналів, керованою зарядовою плазмою, запропонований підхід максимізує ефективність транспортування носіїв заряду. Використовуючи концепцію зарядової плазми, труднощі хімічного легування зменшуються для субнанометрових пристроїв. Конструкція пристрою включає пряме осадження

надтонких шарів кристалів Ge на об'ємну кремнієву пластину, інтегровану з кількома мостовими каналами для покращення продуктивності MOSFET. Результати дослідження підкреслюють помітні покращення, включаючи покращену рухливість електронів, мінімізований гістерезис та чудові вольт-амперні характеристики. Ця інтегрована методологія забезпечує точне керування затвором, оптимізовану динаміку носіїв та загальну покращену продуктивність транзисторів, прокладаючи шлях для досягнень наступного покоління напівпровідникових технологій. Враховуючи, що транзистори є основою напівпровідникової технології, їх еволюція значно сприяла мініатюризації та ефективності сучасних електронних систем. Було проведено комплексний аналіз динаміки носіїв заряду з використанням моделі рухливості Ломбарді, доповненої механізмами рекомбінації Шоклі-Ріда-Холла (SRH) та Оже-рекомбінації для врахування рекомбінації неосновних носіїв. Було проведено аналіз інверторної та 6T SRAM. Результати порівняння інверторної, читальної та записуючої пам'яті показують кращу продуктивність, коли Ge включено між кремнієвим матеріалом.

Ключові слова: Плазмовий заряд, MBCFET, SRAM, Інвертор.