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REGULAR ARTICLE

Graphene Nanoribbon Based Asymmetric Tunnel FET for Fast Switching and Low Power Applications

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This research work mainly investigates the process of layering graphene material as ribbon structure at nano scale i.e. 0 – 2 nm and its outcome for asymmetric tunnel field effect transistor (TFET). Our proposed model i.e. Asymmetric Dual Gate TFET with graphene nano ribbon (ADG-GN-TFET) is designed based on modern quantum tunneling device physics approach, with hetero-structured oxide material, keeping channel length at 20 nm to perform at low power application suit-ably. Silvaco TCAD is used as software for generating the simulation results, which are further analyzed and compared with orthodox TFET models for identifying its uniqueness towards making it as a fast-switching semiconductor device. The various essential physical device parameters i.e. channel length, body thickness, oxide thickness are varied and tradeoff is applied in pursuit of better device performance. The entire simulation process is performed at 0.5 V of supply voltage. This ensures the proposed device model suitable for low power applications. The approach of layering graphene sheet can be modified according to the device model and its source, channel and drain electrode material combination at nano-scale up-to 20 nm. Turn on voltage is recorded at 0.22 V, keeping effective oxide thickness (EOT) as 2 nm. Also, the ambipolar i.e. leakage current is well controlled and best recorded as 6.86×10^{-14} A/μm.

Keywords: Graphene, TFET, TCAD, Nano-Ribbon, Quantum tunneling.

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1. INTRODUCTION

With the advent of nanotechnology, there are several nanodevices which are getting designed and simulated in pursuit of developing a semiconductor device at nano-scale [1]. Since more than a decade, Complementary Metal Oxide Semiconductors (CMOS) uses conventional CMOS device physics to build integrated circuits for practical applications. But due to restriction in low power applications as well as fast switching, the conventional device physics needed to change its approach, which further bring tunnel field effect transistors (TFET) into the modern semiconductor industry [2-10].

Because of its band-to-band-tunneling (BTBT) approach shown in Fig. 1, the modern device physics actually results a path breaking solution for developing low power nano-devices with fast switching compared to CMOS technology [11].

This quantum tunneling using Heisenberg uncertainty principle results high on-state current (I_{ON}) at low threshold voltage (V_{th}). Besides this the off-state current (I_{OFF}) is also matter of concern for better switching device at nano-scale [12].

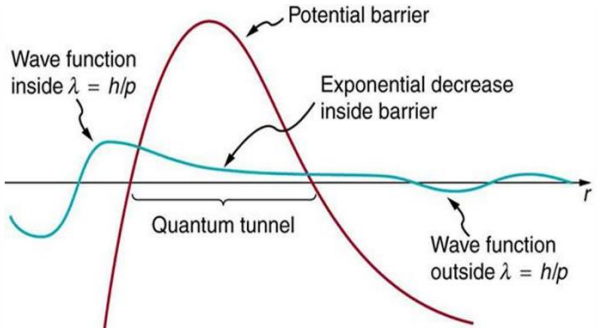

Fig. 1 – Quantum tunneling representing modern device physics compared to classical approach

2. PROPOSED DEVICE MODEL AT NANO SCALE

2.1 Asymmetric TFET with Heterogate

There has been an extensive survey of asymmetric TFETs at nano-scale, where the device model is altered based on potential applications viz. low power, fast

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switching, high frequency applications etc. Symmetry of the semiconductor device is missing because of desperate reformation of device lengths such as gate, source and drain electrode lengths. The reformation of device lengths is strictly analyzed and mathematically resolved based on following equation:

$$I_D = \frac{1}{2}\,\mu_n\,C_{ox}\,\frac{W}{L}\,(V_{GS} - V_t)^2 \qquad (1)$$

From Eq. (1) it can be clearly understood that overdrive potential (V_{OV}) is directly proportional to drain current i.e. on-state current. So, if V_{OV} decreases, I_{ON} also decreases and I_{OFF} increases, which is not desired. Therefore, a tradeoff between width of gate (W) and length of gate (L) is highly required, whereas electron mobility (μ_n) and oxide capacitance (C_{ox}) are also closely varied [13-14] and monitored for better device performance.

2.2 Use of Graphene as Nanoribbon over Proposed Device Model

Structure of the proposed device model is shown in Fig. 2. Here two different materials (Indium Arsenide: InAs and Silicon: Si) are used at source and drain regions respectively.

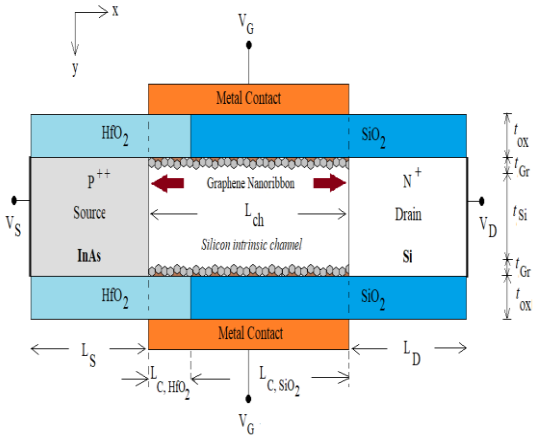

Fig. 2 – Proposed device model at nano-scale (0 – 20 nm)

The source is heavily doped compared to drain, moreover the sandwiched layer i.e. channel is the intrinsic region which is effectively less doped from both the previous regions. The graphene is actually a carbon allotrope having atoms of single layer. It is generally arranged as a planar structure, but here in this research, this carbon-based nano-material forming a 360° folding sheet, which eventually acted as nano-ribbon sheet, shown in Fig. 3.

As we can see that if the graphene planar sheet is replaced by nano-ribbon, where no energy band gap remain exists between conduction (C) and valence (V) bands. This in-turn increases probability of electron transfer between $V-C$ band to multiple times. This further results quantum tunneling and elevates ON state current compared to leakage current. Graphene material is also introduced for its very high electron carrier mobility with low effective mass at room temp. i.e. 273 K.

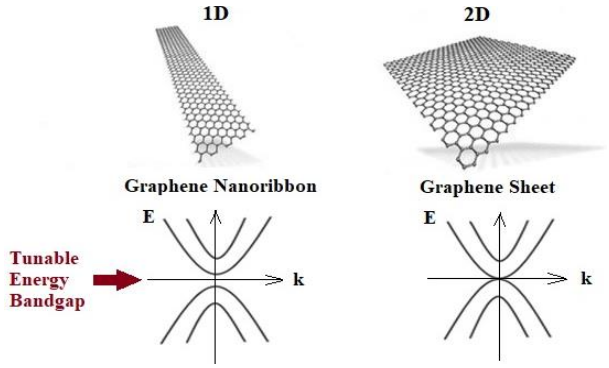

Fig. 3 – Graphene material is used as nano-ribbon in our proposed model

Another aspect of introducing graphene material is to utilize its high thermal conductivity at high thermal strength, that in-turn results better suitable device structure for low power applications.

2.3 Deployment of Device Parameters for Model Simulation

To obtain best device performance, the real balancing between selection of typical physical and electrical parameters is very important. This may be in varying doping concentration level or fixing gate or other electrodes lengths, which eventually help us to obtain suitable result for fast switching and low power application.

Table 1 – Physical & Electrical parameters used in this model

Sl. No.	Physical & Electrical parameters	Unit(s)
1.	Doping at source	4.5×10^{16} atoms/cm^3
2.	Doping at drain	1.5×10^{14} atoms/cm^3
3.	Doping at intrinsic channel	4×10^{12} atoms/cm^3
4.	Length (Gate: L_{ch})	0-20 nm
5.	Thickness (Body: t_{Si}), (Graphene: t_{Gr}), (Oxide: t_{ox})	10, 0.5, 2 (nm)
6.	Supply voltage (V_{DD})	0.5 V

TCAD device simulator [15] is used in solving simulation results and analysis done in this research work.

3. SIMULATION RESULTS

As this article majorly focuses on low power applications, therefore it is evident to showcase the important aspects of output current i.e. drain current as I_{ON} as well as leakage current i.e. I_{OFF} which plays pivotal role in low power application.

3.1 Leakage Current Control

The TFET with modified asymmetric structure always generates high *ON* state current in general due to its BTBT tunneling. But to get a reduced leakage current as we increase gate voltage is a real challenge that we faced during this process.

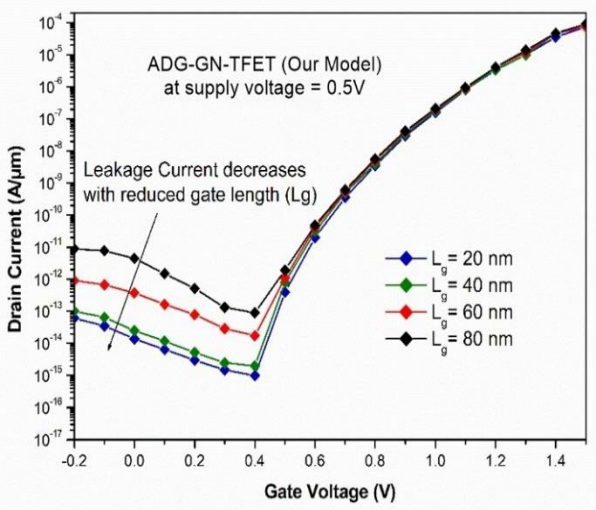

Fig. 4 – Leakage current is getting reduced with reduced channel / gate length

In Fig. 4, it is evident that the gate length (L_g) i.e. channel length (L_{ch}) is same, and trading off the scale from 80 nm to 20 nm, actually provides us better controlled leakage current which is one of the major plus point as far as low power operation is concerned. Our proposed model i.e. Asymmetric Dual Gate- Graphene Nano ribbon Tunnel FET (ADG-GN-TFET) is producing reduced leakage current with reduced channel/gate length of the device.

3.2 Better Turn ON Voltage

The variation of transistor body thickness from 16 nm to 10 nm, eventually helped us to achieve a better turn-*ON* voltage which is much needed for approaching towards a fast-switching device.

Keeping effective oxide thickness (EOT) i.e. t_{ox} at 2 nm with supply voltage at 0.5 V, the tradeoff value of 10 nm of body thickness results turn on voltage at 0.22 V, earlier it was 3.768 V, shown in Fig. 5.

3.3 EBD Analysis

The Energy Band Diagram (EBD) analysis at nano level gives reader an exact graphical representation of improved BTBT tunneling happening at source – channel junction, also at channel – drain junction, shown in Fig. 6 (a) and Fig. 6 (b).

At Fig. 6 (a) it is evident that the channel path window is getting narrower at source-channel inter junction at V_G = 1.5 V with supply voltage fixed as low as possible at 0.5V. Similarly, at Fig. 6 (b) we could find the shrinking of tunneling window at channel – drain junction using graphene sheet at V_G = – 1 V. Therefore, graphene plays pivotal role in controlling BTBT rate across the device, which further helps to yield better and fast switching device model.

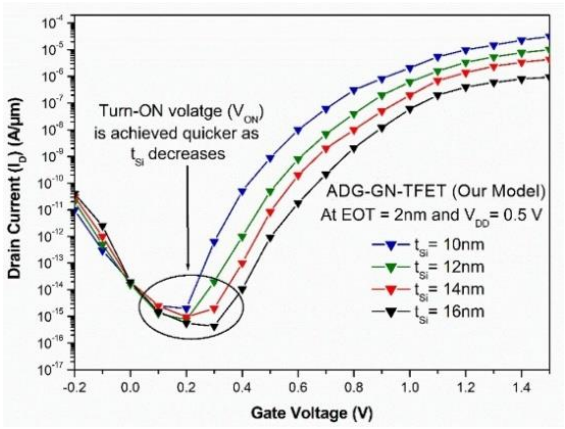

Fig. 5 – Varied body thickness (16-10nm) yields better Turn ON voltage

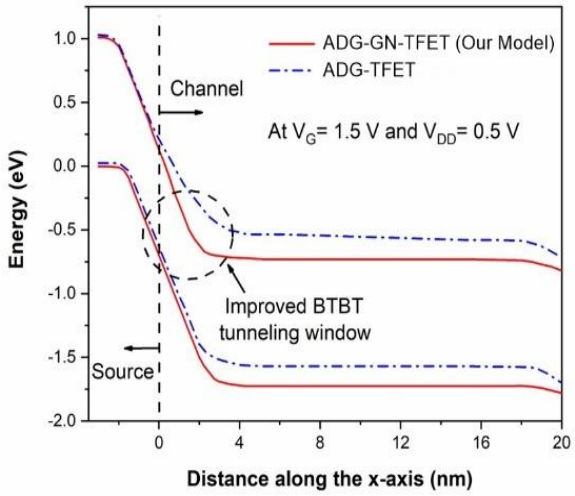

Fig. 6 (a) – BTBT tunneling improved at Source – Channel Junction in presence of graphene at nano scale (0-2nm)

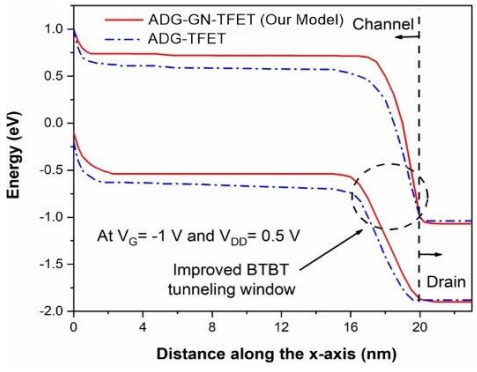

Fig. 6 (b) – BTBT tunneling improved at Channel – Drain Junction in presence of graphene at nano scale (0 – 2 nm)

3.4 Electric Field Distribution Analysis

After investigating the band diagram analysis, the very next crucial aspect is to study the electric field distribution majorly targeted along *x*-axis (lateral) and *y*-axis (vertical), shown in Figs. 7 (a) and 7 (b) respectively.

Here in this comparison study, the orthodox Symmetric Double Gate TFET (SDG-TFET), Asymmetric Dual Gate TFET (ADG-TFET) and our proposed model i.e. Asymmetric Dual Gate TFET (ADG-GN-TFET) have tested with electric field variation laterally and vertically, where in the lateral e-field distributed to its maxima at source – channel junction.

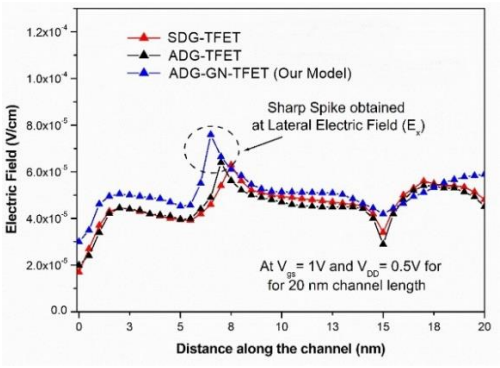

Fig. 7 (a) – Electric Field Distribution (lateral)

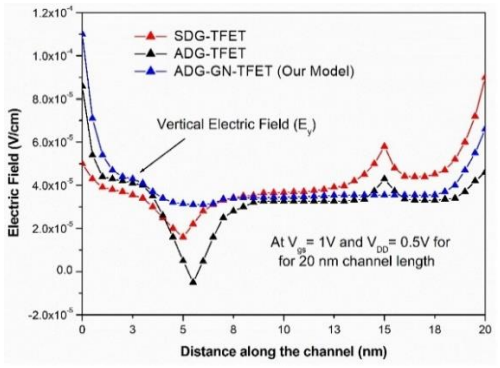

Fig. 7 (b) – Electric Field Distribution (vertical)

3.5 BTBT Rate Comparison Between Existing and Our Proposed Models

The BTBT rate with electric field distribution is studied keeping gate voltage at 0 to 1.5 V. Supply voltage is fixed at 0.5 V at this simulation process.

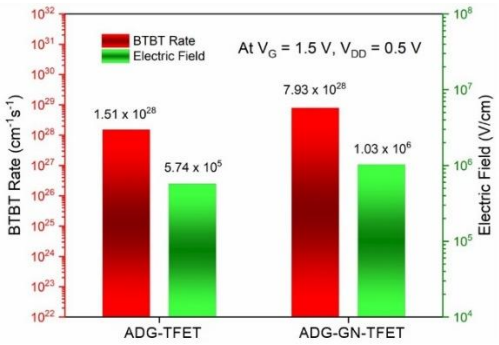

Fig. 8 – Tunneling Rate and E-Field Comparison

Fig. 8 shows a bar-chart comparison of BTBT rate and e-field distribution of asymmetric dual gate TFET with proposed model i.e. ADG-GN-FET. Due to the layering of graphene layer at S-Ch junction for n-channel TFET the spike at surface potential results high BTBT rate as well as e-filed that generated across the channel.

4. CONCLUSION AND FUTURE SCOPE

This research work mainly investigated the typical importance of graphene layer which is put over intrinsic channel as ribbon structure to enhance the switching current at S-C junction. This ensures the fast switching of the proposed model. Moreover, the graphene material helps to grow the induced e-field grows considerably at tunneling region, that also controls the ambipolar current i.e. leakage current as the gate voltage increases, keeping supply voltage fixed at min of 0.5 V. This ensures the proposed device model suitable for low power applications.

The approach of layering graphene sheet can be modified according to the device model and its source, channel and drain electrode material combination at nano-scale up-to 20 nm. Turn on voltage is recorded at 0.22 V, keeping EOT as 2nm. Also, the ambipolar i.e. leakage current is well controlled and recorded as 6.86×10^{-14} A/μm at channel length at 0 – 20 nm.

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REFERENCES

1. R. Sharma, A.K. Sharma, S. Sharma, P. Sharma, *Nanoelectronics: Physics, Materials and Devices*, 159 (2023).
2. P.K. Kumawat, S. Birla, N. Singh, *Mater. Today: Proc.* **79** No 2, 292 (2023).
3. W.Y. Choi, B.G. Park, J.D. Lee, T. Liu, *IEEE Electron Dev. Lett.* **28** No 8, 743 (2007).
4. R. Dutta, N. Paitya, *Int. J. Innovative Technol. Explor. Engg.* **8** No 10, 393 (2019).
5. R. Dutta, N. Paitya, T.D. Subash, *Silicon* **13**, 719 (2021).
6. I.C. Cherik, S. Mohammadi, *IEEE Trans. Electron Dev.* **70** No 2, 801 (2023).
7. F. Najam, Y.S. Yu, *IEEE Trans. Electron Dev.* **66** No 4, 2010 (2019).
8. R. Dutta, S.C. Konar, N. Paitya, *Comp. Adv. Comm. Circ. Syst.* **575** (2020).
9. M.A. Khanday, F.A. Khanday, F. Bashir, F. Zahoor, *IEEE Trans. Nanotechnol.* **22**, 430 (2023).
10. B. Zohmingliana, B. Choudhuri, B. Bhowmick, *IEEE Trans. Consum. Electron.* **70** No 1, 167 (2024).
11. M. Ehteshamuddin, A.G. Alharbi, S.A. Loan, *Conf. Proc. Elec. Electron. Eng.*, 224 (2018)
12. Z. Zhang, X. Shi, A. Wu, D. Li, *IEEE Signal Proc. Lett.* **28**, 1665 (2021).
13. R. Dutta, T.D. Subash, N. Paitya, *J Comput. Electron* **20**, 855 (2021).
14. T.K. Agarwal, A. Nourbakhsh, P. Raghavan, I. Radu, S.D. Gendt, M. Heyns, *IEEE Electron Dev. Lett.* **35** No 12, 1308 (2021).
15. J.K. Mamidala, R. Vishnoi, P. Pandey, *Tunnel Field-effect Transistors (TFET): Modelling and Simulation*, 163 (2017).

Графенова нанострічкова асиметрична тунельна ТТ для швидкого перемикання і низького енергоспоживання

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У цій роботі розглядається процес нанесення графену у вигляді нанострічки (0 – 2 нм) для створення асиметричного тунельного транзистора з польовим керуванням (TFET). Запропоновано модель ADG-GN-TFET (Asymmetric Dual Gate Graphene Nanoribbon TFET), розроблену за принципами квантового тунелювання з використанням гетероструктурованих оксидів та каналу довжиною 20 нм для забезпечення низького енергоспоживання. Симуляції виконано у середовищі Silvaco TCAD, а результати порівняно з традиційними моделями TFET з метою виявлення переваг. Змінювалися параметри як-от довжина каналу, товщина тіла, товщина оксиду, що дозволило знайти оптимальні характеристики для швидкодіючого перемикання. Усі моделювання здійснено при напрузі живлення 0.5 В, а напруга включення (V_{on}) склала 0.22 В при ефективній товщині оксиду (EOT) 2 нм. Особливо варто відзначити низький рівень паразитного струму (амбіполярного), який становив 6.86×10^{-14} А/мкм, що свідчить про ефективне придушення витоків.

Ключові слова: Графен, TFET, TCAD, Нанострічка, Квантове тунелювання.