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REGULAR ARTICLE

Reduction of Common-Mode Voltage Using Novel T-Type Multilevel Inverter for EV Application

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MLIs are very important and essential for controlling the power at medium voltage and very high power. A new T-type MLI based on the pulse width modulation method has been presented in this paper. A five-level voltage and a minimum common-mode voltage are the main circuit's objectives. A design layout and its corresponding output for the proposed system design are included in this article to test its effectiveness and feasibility. The proposed research seeks to enhance the implementation of a multistate switching cell in the PWM signals given to the gate signals of the MOSFETs. To obtain the five levels of voltage output with a lower common-mode voltage. Thus, the losses are reduced and the Efficiency is increased in the inverter. The total number of semiconductor switches is also reduced. This suggested inverter is simulated using Matlab/Simulink application software. The suggested architecture maintains excellent efficiency and dependable operation while reducing the number of switching components. Simulation findings verify the suggested inverter configuration, showing that it can accomplish reliable and effective power conversion for medium-voltage and high-power applications, the novel T-type MLI structure provides an affordable and scalable solution. The reduced common mode voltage will reduce the circulating bearing current problems in the application of induction motor drive.

Keywords: Multilevel inverter, Efficiency, MOSFET, Common mode voltage, Losses.

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1. INTRODUCTION

Converters with high performances and the least size working under low levels of voltages are increasing steadily year by year. The use of a passive component to reduce the sizing and weight of the circuit may lead to an increase in switching frequency of around 10-25 kHz. It may also reduce the losses during switching operations and enhance the efficiency of the system [1-3]. New technology in semiconductors like Sic-based diodes is understudied in the recent scenario. It's not economical and hence, the most practical option for industrial and commercial applications is still the most standard IGBT technology. Multilevel inverters have provided a very effective method that offers the requisite maximum efficiency, and maximum output voltage system stability, as well as smaller passive component size. Application is in wind turbine systems [4-5].

Although two-level topologies remain the standard industry norms for applications requiring low voltage. Recently it can be seen that 3-level MLI circuits have better solutions for applications that work for minimum voltage combined with the switching frequencies range of medium to maximum range which is efficient and economical. The field of application is medium-voltage ac drives [6-8].

Researchers compared two levels and three levels of NPC for a better understanding of the converter efficiency in high-frequency applications. A bidirectional switch is used by a 3-level of *T*-type inverter for controlling the voltage in the dc-link when compared to the five-level NPC [9-10]. In the literature, various multilayer topologies derived from traditional NPC inverters have been devised. The 3LT2I system has the combined advantage of two and three-level inverters, for example, simple and effective operating principle, minimum switching and conduction losses, and high output voltage performance [11–13]. For switching frequencies between 4 and 30 kHz, the efficiency of 3LT2I is exceptional [14]. The 3LT2I system cannot output an ac voltage larger than the input dc-link voltage because it has voltage buck functionality.

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To satisfy economic expectations and improve design complexity, a DC-DC (boost) converter is typically implemented before and during the inverter in real-world practical applications, like systems]. A closed-loop system has an easy time controlling speed and an ongoing feedback loop process. This approach can be used to get the necessary speed. The dual closed-loop system is the closed-loop system used in this case. A new pulse width modulation-based T-type MLI has been proposed and developed. The suggested circuit offers a lower common-mode voltage and 5 levels of voltage. A design layout and its output waveform for the prototype are provided in this article to test its effectiveness and feasibility. Section 2 provides information on the suggested terminology analysis. Section 3 describes the explanation of the common-mode voltage reduction. Section 4 explains the simulation findings and discussion. In section 5, the proposed work finally ended with some conclusions.

2. ANALYSIS OF THE PROPOSED 5-LEVEL INVERTER

The need for this suggested work is to enhance the multistate switching cell application in the PWM signals are given to the gate signals of the MOSFETs. To get the 5- levels in the voltage output with having the reduced common-mode voltage. Thus, the losses are reduced and the Efficiency is increased in the inverter. The total number of semiconductor switches is also reduced [22-24]. A 5-level T-type topology is shown in Fig. 1. S1-S8 are eight bidirectional controlled switches (MOSFET). N1 and N2 windings solely on a single autotransformer. The voltage levels of this suggested inverter are + Vin/4, + Vin/2, 0, – Vin/4, – Vin/2. The suggested architecture is made up of eight MOSFET switches, two RC filters, a linear transformer, and an R Load [25-27].

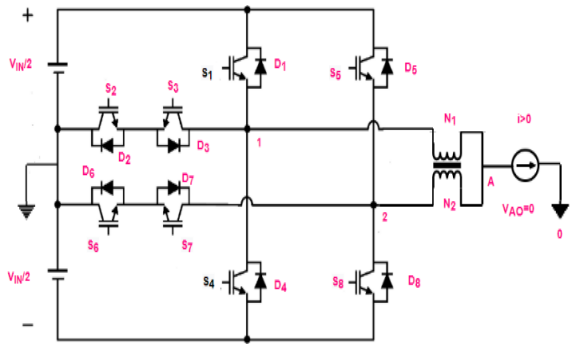

Fig. 1 – 5- Level T-type topology

Two groups of four-four MOSFETs each have been formed. The MOSFETs are supplied with power through filters, and also the transformer serves as an isolation device in between the R load and the switches. The output voltage is obtained across the switch's connection. To find the common-mode applied voltage in the circuit, we connect one terminal of the voltage measurement block to one end of the resistor and the other terminal to the ground. Fig. 2 shows the proposed T-Bridge 5 level Topology [28-30].

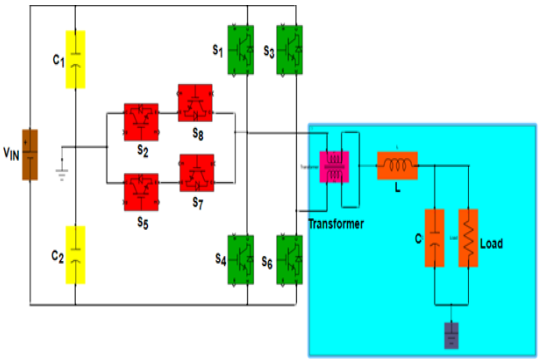

Fig. 2 – Proposed *T*-bridge 5 Level Topology

The waveform is of five levels in the obtained output voltage graph. The common-mode applied voltage during both inputs must be reduced. The common-mode applied voltage is introduced either through the noise induced in the cable or transmitted from a cable. To ensure electromagnetic conductivity, the common-mode voltage should be reduced. The common-mode applied voltage present in the suggested inverter that must be reduced by phase width modulation techniques. A phase-width modulation control scheme is often referred to as a pulse duration modulation control scheme. This type of technique may result in the reduction of average power that has been delivered over chopping the data (signal) into many data in discrete nature. Table 1 shows the switching sequence state for the Proposed T-bridge 5 Level Topology.

Table 1 – Switching Sequence table

S.No	Stage1	Stage2	Stage3
Switch 1	0	0	1
Switch 2	1	1	0
Switch 3	1	1	0
Switch 4	0	1	1
Switch 5	0	1	1
Switch 6	1	0	0
Switch 7	1	0	0
Switch 8	0	0	0

3. COMMON MODE VOLTAGE REDUCTION

The positive level and negative level modes of operation are analyzed for a five-level modified *T*-bridge topology. The voltage obtained between the ground and the load is referred to as the common-mode voltage in *T*-type technology and depends on the different control switching states. Sinusoidal waves and triangular waves or carrier waves are compared and the received output is used as input gate pulses for the switches. The innovative technique of PWM is applied to get the reduced common mode applied voltage. The simulation analysis is done by using the MATLAB/SIMULINK software and thus, the evaluated voltage, and current output is shown below. We are getting a reduced common-mode voltage. Fig. 3a and 3b depict the positive and negative levels of the common mode voltage.

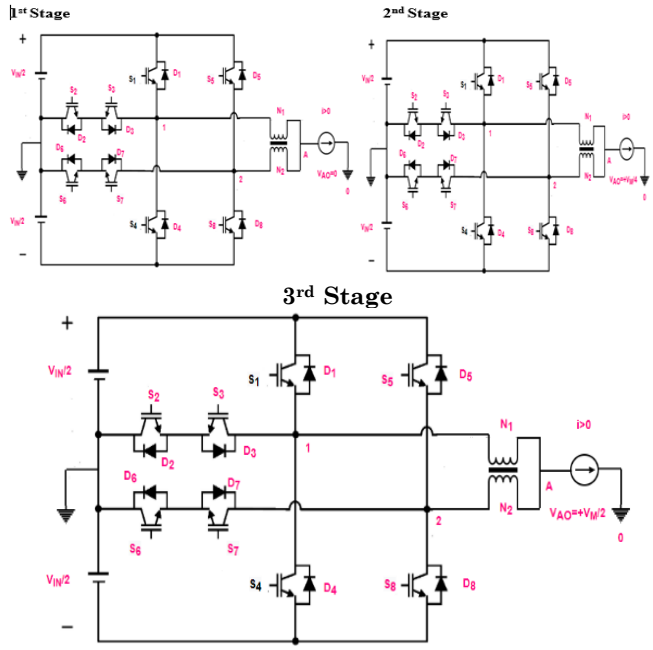

Fig. 3a – Positive level 3 stages

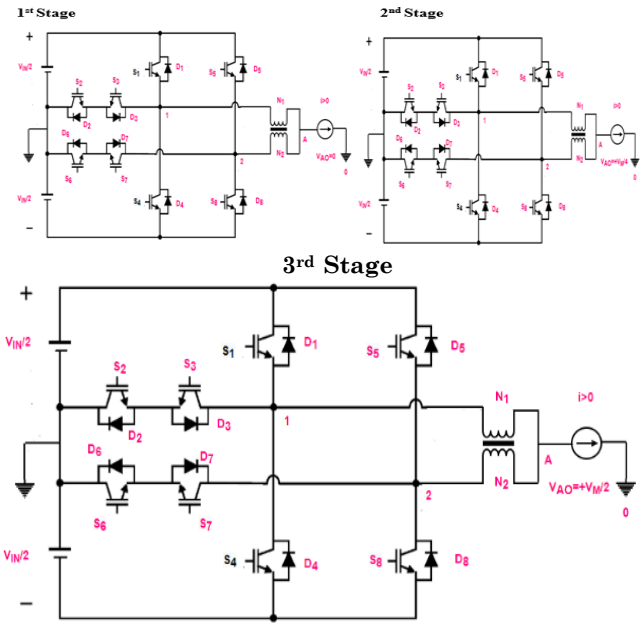

Fig. 3b – Negative level 3 stages

Method 1: **Phase Disposition methods**: Here, the triangular carrier waves are in phase. Gate voltages supply is given to the following connections of switch 1, switch 2, switch 5, and switch 6 using the upper carrier signals. Hence, the lower carrier signals supply the gate voltages to the following connections of switch 3, switch 4, switch 7, and switch 8.

Method 2: Phase Opposition Disposition methods: The triangular carrier signal waves present in the phase disposition method are of phase shift of 180° present in the out of phase. Thus, the upper carrier message

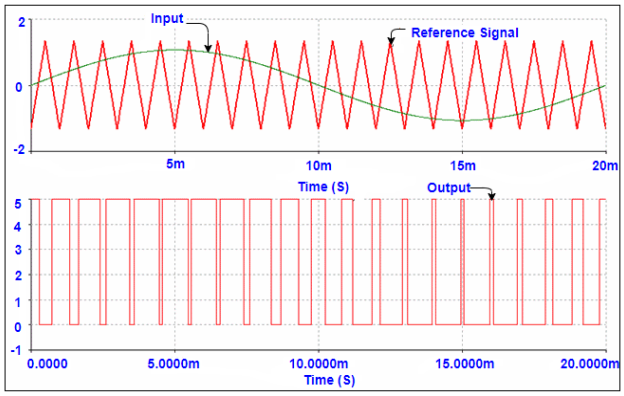

Fig. 4 – Applied PWM technique

signals are used to supply gate voltages to the following connections of switch 1, switch 2, switch 5, and switch 6. Hence, the lower carrier signals supply gate voltages to the following connection of switch 3, switch 4, switch 7, and switch 8. Carrier signals supply the gate voltages to the following connection of switch 3, switch 4, switch 7, and switch 8.

4. RESULTS AND DISCUSSION

The output analysis of the proposed 5-level multilevel inverter by using the MATLAB simulation is shown below. The initial output is 400 V.

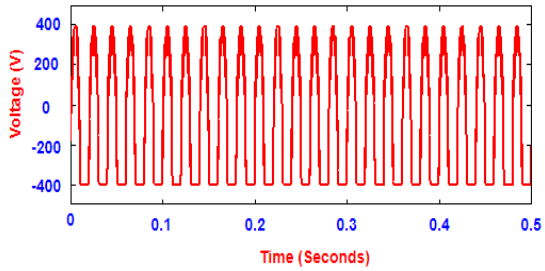

Fig. 5 – Initial Output voltage

The common mode voltage before applying the reduction technique in MATLAB simulation is as given in the Figs. 5 and 6 and the Initial common mode voltage is 400 V.

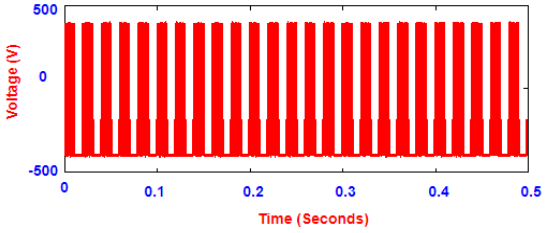

Fig. 6 – Initial Common-Mode Voltage

4.1 PD Method CMV

Using this proposed technique common-mode voltage for 400 V input is 20 V as depicted in Fig. 7. In the conventional PD technique, the common-mode voltage for

400 V input is 60 V as shown in Fig. 8. The proposed PD method has reduced common-mode voltage compared to a conventional method.

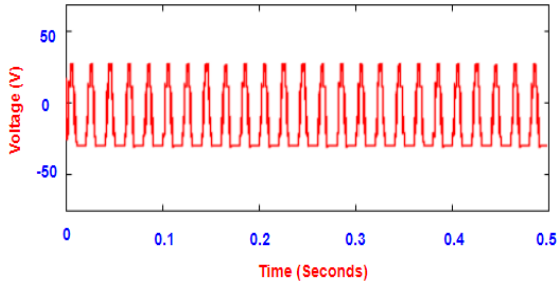

Fig. 7 – CMV –Proposed PD Method

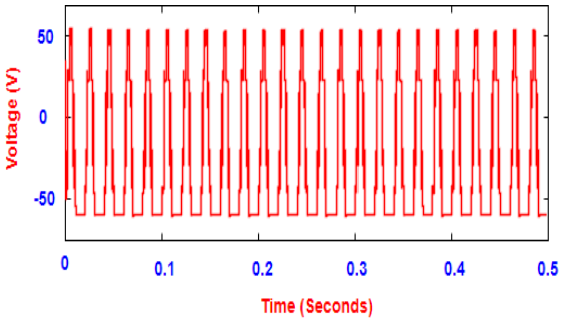

Fig. 8 – CMV – Conventional PD Method POD Method

4.2 POD Method

Using this proposed technique common-mode voltage for 400 V input is 14 V as depicted in Fig. 9. In the conventional PD technique, the common-mode voltage for 400 V input is 32 V as shown in Fig. 10. Thus, the suggested PD approach has reduced common-mode applied voltage compared to the conventional method is shown in the Fig. 10. Table 2 shows the statistical analysis of PD and POD method.

Table 2 – Statistical Analysis of PD and POD Method

Common Mode Voltage	Before Reduction	POD		PD	
		Conventional Method	Proposed Method	Conventional Method	Proposed Method
	400	32	14	60	20

The table's summary of the data shows how well the suggested approach performed in lowering the Common

Mode Voltage (CMV) under the two modulation strategies of Phase Opposition Disposition (POD) and Phase Disposition (PD) when compared to the traditional method. The CMV is 400 units prior to reduction, which suggests a significant degree of noise and possible interference. Regarding the POD methodology, the traditional approach achieves an 88 % reduction in CMV, bringing it down to 32. The CMV is further reduced to 14 by the suggested

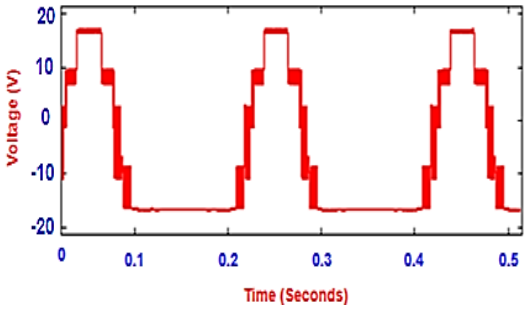

Fig. 9 – CMV-proposed POD Method

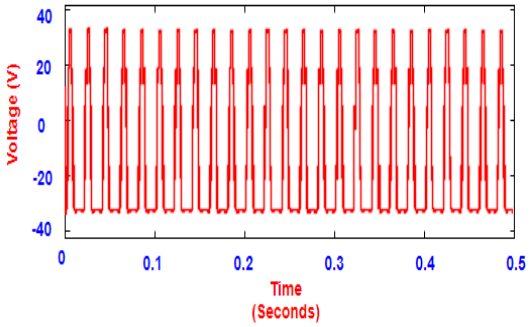

Fig. 10 – CMV-conventional POD Method

method, a 96.5 % reduction that is noticeably superior to the traditional approach. Regarding the PD methodology, the traditional approach achieves an 85 % reduction by bringing the CMV down to 60. The suggested approach results in a 95 % decrease, or a reduction to 20. The suggested strategy has fewer trade-offs and lower CMV values than techniques reported in earlier research. For example, the suggested method provides reductions exceeding 95 %, whereas conventional CMV reduction techniques typically show reductions in the range of 70–90 %. This study's methodology demonstrates its versatility by guaranteeing greater compatibility with both POD and PD modification strategies.

The initial output voltage and common mode voltage of proposed multilevel inverter without POD and PD PWM techniques is high in amplitude as 400 V. The POD and PD techniques has been incorporated in the proposed multilevel inverter to reduce the common mode voltage. The common mode voltage is reduced as 14 V by POD method and 20 V with PD method compared to the conventional methods.

5. CONCLUSION

Common mode voltage for the different dc input values has been measured and compared. An innovative new method of topology for a 5-level inverter has been used as a proposed method in this paper. Thus, the output voltage and their respective waveform have Efficient and must be employed to reduce harmonic distortion. Common mode applied voltage gets reduced up to 8% of the initial value using the POD technique. It could get reduced further by using proper values. Hence, the POD

technique is more efficient. From the above comparison, it gets concluded that the POD method is the best method when compared with the PD method. By using the PD method and POD method common-mode voltage gets reduced. Although the suggested approach reduces CMV more effectively than the traditional approach, there may be additional computing needs and implementation complexity. The trade-off between performance improvements and the difficulty of changing hardware or algorithms should be examined in future research. There should be more research done on how lower CMV affects other performance indicators like switching losses or total harmonic distortion (THD). Future research can incorporate experimental validations to supplement simulation results and compare the suggested approach to a wider variety of modulation techniques. The efficacy of the suggested strategy can be further confirmed by real-time applications, particularly in industrial motors or renewable energy systems.

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Зменшення загального (сумарного) модового напруження за допомогою нової інверторної схеми Т-типу для застосування в електромобілях

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Багаторівневі інвертори (MLI) є важливими елементами у системах керування середньо- та високовольтною потужністю. У цій статті представлено нову інверторну схему Т-типу, що реалізується за допомогою методу широтно-імпульсної модуляції (PWM). Основними цілями є: отримання п'ятирівневої напруги на виході, зменшення загального модового напруження (Common Mode Voltage, CMV). Запропонована конструкція включає мультистанову (багатопозиційну) комірку перемикання, яка покращує PWM-сигнали, що подаються на керуючі входи MOSFET-транзисторів, дозволяючи досягти низького рівня втрат та високої ефективності роботи інвертора. Ключові особливості: Зниження кількості напівпровідникових ключів, Підвищення ефективності та надійності, Зменшення циркуляційних струмів у підшипниках електродвигуна за рахунок зменшеного CMV, що особливо важливо в асинхронних приводах електромобілів. Модель інвертора реалізовано в середовищі MATLAB/Simulink, результати чисельного моделювання підтвердили ефективність і працездатність запропонованої схеми для застосувань середньої потужності та напруги. Нова архітектура Т-типу MLI забезпечує економічне, масштабоване та енергоефективне рішення для систем електроприводів.

Ключові слова: Багаторівневий інвертор, Ефективність, MOSFET, Загальне модове напруження, Втрати.