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REGULAR ARTICLE

Characterization and Optimization of $Si_{0.75}Ge_{0.25}$-FinFETs Based on Operating Temperature and Gate Length

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This study focuses on the effect of temperature on the sensitivity of Metal-Oxide Semiconductor (MOS) transistors and FinFET devices using a $Si_{0.75}Ge_{0.25}$ heterostructure, through the analysis of current-voltage (*I-V*) characteristics under different thermal conditions. To investigate the mode coupling within MOS transistors by analyzing the performance of FinFET transistors under a range of different thermal conditions and gate lengths (L_g = 10, 20, and 30 nanometers). The results showed that FinFET transistors achieve the highest thermal sensitivity when the largest change in current (ΔI) occurs within the voltage range of 0 to 1 volt (V_{DD}), reflecting high efficiency in responding to thermal changes. It was also found that reducing the channel length leads to a significant increase in thermal sensitivity, especially in the length range of 10 to 20 nanometers. The optimal channel length was determined to be 10 nanometers to achieve superior thermal performance, serving as a benchmark for designing FinFET transistors that require high thermal efficiency and stability across various applications. The study included a wide range of temperatures, providing an enhanced understanding of the design.

Keywords: SiGe-FinFET, Temperature, Sensitivity, MuGFET, Nano-sensor.

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1. INTRODUCTION

In semiconductor technology, the Fin Field-Effect Transistor, or FinFET, is a noteworthy breakthrough. It is one of its design aspects that it has a presence of fins. A large amount of interest has been created within the business sector because of this finding, with sensors and switching devices constituting only a small portion of the countless possible uses [1-5]. However, FinFET technology continues to confront considerable obstacles, notably in theoretical modelling and manufacturing techniques, demanding increased research and development to improve efficiency and adaptability. One of the most common uses for this technology is integrated temperature sensors, Nanowire transistors are commonly used to reliably monitor temperature by analyzing the current-voltage characteristics under various thermal circumstances. Moreover, bipolar transistors can be adapted to function as diodes used for measuring temperatures with extreme precision.

As conventional MOSFETs contract closer to their functional limitations, the advancement of field-effect transistor (FET) technology has developed increasingly significantly. Despite MOSFETs' significant impact on the electronics industry, research into nanoscale FET designs is essential to achieving new levels of efficiency and performance. Such an inquiry is critical for moving research forward, enhancing manufacturing methods, and realizing the full promise of these cutting-edge technologies. FinFETs stand out among other FET designs because of their obvious benefits over conventional bulk silicon devices in circuit applications [11]. At temperatures ranging from 275 to 300 degrees Celsius, it has been shown that the Silicon-On-Insulator (SOI) completely depletes, while partly depleted SOI may function successfully up to 225 degrees Celsius. On the other hand, bulk silicon devices can only operate at temperatures up to 200 °C. The heat resistance of FinFETs makes them an excellent choice for applications that need great performance. Moreover, it is essential to consider the reliability of integrated circuits (ICs) when subjected to high heat loads, especially in applications such as automotive systems located near engine blocks and oil drill bit sensors. These specifications highlight how important it is to continue advancing FET technology to enhance the reliability and performance of electronic devices in challenging environments. FinFETs successfully address the constraints of conventional planar transistors, resulting from progress in semiconductor technology [12].

FinFET technology reduces short-channel effects and is a sophisticated method for creating nanoscale semiconductor components. Nonetheless, it encounters obstacles, especially self-heating, which can adversely affect device efficiency. Manufacturers must meticulously assess the effects of temperature variations on device reliability and performance. The complex microstructure of integrated circuits poses additional difficulties in the numerical

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simulation of FinFETs. Accurate electrothermal modelling is essential for producing intricate temperature profiles, regulating heat dissipation, and ensuring uniform temperature distribution.

The progression of FinFET technology has resulted in enhancements in semiconductor device efficacy. Preliminary assessments indicate minor discrepancies in thermal performance, implying that these models can attain significant precision in temperature predictions. The cofabrication of gate dielectrics in FinFET manufacturing mitigates contamination and gate misalignment, thereby enhancing device performance through the utilization of conventional materials rather than standard CMOS technology. Nonetheless, the manufacturing process presents challenges, including the etching procedure, which may result in discrepancies in device dimensions relative to traditional SOI devices. Comprehending these constraints is essential for advancing FinFET technology and refining its utilization in contemporary electronics.

The article emphasizes FinFET technology as a crucial element in the progression of semiconductor devices, especially as they shrink to the nanoscale. The analysis covers different device configurations, emphasizing their advantages and drawbacks. Future electronics applications need an understanding of how various configurations might impact device performance and scalability, which is provided by the simulations used in the study. Reducing the implementation and manufacturing costs of FinFET devices is another goal of the paper, which aims to increase their accessibility [14]. The investigation also examines the effects of channel parameters and oxide thickness, width, and length on the electrical properties of FinFETs. This analysis may play a significant role in optimizing their performance. FinFETs are multigate transistor designs that increase channel control to increase efficiency even in the absence of physical gates [15, 16]. On the other hand, the study provides a comprehensive analysis of FinFET technology, focusing on its configurations, concerns regarding cost, and electrical characteristics. This technology has been instrumental in the advancement of semiconductor design.

Table 1 – Advantages of FinFET

Parameters	Details
Power	– FinFETs have high power efficiency, which allows for better integration. – In high-performance systems, early adopters reported energy savings of up to 150 %.
Operating voltage	– FinFETs low threshold voltage (VT) allows them to operate well at lower voltage levels. – This reduces power loss and improves thermal management, making them ideal for portable and energy-intensive applications.
Feature size	– FinFET technology enables breaching the 20 nm barrier, which was previously thought to be the limit for planar devices. – This discovery allows for increased device density and improved performance, hence advancing semiconductor scaling.
Static leakage current	– Static leakage current is decreased by up to 90 %, considerably increasing energy efficiency in idle periods. This is especially helpful for systems that run on batteries, as leakage current is a big issue.
Operating speed	– FinFET variants are usually 30 % quicker than non-FinFET counterparts. Faster signal processing is ensured by reduced short-channel effects and enhanced electrostatic control over the channel.

2. METHODOLOGY

The structure of the FinFET examined in this study is shown in Figure 1. To assess the features of the FinFET transistor, the MuGFET model was used. The output characteristic curves of the transistor were examined through various configurations and conditions. The impact of numerous parameters, including temperature and gate length, on the behavior of the tiny transistor were carefully investigated utilising simulation-derived I-V physical attributes. This was done with Purdue University's MuGFET simulation program [17], it enables exact modelling and analysis of field-effect transistors with nanoscale geometries.

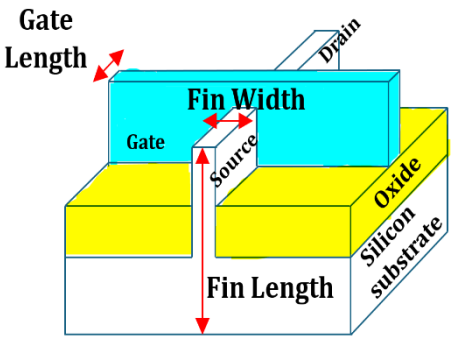

Fig. 1 – FinFET structure

PADRE and PROPHET, two powerful simulation tools integrated into MuGFET capabilities, were developed by Bell Laboratories. PADRE is a versatile device simulator designed for two- or three-dimensional devices with adaptable geometries, while PROPHET is an equation-based solver applicable to one, two, or three dimensions [17]. By producing typical FET output curves, these software tools provide researchers with important insights, particularly when the physics of FET operation is well represented. Independent responses to drift-diffusion models can be used to mimic transport dynamics by utilizing MuGFET [18]. Purdue University, one of the leading research universities in this field, developed and authorized the MuGFET nanoHUB. MuGFET tool is reliant on simulating Nanoscale Multi-gate-FET architectures (Nanowire and FinFET) utilizing drift-diffusion methods. Due to the high cost of nanodevices and the extensive body of research relying on simulation utilizing MuGFET, researchers used this technology to prevent losses in nanodevices [19-20].

To recreate the I_d-V_g properties of FinFETs at different temperatures, the following attributes were used in the MuGFET simulation: channel concentration

(*p*-type), channel width, drain length and source, drain concentration (*n*-type), and source. Oxide thickness and gate length. An illustration of the FinFET environment could be found in [21-22]. These parameters were carefully chosen to ensure precise FinFET behavior modelling, allowing a thorough examination of the device's electrical characteristics under various thermal conditions.

I_d-V_g characteristics of FinFET transistors were simulated at different temperatures (275, 300, 325, and 350 K) using specific parameters. These parameters included source and drain lengths of 5 nm, an equal distribution of N-type concentrations, an oxide layer thickness of 1 nm, and a channel diameter of 3 nm with a gate doping concentration of 10^{19} cm^{-3}. The optimal thermal sensitivity of the FinFET was determined in the operating voltage range of 0-1 V by identifying the maximum current change (ΔI). Moreover, increasing oxide thickness reduces the drain-induced barrier lowering (DIBL) and results in a proportional shift in the threshold voltage.

3. ARTICLE STRUCTURE AND THE CORRESPONDING STYLES

Figs. 2-4 show the variation in current (I) because of gate lengths (L_g) of 10, 20, and 30 nm, with voltage increments of 0.1 V. Within the V_{DD} range of 0 to 1 V, the results show a linear reduction in V_{DD} with increasing temperature, with lower temperatures showing the most sensitivity (max ΔI). For L_g values of 10 nm and 20 nm, respectively, Figures 4 (a) and (b) show the ideal temperature sensitivity coefficients at V_{DD} = 0.9 V, whereas Figbre 4 (c) shows the lowest sensitivity at L_g = 30 nm for V_{DD} = 1 V. These findings highlight that, as shown in Figures 4 (a) to (c), the transistor operates most favorably at a drain voltage (V_d) of 0.9 V, which provides stability over the 325-350 K temperature range.

This behavior suggests that gate length and operating voltage have a significant influence on the thermal and electrical performance of the FinFETs and emphasizes the importance of modifying these characteristics for reliable device operation across a range of temperature settings.

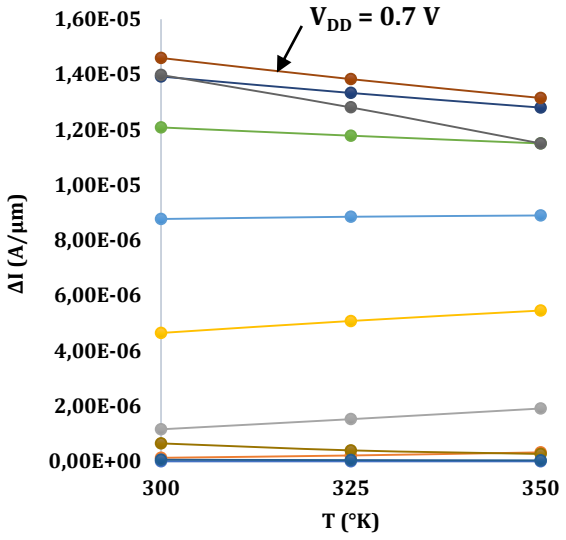

Fig. 2 – ΔI–T characteristics of FinFET (W_g = 10 nm, L_g = 10 nm)

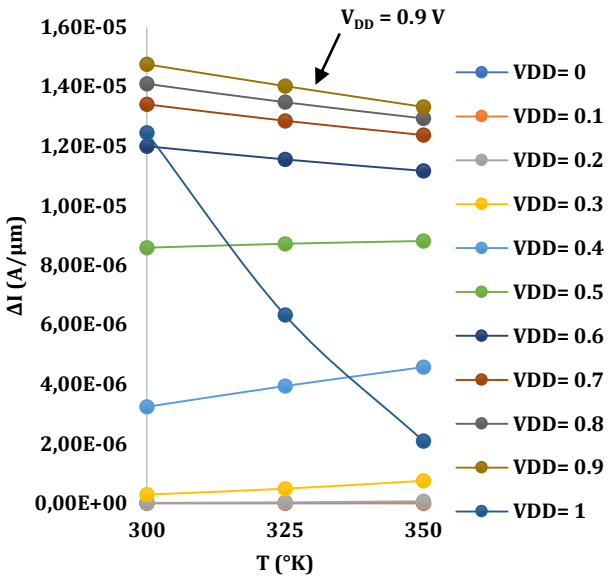

Fig. 3 – ΔI–T FinFET characteristics (W_g = 10 nm, L_g = 20 nm)

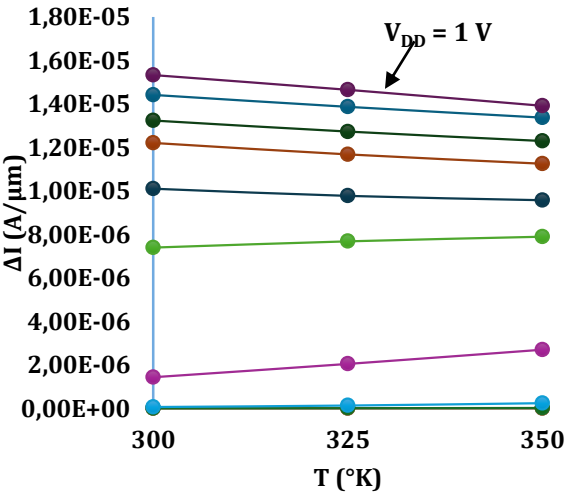

Fig. 4 – (c) ΔI–T FinFET characteristics (W_g = 10 nm, L_g = 30 nm)

Figs. 5-7 show how various temperatures (275, 300, 300, 325, and 350 K) affect the current variations (ΔI) of FinFET gates with varied widths (10 nm, 20 nm, and 30 nm) and variable power supply voltages. The results showed that the highest sensitivity (ΔI) occurs at V_{DD} = 0.7 volts for the 10-nm gate, V_{DD} = 0.9 volts for the 20-nm gate, and V_{DD} = 1 volt for the 30 nm-gate. The study identified a substantial association between current fluctuations, temperature, and voltage conditions, demonstrating that ΔI increases with higher temperature and V_{DD} voltage. The results indicated that the ideal working voltage is 0.9 volts with a gate width (W_g) of 10 nm for both 10-nm and 20-nm gates, enhancing stability and sensitivity under these parameters. These results emphasize the importance of optimizing gate design, such as gate length (L_g), gate width (W_g), and operating voltage (V_{DD}), to improve the thermal and electrical properties of FinFETs, especially in applications that require long-term stability and high sensitivity over a wide temperature range.

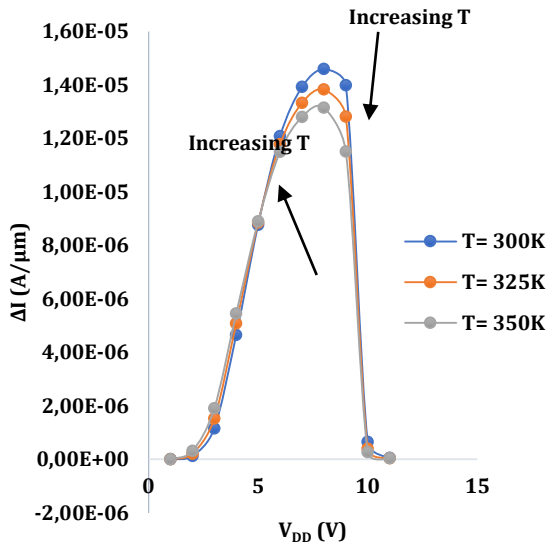

Fig. 5 – FinFET characteristics (W_g = 10 nm, L_g = 10 nm) ΔI–V_{DD}

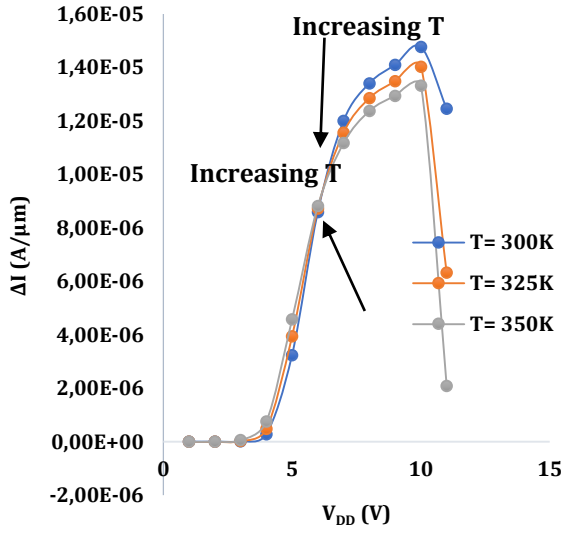

Fig. 6 – FinFET characteristics (W_g = 10 nm, L_g = 20 nm) ΔI–V_{DD}

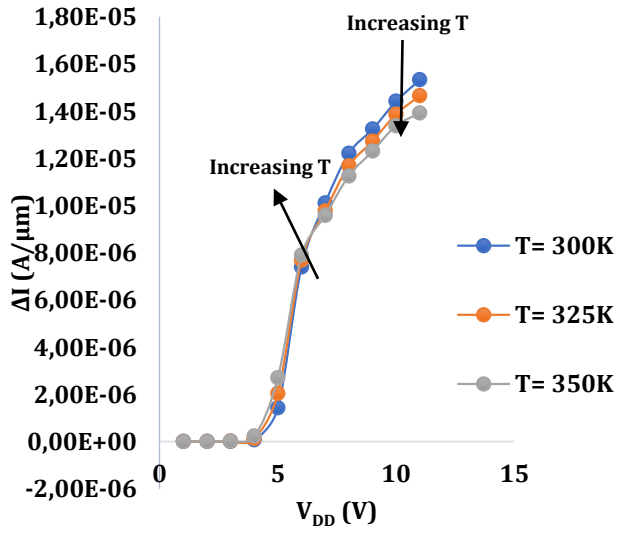

Fig. 7 – FinFET characteristics (W_g = 10 nm, L_g = 30 nm) ΔI–V_{DD}

As seen in Figure 8 is the correlation between the optimal temperature sensitivity and the channel length (L_g). Figs. 5-7 illustrates the appropriate ideal operating voltage (V_{DD}) that results in the highest thermal sensitivity. The results demonstrate that the thermal sensitivity increases significantly up to L_g = 20 nm, despite the very small range of channel lengths (10-30 nm). As the channel length grows beyond 20 nm, the relationship between thermal sensitivity and length diminishes linearly. This advancement highlights how important channel length is in modifying FinFETs' thermal performance. Up to 20 nm, the sensitivity sharply increases, indicating the ideal trade-off between device scalability and thermal response. Nevertheless, the sensitivity falls with increasing channel length. These findings offer crucial information for creating FinFETs with improved thermal sensitivity, especially when it comes to choosing the ideal channel length to maximize device capacity.

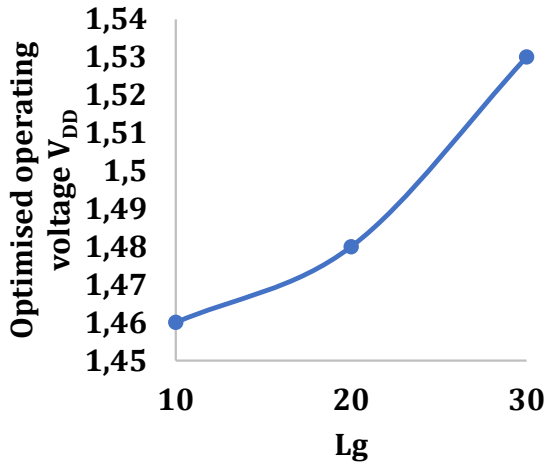

Fig. 8 – Based on the highest temperature sensitivity, the operating voltage V_{DD} was optimized using a range of channel lengths)

With L_g = 10 nm and W_g = 10 nm, the temperature profiles for important FinFET properties, such as subthreshold swing (SS), threshold voltage (V_T), and drain-induced barrier lowering (DIBL), are shown in Fig. 9 at temperatures of 275 K, 300 K, 325 K, and 350 K.

V_T decreased linearly as the temperature increased, from 0.37 V at 275 K to 0.31 V at 350 K. Due to the impact of DIBL, the leakage current in the OFF-state increases because of the channel's potential barrier being lowered at the source.

The most departure from the optimal SS value of 69.5 mV/dec was seen at 350 K, when SS increased to 224.75 mV/dec, as opposed to 166.82 mV/dec at 275 K. It's interesting to see that SS got closer to the optimal value of 54.6 mV/dec at 350 K, suggesting better performance at higher temperatures.

DIBL increased exponentially with temperature, reaching 214.96 mV/V at 350 K from 191.19 mV/V at 275 K. This demonstrates how temperature significantly affects the FinFET's OFF-state leaking behavior. The research shows that the ideal transistor size for L_g values of 10 nm and 20 nm is at 350 K. Furthermore, the results show that: hyperbolic rise in V_T with increasing oxide

thickness, and DIBL exhibits exponential growth with increasing temperature. As temperature rises, SS increases linearly.

These discoveries offer important information on how to optimize the design parameters of FinFETs for improved performance in a range of temperature settings.

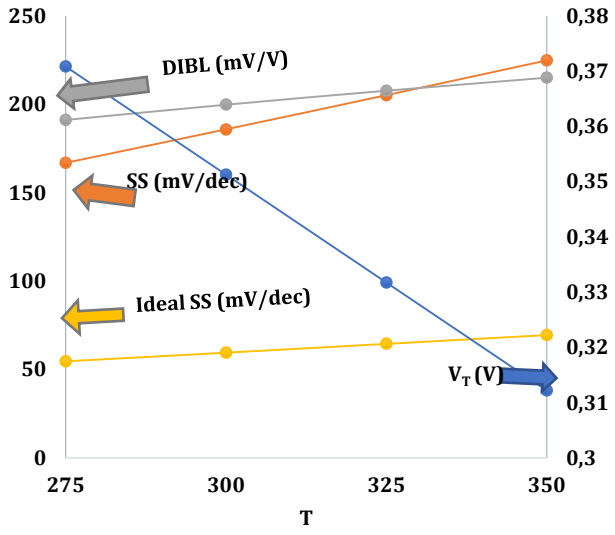

Fig. 9 – V_T, SS and DIBL at W_g = 10 nm, L_g = 10 nm

Fig. 10 illustrates the behavior of V_T, SS, and DIBL for a FinFET at temperatures of 275 K, 300 K, 325 K, and 350 K, with a gate length (L_g) of 20 nm and W_g of 10 nm. As the temperature rises from 275 K to 350 K, these parameters exhibit a linear decrease. Specifically, SS ranges from 93.65 to 120.92 mV/dec, DIBL from 25.1 to 36 mV/V, and V_T from 0.56 to 0.52 V. The greatest deviation from the ideal SS value of 54.6 mV/dec occurs at 350 K, where SS exceeds 93.65 mV/dec. The increasing temperature leads to higher SS, peaking at 120.92 mV/dec. Similarly, DIBL exhibits a rising trend with temperature.

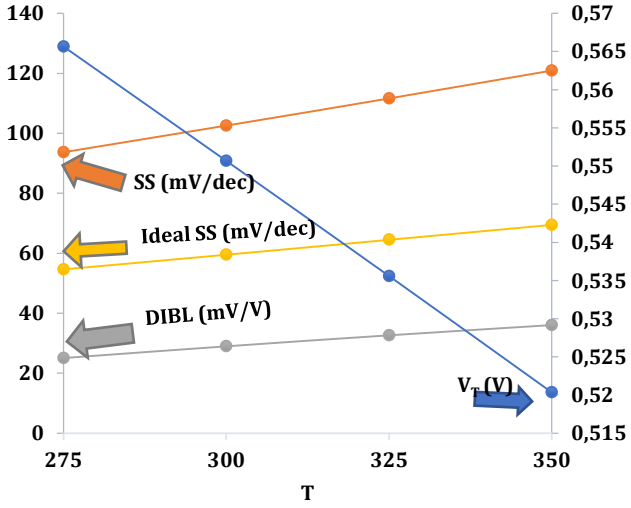

Fig. 10 – V_T, SS and DIBL at W_g = 10 nm, L_g = 20 nm

Fig. 11 highlights the interplay between V_T, DIBL, and SS for L_g = 30 nm and W_g = 10 nm, demonstrating their collective impact on FinFET performance across the same temperature range. From 0.58 V at 275 K to 0.56 V at 350 K, V_T falls linearly with rising temperature. DIBL grows from 4.11 to 7.98 mV/V while SS climbs from 75 to 97.25 mV/dec. At 350 K, when the SS hits 69.6 mV/dec, the optimum SS value of 54.6 mV/dec is most nearly attained. The best mix of gadget size and running temperatures depends on these electrical properties. SS rises to 97.25 mV/dec at 350 K, whereas DIBL maintains its upward trend underlining their impact on device performance.

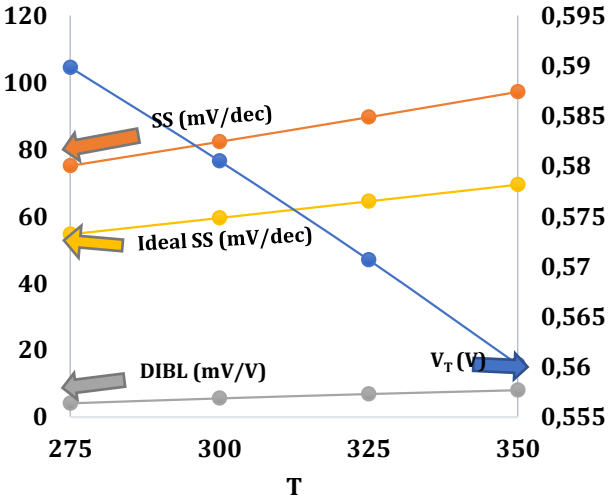

Fig. 11 – V_T, SS and DIBL at W_g = 10 nm, L_g = 30 nm

Fig. 12 shows the relationship between the channel length of a FinFET transistor and its electrical characteristics. It is observed that the optimal channel length ranges between 20-30 nanometers, where the maximum value of the threshold voltage (V_T) and the minimum value of the drain-induced barrier lowering (DIBL) are achieved, and the subthreshold slope (SS) is closest to the ideal value. These results confirm previous studies [23] that indicate a linear relationship between the electrical characteristics of FinFET devices and the diameters of their channels. Table 2 also presents a comparison between FinFET results and other studies.

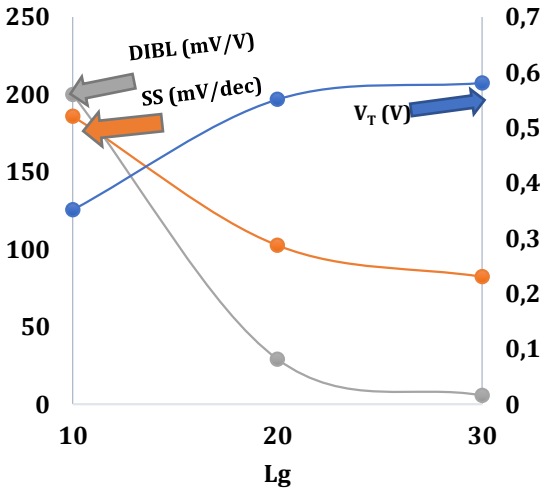

Fig. 12 – V_T, SS and DIBL with L_g

Table 2 – Comparison with another research works

Reference	Best value of SS	Best value of DIBL
[24]	72.43 mv/dec	139.52 mv/V
[25]	80 mv/dec	10 mv/V
[26]	73 mv/dec	28mv/V
[26]	60 mv/dec	10 mv/V
Present study	75 mv/dec	4.11 mv/V

4. CONCLUSION

The study identifies a channel length of 20 nm as the optimal choice for FinFETs, delivering superior electrical performance in terms of threshold voltage (V_T), drain-induced barrier lowering (DIBL), and subthreshold swing (SS). Results reveal that as the channel length extends beyond 20 nm, V_T increases and approaches saturation, while SS improves, nearing its ideal value. Drain-Induced Barrier Lowering (DIBL) demonstrates a gradual increase as the channel length exceeds 20 nm. However, beyond this point, it experiences a significant and rapid decline. The research conducted offers a thorough investigation of the effects of temperature on these parameters over channel lengths ranging from 10 to 30 nm and was carried out at different temperatures (275, 300, 325, and 350 K). The findings indicate that future studies could aim to refine gate operation and mesh spacing parameters to further optimize FinFET performance, particularly for shorter gate lengths. This research offers valuable contributions to the design and optimization of FinFETs, playing a pivotal role in advancing semiconductor technology and enhancing electronic device performance.

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Характеристика та оптимізація $Si_{0.75}Ge_{0.25}$-FinFET на основі робочої температури та довжини затвора

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Це дослідження зосереджено на впливі температури на чутливість МОН-транзисторів та FinFET-пристроїв з використанням гетероструктури $Si_{0.75}Ge_{0.25}$ шляхом аналізу вольт-амперних (ВА) характеристик за різних теплових умов. Метою є дослідження зв'язку мод у МОН-транзисторах шляхом аналізу продуктивності FinFET-транзисторів за різних теплових умов та довжин затворів (L_g = 10, 20 та 30 нанометрів). Результати показали, що FinFET-транзистори досягають найвищої теплової чутливості, коли найбільша зміна струму (ΔI) відбувається в діапазоні напруги від 0 до 1 вольта (V_{DD}), що відображає

високу ефективність реагування на теплові зміни. Також було виявлено, що зменшення довжини каналу призводить до значного збільшення теплової чутливості, особливо в діапазоні довжин від 10 до 20 нанометрів. Оптимальна довжина каналу була визначена на рівні 10 нанометрів для досягнення чудових теплових характеристик, що служить орієнтиром для проектування FinFET-транзисторів, які потребують високої теплової ефективності та стабільності в різних застосуваннях. Дослідження включало широкий діапазон температур, що забезпечило глибше розуміння конструкції.

Ключові слова: SiGe-FinFET, Температура, Чутливість, MuGFET, Наносенсор.