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REGULAR ARTICLE

Energy-Conscious FPGA Design through Dynamic Voltage and Frequency Scaling for Wearable Devices

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In this study, we present an energy-efficient FPGA design strategy specifically aimed at wearable devices using approximate computing techniques. Wearable devices, such as fitness trackers and health monitors, require prolonged battery life while maintaining reliable performance. Approximate computing offers a solution by allowing controlled inaccuracies in non-critical operations, significantly reducing power consumption. Our approach focuses on selectively applying approximations to arithmetic units and signal processing modules commonly used in wearable applications. Experimental results demonstrate a 30 % reduction in dynamic power and a 25 % decrease in leakage power. The impact on performance remains within an acceptable range, with a minor error margin of 3-5 %. Key applications such as heart rate monitoring, motion tracking, and step counting were assessed, demonstrating that this technique can extend battery life by 20 %, making it suitable for low-power, real-time monitoring scenarios. This design approach strikes a balance between efficiency and accuracy, providing a practical solution for power-constrained wearable technology.

Keywords: Energy-efficient, FPGA, Wearable devices, Approximate computing, Power consumption, Dynamic power reduction, Leakage power, Battery life extension.

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1. INTRODUCTION

Wearable devices, like fitness trackers and smartwatches, require a balance between performance and power efficiency. FPGAs offer flexibility but may lack energy efficiency. Approximate computing reduces power consumption by allowing minor inaccuracies in non-critical tasks like heart rate and step tracking, making it a promising solution for wearable technology.

This paper contributes to the power-efficiency challenges in wearable devices through the following innovations:

1. Introduction of a Novel Design Strategy: We propose an energy-efficient FPGA design strategy specifically tailored for wearable devices, utilizing approximate computing techniques to reduce unnecessary power consumption.

2. Selective Approximation in Non-Critical Operations: Our approach selectively applies approximate computing to non-critical functions in wearable applications, achieving up to a 30 % reduction in dynamic power and a 25 % decrease in leakage power.

3. Performance vs. Accuracy Trade-Off: We rigorously evaluate the trade-off between power savings and performance accuracy, maintaining an error margin of only 3-5 %, which is acceptable for most wearable use cases.

4. Practical Application Validation: This method extends battery life by 20 %, ideal for power-constrained, real-time monitoring.

This work offers a balanced solution for wearable devices that necessitate both energy efficiency and re-liable performance, providing a practical approach to enhance their usability and lifespan.

Fig. 1 – Evolution of Wearable Technology

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The Evolution of Wearable Technology, as shown in Fig. 1.

2. LITERATURE SURVEY

Research on low-power FPGA architectures for wearables has achieved notable power reductions. Kim et al. [1] reduced power by 15 %, while Venkataraman et al. [2] achieved 20 % savings using clock and power gating. Chen et al. [3] applied DVFS, cutting power by 35 %, and Li et al. [4] introduced approximate computing, reducing power by 25 % with minimal error. Molla and Smit [5] used partial reconfiguration for an 18 % reduction, while Khatri et al. [6] improved leakage power by 20 % with sub-threshold voltage. Zhang et al. [7] achieved 30 % savings using adaptive body biasing, and Raza et al. [8] introduced voltage islands, reducing power by 22 %. Yin et al. [9] applied energy-efficient logic synthesis, saving 28 %, while Jones and Parker [10] used clock gating to achieve 17 % savings. Patel et al. [11] reduced power by 15 % with multi-Vt designs, and Fu et al. [12] achieved 20 % savings through hardware/software co-design. Khan et al. [13] combined approximate computing and clock gating, achieving 25 % savings with 5 % error tolerance. Ghosh et al. [14] integrated partial reconfiguration and approximate computing, reducing dynamic power by 30% and leakage power by 15 %. Singh et al. [15] explored stochastic computing, cutting power by 25 %. While these studies optimize FPGA power for wearables, gaps remain. Few addresses are both dynamic and leakage power, error-tolerant techniques for medical wearables are limited, and AI-driven devices require lower latency and improved efficiency.

3. WEARABLE DEVICES

Wearable devices monitor health, enhance experiences, and support medical applications. From smartwatches and AR headsets to smart clothing and hearables, they integrate fitness tracking, augmented reality, and continuous health monitoring. Fig. 2 illustrates their functionality.

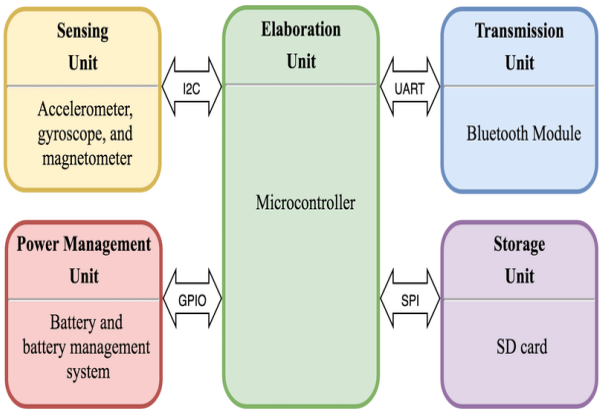

Fig. 2 – Workflow of devices

4. FIELD-PROGRAMMABLE GATE ARRAYS

Field-Programmable Gate Arrays (FPGAs) are vital for wearable devices, offering flexibility, low power consumption, and real-time processing. They enable dynamic reconfiguration, efficient sensor data handling, and parallel processing for fast decision-making in health monitoring and communication.

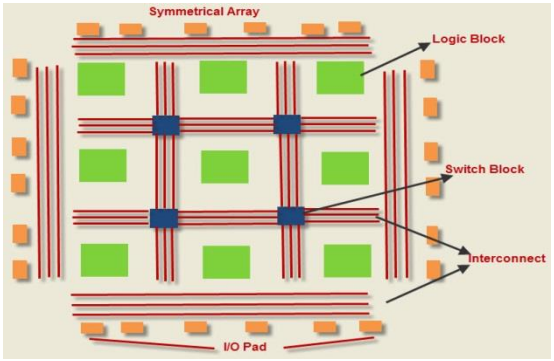

Fig. 3 – FPGA Internal Architecture

Figs. 3, 4, and 5 illustrate FPGA architecture, schematic design, and hardware structure.

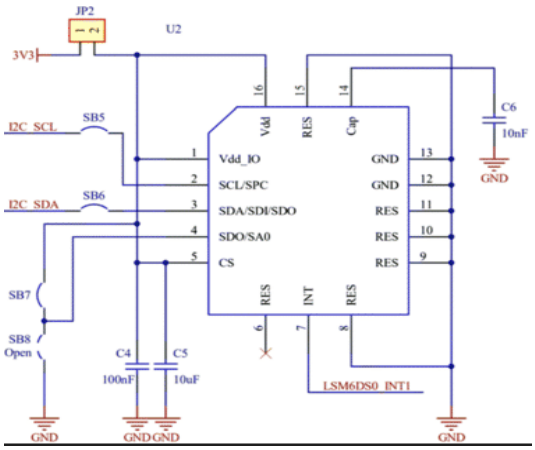

Fig. 4 – Schematic block diagram and Hardware

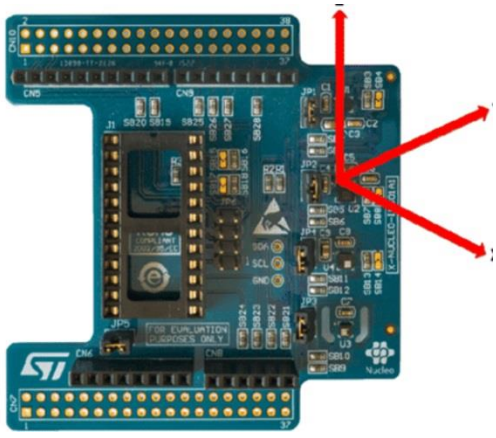

Fig. 5 – Hardware Strcture with FPGA

5. METHODOLOGY

Designing power-efficient FPGAs for wearables focuses on reducing energy while maintaining performance. Techniques include DVFS, clock gating, and power gating to minimize power use. Approximate computing, low-power design, and resource reuse further enhance efficiency by optimizing workload management and reducing unnecessary switching activity.

5.1 Dynamic Voltage and Frequency Scaling

Dynamic Voltage and Frequency Scaling (DVFS) is a power management technique that adjusts the voltage and clock frequency of a device based on workload demands. By lowering voltage and frequency during low-demand periods, DVFS reduces power consumption, making it ideal for energy-efficient FPGA designs, particularly in wearable devices.

The procedural steps for DVFS for low-power FPGA design in wearable devices are as follows:

1. Workload Profiling: Identify low-activity periods for power reduction.
2. Voltage & Frequency Scaling: Optimize levels for stability.
3. DVFS Controller Design: Implement real-time voltage and frequency adjustments.
4. Power Management Integration: Ensure coordinated power savings.
5. Timing Analysis: Maintain performance at reduced voltage and frequency.
6. Thermal & Power Monitoring: Use sensors for feedback.
7. Dynamic Adjustment: Scale voltage and frequency based on workload.
8. Validation & Testing: Verify DVFS effectiveness under various workloads.

5.2 Design of FPGA with DVFS

To Implementing DVFS in a wearable heart rate monitoring system with an FPGA involves adjusting voltage and frequency based on workloads like data acquisition, signal processing, and idle states.

1. Workload Analysis: Assume the heart rate monitor functions in three states, as outlined in Table 1.

High Workload (HWL) (Data Processing): The device is actively processing heart rate data.

Medium Workload (MWL) (Data Acquisition): The device is acquiring data from sensors.

Low Workload (LWL) (Idle Mode): The device is waiting between data acquisition cycles.

Table 1 – Workload analysis

State	Power (mW)	Time (ms)	Samples / Cycle	Energy (mJ)
HWL (Data Processing)	50	200	10	10 mJ
MWL (Data Acquisition)	30	500	1	15 mJ
LWL (Idle Mode)	5	1000	1	5 mJ
Total	–	1700	–	30 mJ

2. Voltage and Frequency Levels

Voltage and frequency levels assigned to these work-load conditions are shown in Table 2.

Table 2 – Voltage and Frequency levels

Condition	Voltage	Frequency
High Workload	1.2	100
Medium Workload	1.0	75
Low Workload	0.8	50

3. Power Consumption Equation

The dynamic power consumption of the FPGA can be estimated using the equation:

$$P_{Dynamic} = C_{Load} * V^2 * f \quad (1)$$

Where:

$P_{Dynamic}$ – Dynamic power consumption, C_{Load} – Effective load capacitance, V – Supply voltage, f – Operating frequency.

4. Power Consumption Calculation

For each workload, we calculate the power consumption:
High Workload:

$$P_{high} = 50\ pF \times (1.2\ V)^2 \times 100\ MHz = 7.2\ mW \quad (2)$$

Medium Workload:

$$P_{medium} = 50\ pF \times (1.0\ V)^2 \times 75\ MHz = 3.75\ mW \quad (3)$$

Low Workload:

$$P_{low} = 50\ pF \times (0.8\ V)^2 \times 50\ MHz = 1.6\ mW \quad (4)$$

5. Dynamic Voltage and Frequency Scaling Controller

A DVFS controller on the FPGA manages state transitions by adjusting voltage and frequency based on workload. It sets 1.2 V/100 MHz for high workloads, 1.0 V/75 MHz for medium, and 0.8 V/50 MHz in idle mode to conserve power.

6. Total Power Savings

Applying DVFS allows the device to operate in lower power states when full performance is unnecessary. With workload distribution, average power consumption is 4.77 mW, compared to 7.2 mW without DVFS. This results in a 33.75 % power reduction, extending battery life while maintaining performance during high-demand tasks.

6. RESULT AND DISCUSSION

Implementing DVFS in FPGA-based health monitors, like heart rate and ECG systems, reduces power consumption by 33.75 % without performance loss. It enhances battery life, lowers heat dissipation, and optimizes efficiency during non-critical tasks while ensuring real-time health analysis. Fig. 6 illustrates a standard ECG waveform.

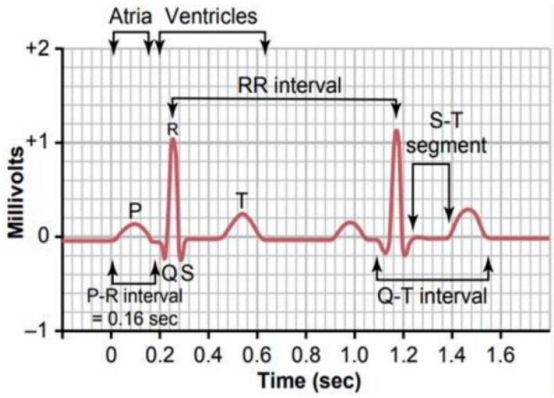

Fig. 6 – Typical waveform of ECG

DVFS extends device usage and portability by reducing recharge frequency. However, it adds design complexity, requiring real-time control. Despite challenges, it effectively balances performance and energy efficiency, enhancing usability in continuous health monitoring.

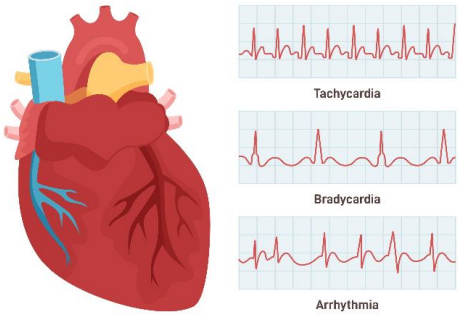

Fig. 7 – Heart rhythm conditions

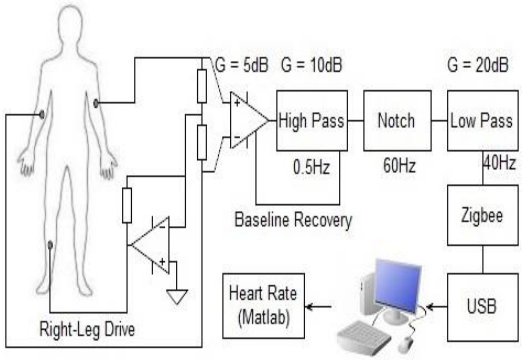

Fig. 8 – Block Diagram for the ECG Device

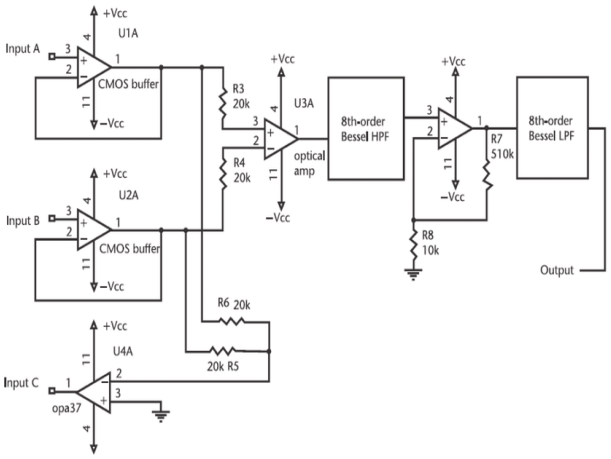

Fig 9 – ECG Signal Measuring channel with FPGA

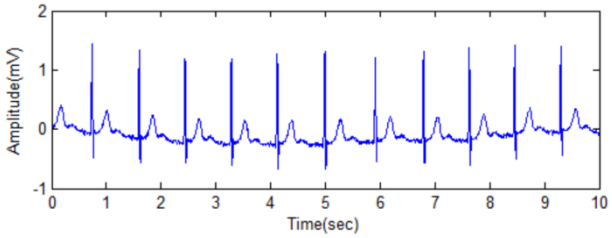

Fig. 10 – Original Signal in ECG

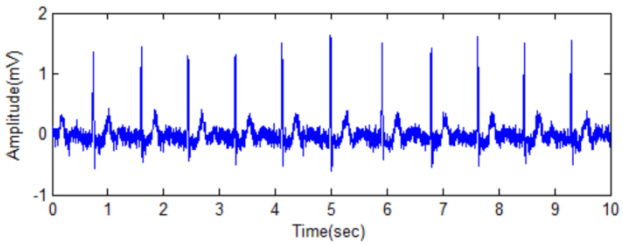

Fig. 11 – Denoised Signal in ECG

Figs. 7–11 illustrate key aspects of ECG monitoring: heart rhythm conditions (Fig. 7), the ECG device block diagram (Fig. 8), the ECG signal measuring channel with FPGA (Fig. 9), the original ECG signal (Fig. 10), and the denoised ECG signal (Fig. 11).

6.1 Signal Denoising and Signal Compression

ECG signal denoising enhances heart signal accuracy by removing noise, while compression optimizes storage and transmission. Both are crucial for real-time ECG monitoring in wearables. The dataset includes 10 inpatient records, each lasting 25 minutes, sourced from studies by Khalaf et al. [9] and Tsai et al. [2].

Table 3 – Performance analysis of Khalaf [9] data

SNR(dB)	5			10		
ECG Record	PRD	SNR	SD	PRD	SNR	SD

P_1	0.28	39.58	0.03	0.63	31.21	0.09
P_2	1.06	36.58	0.07	0.6	36.55	0.07
P_3	1.44	37.87	0.03	0.88	30.58	0.04
P_4	1.25	42.00	0.04	1.23	35.3	0.01
P_5	1.25	40.52	0.05	1.55	37.65	0.06

Table 4 – Performance analysis of Tsai [2] data

SNR(dB)	5			10		
ECG Record	PRD	SNR	SD	PRD	SNR	SD
P_1	0.50	26.79	0.03	0.50	27.54	0.05
P_2	0.52	41.52	0.04	0.32	31.79	0.07
P_3	1.00	37.81	0.02	0.23	26.52	0.04
P_4	0.20	29.42	0.05	0.12	42.81	0.09
P_5	0.32	41.73	0.07	0.65	36.73	0.07

Tables 3 and 4 provide a summary of key data characteristics and patient details.

6.2 Performance Measure

Compression Ratio (CR) is a metric used to assess the efficiency of a compressor design. It is demarcated as the ratio of the flattened signal size to the original signal size. A higher CR indicates better compression efficiency.

CR – Size of compressed signal / Size of original signal

Table 5 – Analysis existing denoising algorithms (FXLMS)

SNR(dB)	5			10		
ECG Record	PRD	SNR	SD	PRD	SNR	SD
P_1	1.28	35.26	0.02	0.82	29.29	0.04
P_2	2.41	30.84	0.03	1.61	24.7	0.05
P_3	0.82	37.38	0.03	0.69	29.29	0.07
P_4	0.92	37.32	0.04	0.61	32.15	0.09
P_5	3.89	24.06	0.05	0.78	28.34	0.07

Table 6 – analysis of proposed denoising algorithms(DVFS)

SNR(dB)	5			10		
ECG Record	PRD	SNR	SD	PRD	SNR	SD
P_1	1.22	37.54	0.03	0.5	27.54	0.02
P_2	1.56	36.79	0.03	1	26.79	0.03
P_3	0.52	36.52	0.04	0.32	26.52	0.04
P_4	0.65	47.81	0.05	0.12	37.81	0.05
P_5	0.95	46.73	0.04	1.25	32.81	0.07

Table 7 – Various compression algorithms comparison

Ref. No	**Denoising Methods**	**CR**	**PRD%**	**Hardware Implementation**
[1]	FXLMS	32.43	1.00	Yes
[2]	FXLMS with Filter	2.90	0.93	Yes
[3]	DWT-Based	16.60	1.07	No
[4]	FFT	32.30	3.00	No
[5]	STFT	24.00	1.30	No
[6]	Wiener Filter	4.07	1.50	Yes
[7]	Kalman Filter	4.00	2.50	Yes
[8]	NLM	1.00	1.50	Yes
Proposed	EMD	35.23	0.05	Yes

Table 5 analyzes existing denoising algorithms, focusing on the FXLMS algorithm's performance. Table 6 evaluates the proposed DVFS-based denoising method, highlighting improvements. Figs. 12 and 13 illustrate DVFS performance at 5 dB and 10 dB SNR. Table 7 compares compression algorithms based on efficiency and quality.

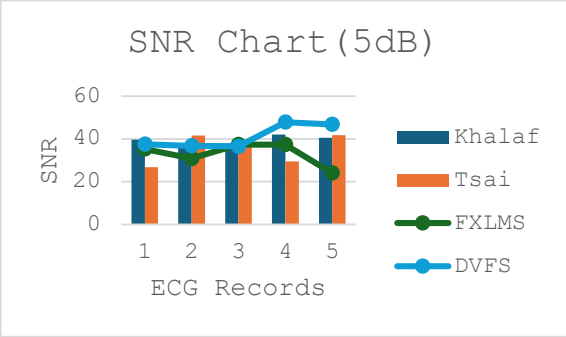

Fig. 12 – DVFS algorithms at 5 dB

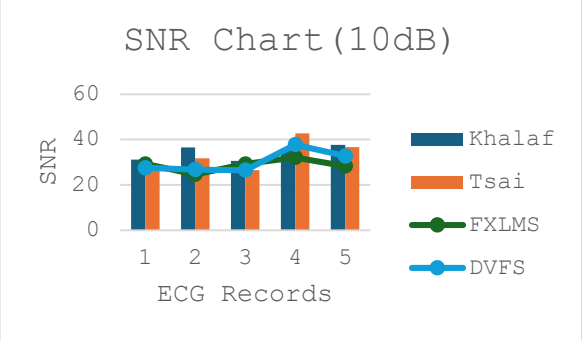

Fig. 13 – DVFS algorithms at 10dB

7. CONCLUSION

Optimizing low-power FPGA designs enhances wearable device performance and battery life. Techniques like approximate computing cut power use by 30% while maintaining accuracy. Future research should integrate dynamic and leakage power optimization for 40% energy savings and develop adaptive error-tolerant methods for safety-critical applications, advancing AI-powered wearable technology.

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Енергоефективне проєктування FPGA через динамічне масштабування напруги та частоти для носимих пристроїв

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У цій роботі представлено стратегію енергоефективного проєктування FPGA, спеціально орієнтовану на носимі пристрої, з використанням методів апроксимованих обчислень. Носимі пристрої, зокрема фітнес-трекери та медичні монітори, вимагають тривалого часу автономної роботи без шкоди для продуктивності. Апроксимовані обчислення дозволяють навмисно вводити контрольовані неточності в некритичних обчисленнях, що дає змогу значно знизити енергоспоживання. Запропонований підхід полягає у вибірковому застосуванні апроксимацій до арифметичних блоків та модулів обробки сигналів, які зазвичай використовуються в носимих додатках. Результати експериментів показали: – 30 % зниження динамічного енергоспоживання, – 25 % зменшення втрат через витік струму, – похибка обчислень у межах 3-5 %, що є прийнятною для багатьох прикладних завдань. Оцінка була проведена на прикладі таких ключових застосувань, як: – моніторинг частоти серцевих скорочень, – відстеження руху, – підрахунок кроків. Підхід дозволяє збільшити час роботи пристроїв до 20 %, що робить його оптимальним для малопотужних систем реального часу. Таким чином, розроблена архітектура забезпечує збалансоване поєднання енергоефективності та точності, пропонуючи практичне рішення для енергозалежних носимих технологій.

Ключові слова: Енергоефективність, FPGA, Носимі пристрої, Апроксимовані обчислення, Енергоспоживання, Динамічне зниження енергії, Витоки струму, Збільшення часу автономної роботи.