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REGULAR ARTICLE

An Improved Low Power Sense Amplifier Using Level Restoration Technique and Performance Comparison with Existing Sense Amplifier Topologies at 32 nm Technology

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Sense amplifiers (SA) are essential in the peripheral circuitry of Static Random Access Memory (SRAM). They enhance operational speed, minimize power consumption, and reduce access time. This paper introduces a modified and enhanced Dual Switch Level Restoration Voltage-mode Sense Amplifier (DSLR-VMSA). An operational voltage of 1.8 V and a 32 nm technology node were used to simulate the design. Comparative analysis with established sense amplifier topologies on parameters such as power consumption, energy efficiency, delay, and current characteristics reveals DSLRA-SA's superior performance. Notably, this improved circuit achieves a power consumption of 6.7 uW, half that of the conventional Cross-Coupled Voltage Latch Sense Amplifier (CCVLSA). Energy and delay metrics also exhibit marked improvements. The study includes in-depth analyses such as Dimensional, Monte Carlo, and Temperature analyses, as well as evaluations on the impact of sleep transistors, to validate the enhanced SA's performance. Incorporating sleep transistors in the modified design further reduces power, delay, and energy consumption, significantly enhancing overall performance. The results underscore the suitability and superiority of the improved SA, particularly for low-power CMOS SRAM applications.

Keywords: Sense amplifier, Level restoration, Sleep transistor, Delay, Current, Monte Carlo analysis.

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1. INTRODUCTION

In modern CMOS memory circuits, the power and speed performance of sense amplifier is a critical aspect [1-2]. Amongst the different memory topologies, the embedded SRAM is thefastest, but it is usually the most power-hungry memory. The SRAM operates solely when a supply voltage (VDD) is present in the circuit. This means that data is retained within the memory cell when VDD is applied, but is lost when VDD is disconnected (turned off). SRAM is typically integrated within System on Chips (SOCs) for quick operation and is referred to as cache. The major performance parameters for an SRAM are energy consumption, leakage current, power utilization and propagation delay required for the circuit. Additionally, Reducing the circuit's power consumption, size, and latency has become a key design goal due to the growing need for low-power portable digital devices.

An important component of the SRAM peripheral circuit is the sense amplifier. Sense amplifiers play a crucial role in the operation of RAM, DRAM, and SRAM cells by facilitating the accurate reading of their contents. Due to their high sensitivity to noise, their design ensures robust noise margins to guarantee reliable data representation from each memory cell. There exist two primary types of sense amplifiers: static sense amplifiers, employed in static RAMs and SRAMs to detect logic states, and dynamic sense amplifiers, utilized to conserve energy during low power consumption phases.

The significance of fast sense amplifiers lies in their ability to minimize latency in various circuits, particularly in tasks like bit-line reading within memory systems. As CMOS chips advance towards sub-micrometer scales, minimizing on-chip delays caused by interconnections becomes increasingly critical. Fast sense amplifiers serve as essential repeaters for high-speed signals that need to traverse large chip distances efficiently.

Aspect ratio is another important factor that affects the operational effects in relation to the voltage level. To ensure optimized aspect ratios are utilized for circuit evaluation, dimensional analysis is employed for determining pull up and cell ratio for the modified SA topology. The study is examined in supplementing part of this paper. The modified SA topology is designed based on the different SA topologies already reported in the literature. The different categories of the SA topology include – single and double ended, voltage mode, current mode, charge transfer mode and latch type SA etc. [4-6]. Amongst the different SA topologies, the cross coupled voltage mode SA (VMSA) is reported to have optimal performance. The feature that deems the cross coupled latch type SA better than others due to its no static current through the circuit. Therefore Low power cache implementation requires extensive analysis and planning, as well as the output of the highest performing VMSA and appropriate circuit operation. Power, speed, transistor count area, and aspect ratio are the primary design factors to be taken into account [7-8]. Transistors are typically utilized in circuits with fewer space requirements

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in lower numbers [9]. The impact of adding or removing head and foot switch sleep transistors has been studied in order to investigate the same. High speed and low power, energy, and area SAs are regarded as the best SA topologies [9].

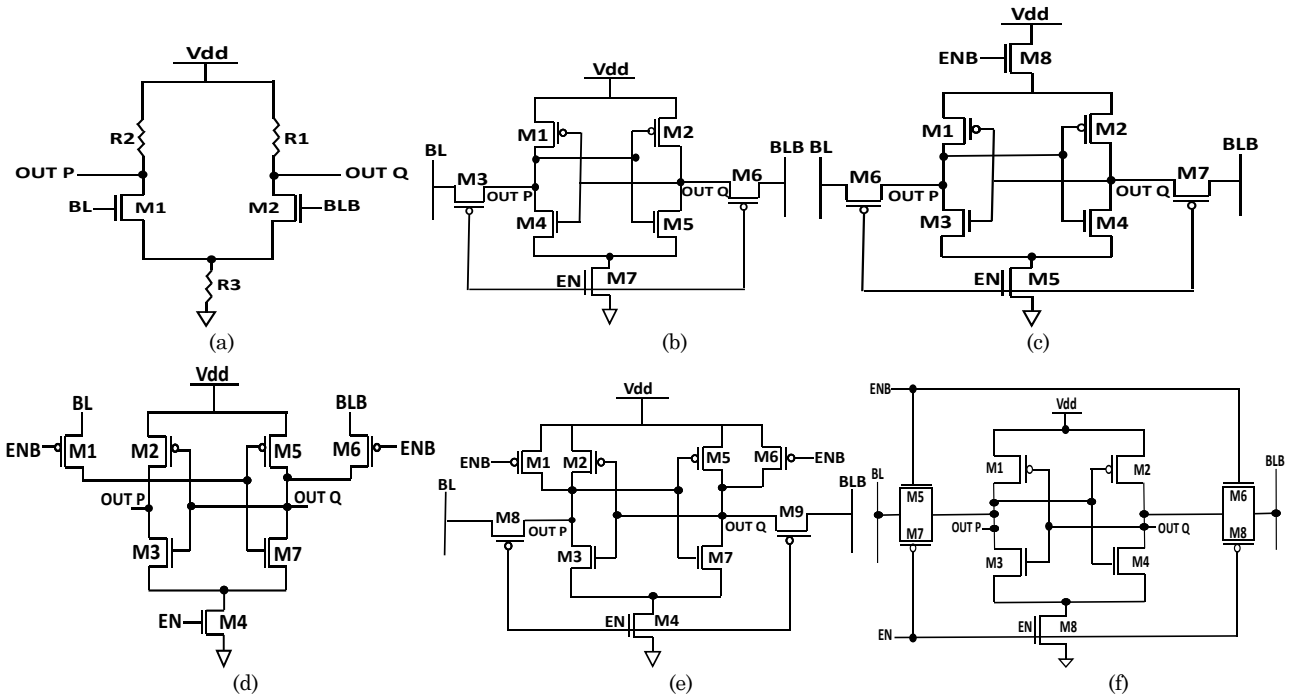


Fig. 1 – Circuit Design for (a) BDVMSA, (b) CCCVMSA, (c) DTCCVMSA, (d) CVLSA, (e) CCLSA, and (f) TGVMSA

This paper focuses on the development of modified DSLR-VMSA based on an LRC. Based on a single supply circuit, the design was created. LRCs offer the necessary positive feedback network for short circuit dissipation. The efficacy of DSLRA-SA is contrasted with prominent extant SAs.

The paper is structured into five sections. The introduction is covered in the first section. The various pre-existing SA topologies are discussed in further detail in section II. Section III provides an explanation of the circuit design, dimensional analysis, features and impact of sleep transistors on the modified SA topology. Whereas, in section IV, the findings of the modified SA are compared with the existing SA topologies explained in section II. Finally, Section V concludes the finding of the paper.

2. SCHEMATIC OVERVIEW OF VARIOUS EXISTING SA TOPOLOGIES

The demands of the modern world are minimal power dissipation and rapid speed, various SA topologies have been reported in the literature for achieving various design objectives such as high packaging density, low power, ideal output, and fast sensing. Some of thepopular SA topologies and their working mechanisms are detailed in this section. All the pre-existing SA topologies discussed in this paper are depicted in Fig. 1. The first SA topology depicted in Fig. 1 (a) was reported in 2019 by Selvakumar *et al.*[10]. It is a basic differential voltage mode sense amplifier (BDVMSA) that contains each component required for sensing. It consists of three resistors (R1, R2, and R3) along with two NMOS transistors. To produce the desired output signal, the BDVSMA circuit amplifies the input signal. Noise rejection is the main application for these circuits [11].

This circuit is able toproduce an ideal output, but its low speed makes it unfit for many applications. The input to the topology is applied via the bit line pair BL and BLB.A small differential input on the bit lines is amplified to full swing output node.

A different SA topology was reported by Na *et al.* [12] in 2013. This topology is referred to as conventional cross coupled voltage mode SA (CCCVMSA) as it is the most conventionally used SA topology. Its simple topology and fast operation make it the de-facto SA topology. The circuit design for the CCCVSMA is presented in Fig. 1 (b). The circuit for the CCCVSMA can be split into four parts: driver transistors, load transistors, access transistors and foot switch transistors. A critical aspect of the CCCVSMA is the Enable (EN) signal. The EN signal has to be used cautiously as the input and output nodes for the circuit are the same. When the EN signal is high, the CCCVMA SA is in its active mode and senses the differential input available at the bitline pair. Another important aspect of this topology is the M7 foot switch NMOS transistor, which enables high drive current in the active mode and restricts the leakage current during standby operation.

To further improve the performance of the CCCVSMA topology in terms of power consumption, energy, and drive current, a double tailed cross coupled VMSA (DTCCVMSA). This topology was reported by Hemaprabha *et al.* [13] in 2015. The circuit topology of DTCCVMSA is similar to CCCVMSA with the exception of an additional PMOS transistor M8. The M8 transistor acts as a head tail transistor as it connects the V_{DD} rail to the cross coupled inverter core; it is controlled by the

enable bar signal (ENB) as depicted in Fig. 1 (c). The main utility of the M5 and M8 transistors are to disconnect the internal core of the SA from the V_{DD} and ground rails, when the cell is in standby mode. Assuming the case when BL is '1'(BLB is '0') and EN is '1'(ENB is '0'), the EN signal results in transistor M5 being turned ON, then the drain node of M5 is charged to OUTQ.

A different SA topology referred to as current latched Voltage Mode SA (CLVMSA) was reported by W. Jinn-Shyann*et al.* [13] in 2014. The schematic diagram for CLVSMA is shown in Fig. 1 (d).The topology for CLVSMA consists of inverter pair formed by transistors M2, M3, M5, and M7. To segregate the input and output nodes for the SA, the M1 and M6 PMOS transistors are utilized. The input is applied via the bitline pair (BL and BLB). The M4 transistor is used to control the drive current for the circuit. The M4 transistor is controlled via the control signal EN. When the EN signal is low, the M4 transistor is off, where as the pass transistors M1 and M6 are ON, and full swing output is amplifying the differential voltage. The circuit provides strong feedback. The enable signal (EN) activates the M4.

In 2016, Gundu et al. presented on another cross coupled latch sense amplifier (CCLSA) topology [14]. Fig. 1 (e) shows the schematic representation for the CCLSA circuit. In this topology, the cross coupled inverter pair is formed by transistor M2, M3, M5 and M7. Two additional transistors - M1 and M6areused for pre-charging the circuit before a read operation is performed. The pre-charging nodes for this topology bestows it with high-speed functionality. Thereby, making it a preferred choice for SA implementation for high-speed circuits, but this results in high power consumption trade-off.The other drawback of this SA topology is current leakage from output node to input node between drain and source of M7 and M8 when EN is active high. Therefore, for proper isolation between the internal and output nodes of the circuit, the EN signal in the circuit should be carefully controlled.

In 2019, Kishore et al. presented a transmission gate-based voltage mode SA (TGVMSA) [15]. Fig. 1 (f) shows the circuit design for the TGVMSA. The circuit is divided into three divisions – load transistors, transmission gate and driver transistor. The working of TGVMSA is same as CCCVMSA; only two additional NMOS transistors M5 and M6 are combined to the access transistors. The combination of NMOS M5 and M6 with PMOS transistors M7 and M8 forms a transmission gate circuit which is also known as analog switch. This combination is connected to bit lines. Power, energy, and delay of TGVMSA are better than that of CCCVMSA.

3. MODIFIED SENSE AMPLIFIER TOPOLOGY

SA is a component of CMOS memories' read circuits. Its main function is to amplify the low differential signal developed on the bit line pair due to discharge current during the read operation, to develop the desired output level to define the data value stored in the memory cell. VMSA are the SA that identifies the bit lines voltage differences. In cross coupled VMSA, back-to-back inverter are connected; the input of first CMOS inverter is connected to output of second and input of second is connected to output of first inverter.

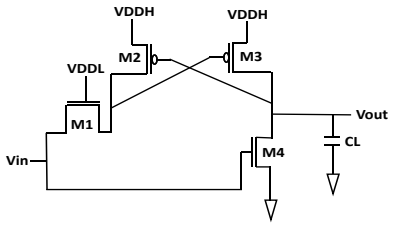


Fig. 2 – Basic LRC along Pass Transistor Logic

A level restoration circuit (LRC) behaves as a voltage swing between a low and a high valid logic level. The stand-by power consumption increases further when the low-swing signal is converted to a full-swing signal using a standard CMOS inverter. Therefore, in order to correctly switch the low-swing signal to a high-swing signal without creating an extreme short-circuit DC current, a LRC must be used as a receiver. Because of their simplicity, the circuits are widely used, although they aren't active enough. Moreover, there is a significant amount of short-circuit dissipation [3].

3.1 Schematic Design of Modified SA

In this paper, Dual Switch Level Restoration Voltage-mode Sense Amplifier (DSLR-VMSA)suggested. The circuit topology for DSLR-VMSA consists of five PMOS transistors (M1, M2, M3, M4 and M5) and five NMOS transistors (M6, M7, M8, M9 and M10).Fig. 3 shows the circuit diagram for the DSLR-VMSA circuit. The design and working of DSLR-VMSA is inspired from the DTCCVMSA, with the exception of a LRC, formed by two additional PMOS transistors(M1 and M2).

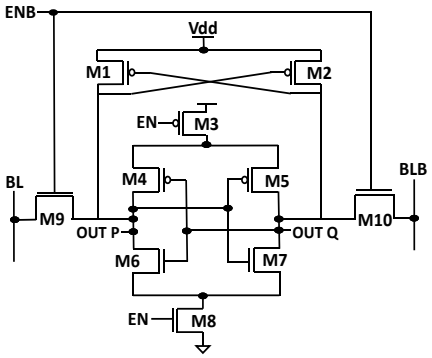
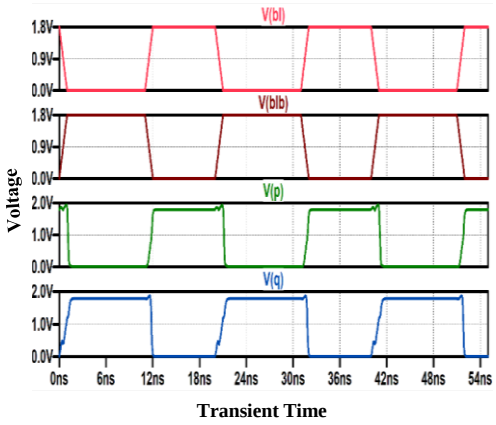


Fig. 3 – Schematic design of Modified SA

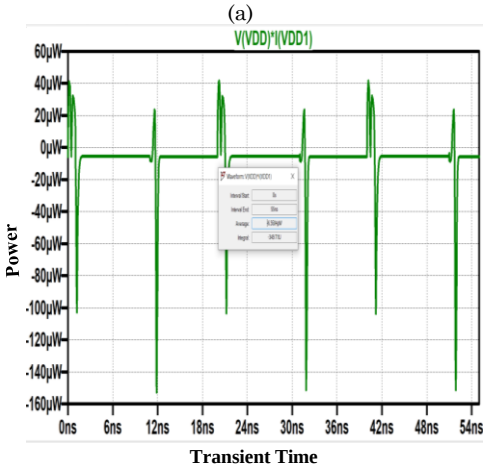
The LRC topology used in the modified SA topology is composed of pass transistors (M1 and M2) connected in a latch type topology. The inputs to the two PMOS transistors are connected to the drain voltages of transistors(M4, M6, M7 and M8).It is also the input node for the modified SA topology, therefore during the read operation, a small differential voltage is developed on the BL-BLB pair [16-17]. When EN is "1" and ENB is "0", the sleep transistors M3 and M4 are turned "ON". Assuming initially bit line BL is high and bit line bar BLB is low and switching transistors are turned "OFF", then output nodes will charge and provide low to high voltage swing.

3.2 Characteristics Analysis of Modified Sense Amplifier

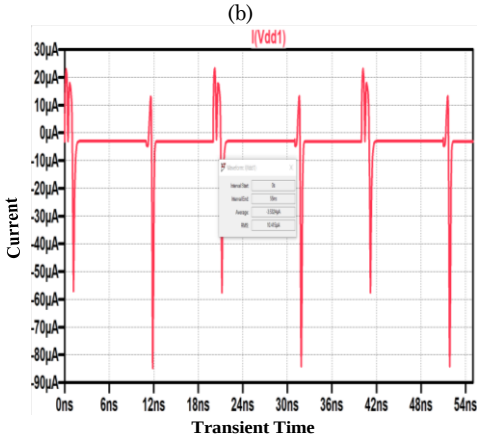
The first round of evaluation for an SA topology is its ability to perform fast sensing operation for minimal differential input voltage on the input nodes. The modified DSLR-VMSA topology's output waveform is depicted and examined.



(a)



(b)



(c)

Fig. 4 – Simulation results of SA (a) output wave form (b) energy andpower analysis (c) current analysis

The modified SA topology is analyzed for all the important parameters necessary for best design considerations such as power, energy, delay, and current [18]. The simulation waveforms corresponding to each of the evaluated parameters for the modified SA topology are depicted in Fig. 4. The modified SA topology is designed for 32 nm technology node and is simulated at 1.8 V supply voltage.

When EN and BL signal both are active high, the output node OUTP follows the BL voltage. Similarly, when the ENB is active low and BL signal is high, the output node OUTQ follows the BLB voltage. The modified SA topology's output waveform can also be used for verification of the same. Another essential parameter while designing an SA topology is its power consumption. With the decreasing technology node, the focus on power consumption has grown exponentially. The power consumption, energy performance for the modified SA topology is depicted in Fig. 4(b). The current performance for the modified SA is depicted in Fig. 4(c). As can be inferred from Fig. 4(b) and (c), the modified SA tends to consume more power and current during the transient operation.

3.3 Effect of Sleep Transistor on Modified SA

An SA topology's power consumption is a significant factor. Power gating is a widely used low power approach in VLSI devices. It relies on switching off the unused portion of circuit to save power consumption for the circuit. Therefore, to reduce the power consumption for the modified SA topology, As a power switch, PMOS and NMOS transistors are added between the supply voltage and ground pins. Power gating technique is also known as sleep transistor technique. Kanika et al. [19] reported sleep transistor impact on SRAM.

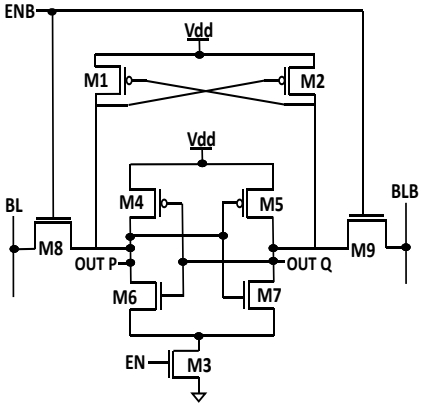


Fig. 5 – Modified SA without head switch

To understand the impact of head switch transistor on the performance of the modified SA, a modified SA without head switch PMOS is analyzed. The circuit design for modified SA is represented in Fig. 5. The modified DSLR-VMSA is compared with the modified SA without head switch in terms of power, energy, and delay.

Table 1 – Effect of sleep transistors on SA

	Power (uW)	Energy (fJ)	Delay (ps)
Modified SA	6.3181	347.5	187.14
Modified SA without Head Sleep Transistor	6.7589	371.74	338.48

3.4 Monte Carlo Analysis on Modified SA

As the technology node decreases, the impact of process variation on the performance of the cell increases. To ensure that process variation does not have a drastic impact on the performance of the modified SA, Monte Carlo analysis is used. For the Monte Carlo analysis, the V_{TH} for each transistor is varied6σ around the mean (standard) V_{TH} value. The analysis is performed for the modified SA for 10,000 data points. The Monte Carlo simulation results for the modified SA is depicted in Fig. 6.

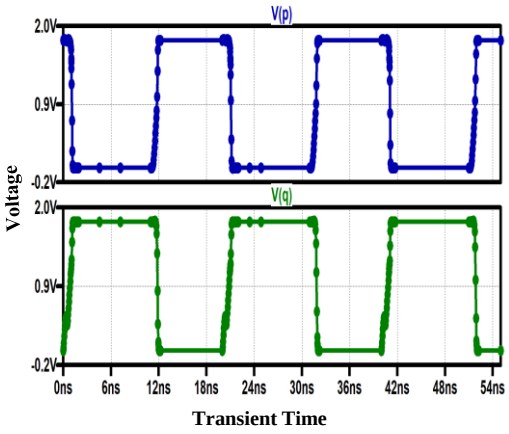


Fig. 6 – Monte Carlo waveform of output P and Q

For Monte Carlo simulations, a model file is used to analyze the possibility of variation in outcome when the arbitration of random variable (in this paper V_{TH} for each transistor) is introduced in the circuit. Threshold voltage variation V_{TH} is varied around 3σ variation which is corelated to μ-3σ, where "μ" is equal to mean and "σ" is equal to standard deviation. The outcomes of the least and maximum process variation of output P and Q are 0 V and 1.8 V. The extent of variation is minimal for the modified SA, which can be observed from the analysis.

3.5 Temperature Analysis

As elaborated in the previous sections, SAs are the heart of CMOS memories in VLSI industry. A wide variety of digital circuits are made to function reliably in a temperature ranges. With the ability to carry devices anywhere and utilize them in any kind of environment, temperature evaluation is an essential. Devices can have different temperatures. In order to investigate how the modified SA design performs differently depending on temperature, a temperature variation analysis is performed.

This analysis is used to ensure the performance reliability for the modified DSLR-VMSA circuit. The temperature variation study is carry outat temperatures varying from (27°-120°) C. The simulation results obtained for the temperature variation analysis is depicted in Fig. 7. It can be inferred from Fig. 7 that the impact

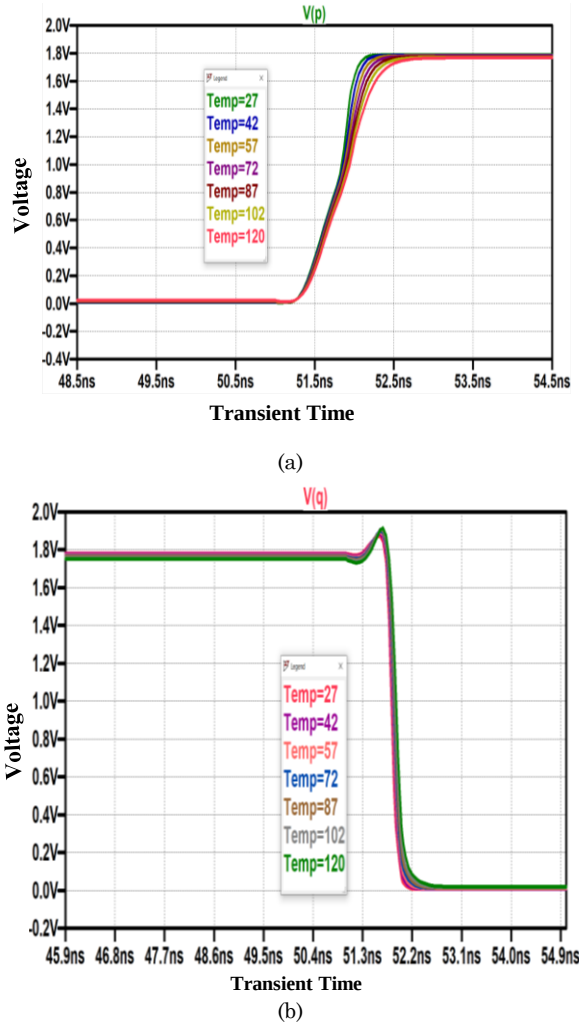


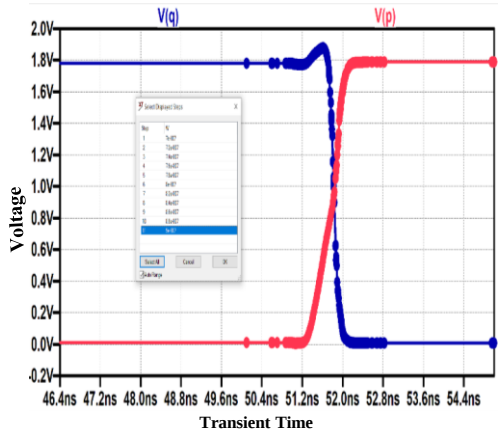
Fig. 7 – Temperature Variations of output P and Q

of temperature variation on the performance of the SA is within the reliable range, as it does not show high variation in its performance. SA's output voltage level varies from 0V to 1.8V. While the modified SA's typical operating range is approximately 84 mV.

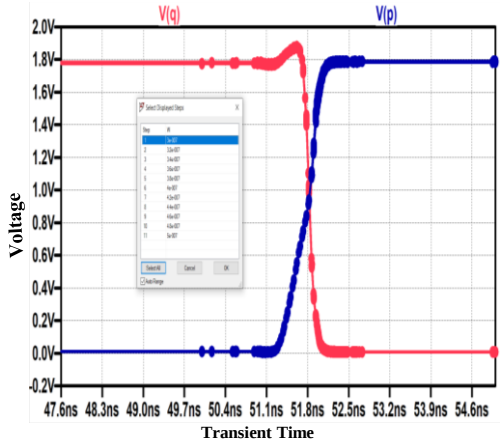
3.6 Dimensional Analysis of Modified Sense Amplifier

The operational speed for an SA is determined as the time elapsed in charging the output nodes of the SA. Therefore, to ensure faster operation, it is mandatory to correctly design the circuit topology to charge output nodes through pre-charge transistors in minimum time.

To achieve the same, dimensional analysis is performed for the modified DSLR-VMSA circuit. The range of aspect ratios and their best values for transistor are tabulated in Table II. The output waveform corresponding to variation in aspect ratio of driver transistors and load transistors is depicted in Fig. 8. The same is done to identify the perfect pull-up ratio and cell ratio [20] for the modified DSLR-VMSA circuit. The channel length for all driver and load transistors is maintained at 180 nm. While, the width for the transistors M4, M5, M6, and M7 are maintained at 900, 900, 300, and 300 nm respectively.



(a)



(b)

Fig. 8 – Output waveform when width is varied for (a) P_{mos} (700-900 nm), and (b) N_{mos} (300-500 nm)

Table 2 – Aspect Ratios of Transistors

Transistor	Range (nm)	Best Dimension (nm)
M4, M5 (W)	700-900	900
M6, M7 (W)	300-500	300
M4, M5 (L)	180	180
M6, M7(L)	180	180

The modified SA is developed by modifying the pre-existing SA topologies in order to create a SA that can minimize the amount of time needed to charge the output nodes and store and amplify low voltage variations to the necessary logic level. From Fig. 8(a) and (b), it can be deduced that the fastest output node charging occurs when the aspect ratios of the driver and load transistors are, respectively, 900/180 nm and 300/180 nm. This approach can increase SA's speed.

4. PERFORMANCE COMPARISON OF EXISTING SA WITH MODIFIED SA

In the preceding section, the circuit topology, operation, and performance of the modified DSLR-VMSA circuit is elaborated upon. But it is equally important to compare the performance of the modified DSLR-VMSA circuit with the different pre-existing SA topologies explained in section II. Therefore, This section presents a comparative performance analysis of different cross coupled voltage mode SAs with changed SA. The four main design parameters taken into consideration in this paper are speed, delay, power, and energy.

4.1 Delay Analysis

The growing interest in high-speed circuits, the delay utilized by a circuit becomes a primal factor in determining the utility of the VLSI circuits [22-23]. Propagation delay of logic circuit is defined as time needed for output voltage to hold out the midway between the 0 and 1 logic levels, i.e., half (50%) of V_{DD}. The delay performance for the different SA topologies along with the modified SA topology is compared in Fig. 9.

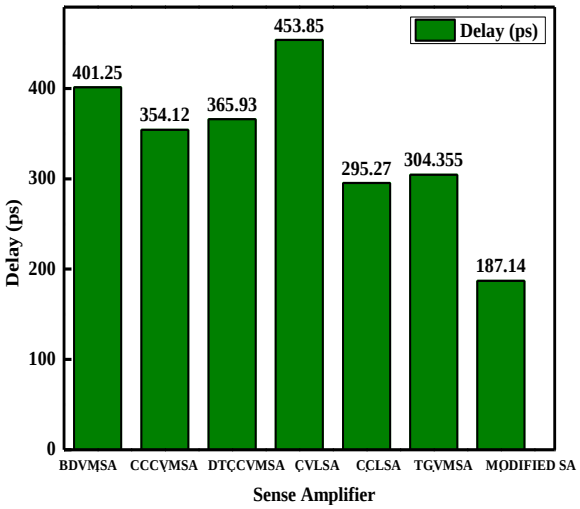


Fig. 9 – Graphical comparison of delay values obtained for the different SA topologies

It can be inferred from Fig. 9 that the DSLR-VMSA has the least delay requirement of 187.14 ps amongst the other SA topologies. Therefore, in terms of delay performance, the DSLR-VMSA is the best choice. For the ease of comparison, the delay values obtained for all the SA topologies are summarized in Table 3.

4.2 Current Analysis

The current flow through the circuit determines the charging/discharging rate for the circuit. Therefore, the current flow through an SA topology is an important performance parameter. It also helps to determine the static power estimate for the circuit. The current flow through the different SA circuits is graphically compared in Fig. 10. Current (I) equals to power divided by voltage ($I = P/V$). Here, we have calculated the average current passing towards the output nodes. It can be inferred from Fig. 10 that CCCVMSA has the lowest current flow through the circuit, whereas, the CCLSA topology possess the maximum current of 38.013 μA. The high current value for the CCLSA is due to its transistor count and dual voltage source. The current requirement for the modified DSLR-VMSA design is moderate, but it consumes lowest power (explained in the subsequent section).

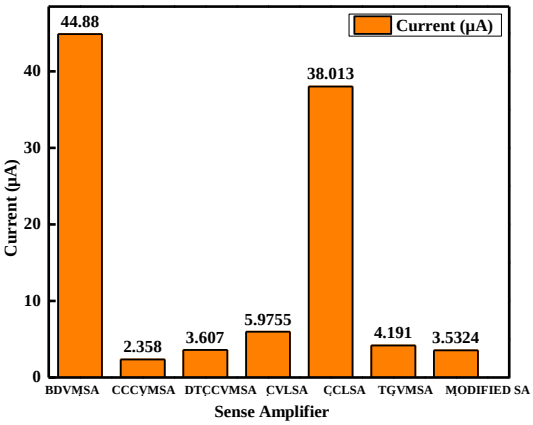


Fig. 10 – Graphical comparison of current values obtained for the different SA topologies

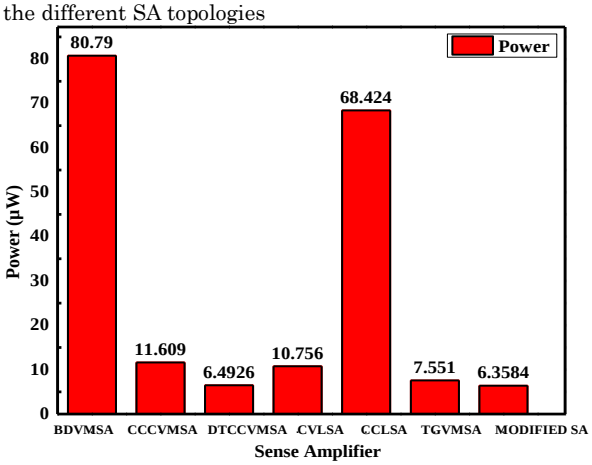


Fig. 11 – Graphical comparison of power consumption values obtained for the different SA topologies

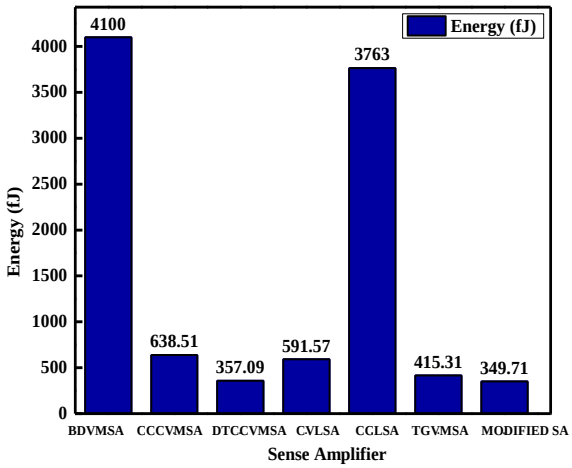


Fig. 12 – Graphical comparison of energy values obtained for the different SA topologies

4.3 Power and Energy Analysis

Energy and power consumption are two principal parameters for all digital circuits. The increasing need for low-power appliances has led to increased interest in the study of reducing the energy and power consumption of sense amplifiers [24-25]. As the two parameters (energy and power) for a digital circuit are of primal importance, the energy and power performance for all the SA topologies are also evaluated.

Here, Power (P) = $V \times I$

The energy and power consumption values obtained for the different SA topologies are graphically compared in Fig. 11 and Fig. 12 respectively and tabulated in table III. Amongst the different existing SAs, DSLR-VMSA has the lowest power consumption and the least amount of energy.

Table 3 – Comparison of SA configuration designed at 180nm technology node and evaluated for 1.8 V supply [10]

Sense Amplifier	Power (uW)	Energy (fJ)	Delay (ps)	Current (uA)	Transistor Count
BDVMSA	80.79	4100	401.25	44.88	**2**
CCCVMSA	11.609	638.51	354.12	2.358	7
DTCCVMSA	6.4926	357.09	65.93	3.607	8
CVLSA	10.756	591.57	453.85	5.9755	7
CCLSA	68.424	3763	295.27	**38.013**	9
TGVMSA	7.551	415.31	304.35	4.191	9
MODIFIED SA	**6.3584**	**349.7**	**187.1**	3.5324	10

Table 3 provides comparative statistics of the parameters of each SA analyzed for 1.8V, including transistor count, power, switching energy delay, and current.

CONCLUSION

In this paper, Dual Switch Level Restoration Voltage-mode Sense Amplifier (DSLR-VMSA) has been reported to reform the performanceof sense amplifier. The SA is developed using a 1.8 V power supply and a 32nm technology node. Using a 55 ns pulse width, a comparative transient analysis is performed for each SA and modified SA. For high speed and low power consumption, the (DSLR-VMSA) is primarily modified. The simulated findings modified that the improved SA has the lowest power, measuring 6.358 μW. When considering the current SAs examined in the paper, this is a significant improvement. For DSLR-VMSA, four more analyses have been conducted, and the results indicate that the updated design is the best option. The power increases, exactly like in the case without sleep transistors. Circuits requiring less power are intended to use the DSLR-VMSA.

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Удосконалений підсилювач чутливості малої потужності з використанням методу відновлення рівнів та порівняння продуктивності з існуючими топологіями за технологією 32 нм

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Підсилювачі зчитування (SA) є важливими в периферійних схемах статичної оперативної пам'яті (SRAM). Вони підвищують швидкість роботи, мінімізують споживання енергії та зменшують час доступу. У цій статті представлено модифікований та вдосконалений підсилювач зчитування з подвійним перемиканням рівнів напруги відновлення (DSLR-VMSA). Для моделювання конструкції використовувалися робоча напруга 1,8 В та 32-х нанометровий технологічний вузол. Порівняльний аналіз з усталеними топологіями підсилювачів зчитування за такими параметрами, як споживання енергії, енергоефективність, затримка та струмові характеристики, показує переважну продуктивність DSLRA-SA. Примітно, що ця вдосконалена схема досягає споживання енергії 6,7 мкВт, що вдвічі менше, ніж у звичайного підсилювача зчитування з перехресним зв'язком напруги та фіксацією (CCVLSA). Показники енергії та затримки також демонструють помітні покращення. Дослідження включає поглиблений аналіз, такий як розмірний, метод Монте-Карло та температурний аналіз, а також оцінку впливу транзисторів сну, для підтвердження продуктивності покращеного підсилювача сну. Включення транзисторів сну в модифіковану конструкцію додатково зменшує споживання енергії, затримку та енергоспоживання, значно підвищуючи загальну продуктивність. Результати підкреслюють придатність та перевагу покращеного SA, особливо для застосувань малопотужних CMOS SRAM.

Ключові слова: Підсилювач чутливості, Відновлення рівня, Транзистор, Затримка, Струм, Аналіз Монте-Карло.