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REGULAR ARTICLE

An Improved Low Power Sense Amplifier Using Level Restoration Technique at 32 nm Technology

Divya* ✉, Neha Goel†, Renu Rani, Hashmat Usmani

Department of ECE, Raj Kumar Goel Institute of Technology, Ghaziabad, India

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Sense amplifiers (SA) are essential in the peripheral circuitry of Static Random Access Memory (SRAM). They enhance operational speed, minimize power consumption, and reduce access time. This paper introduces a modified and enhanced Dual Switch Level Restoration Voltage-mode Sense Amplifier (DSLR-VMSA). An operational voltage of 1.8 V and a 32 nm technology node were used to simulate the designreveals DSLRA-SA's superior performance. Notably, this improved circuit achieves a power consumption of 6.7 uW, half that of the conventional Cross-Coupled Voltage Latch Sense Amplifier (CCVLSA). Energy and delay metrics also exhibit marked improvements. The study includes in-depth analyses such as Dimension and Temperature analyses, as well as evaluations on the impact of sleep transistors, to validate the enhanced SA's performance. Incorporating sleep transistors in the modified design further reduces power, delay, and energy consumption, significantly enhancing overall performance. The results underscore the suitability and superiority of the improved SA, particularly for low-power CMOS SRAM applications.

Keywords: Sense amplifier, Level restoration, Sleep transistor, Delay, Current, Temperature.

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1. INTRODUCTION

In modern CMOS memory circuits, the power and speed performance of sense amplifier is a critical aspect [1-3]. Amongst the different memory topologies, the embedded SRAM is the fastest, but it is usually the most powerful-hungry memory. The SRAM operates solely when a supply voltage (V_{DD}) is present in the circuit. This means that data is retained within the memory cell when V_{DD} is applied but is lost when V_{DD} is disconnected (turned off). SRAM is typically integrated within System on Chips (SOCs)for quick operation and is referred to as cache. The major performance parameters for SRAM are energy consumption, leakage current, power utilization and propagation delay required for the circuit. Additionally, Reducing the circuit's power consumption, size, and latency has become a key design goal due to the growing need for low-power portable digital devices.

An important component of the SRAM peripheral circuit is the sense amplifier. Sense amplifiers play a crucial role in the operation of RAM, DRAM, and SRAM cells by facilitating the accurate reading of their contents. Due to their high sensitivity to noise, their design ensures robust noise margins to guarantee reliable data representation from each memory cell. There exist two primary types of sense amplifiers: static sense amplifiers, employed in static RAMs and SRAMs to detect logic states, and dynamic

Sense amplifiers, utilized to conserve energy during low power consumption phases.

The significance of fast sense amplifiers lies in their ability to minimize latency in various circuits, particularly in tasks like bit-line reading within memory systems. As CMOS chips advance towards sub-micrometer scales, minimizing on-chip delays caused by interconnections becomes increasingly critical. Fast sense amplifiers serve as essential repeaters for high-speed signals that need to traverse large chip distances efficiently.

Aspect ratio is another important factor that affects the operational effects in relation to the voltage level. To ensure optimized aspect ratios are utilized for circuit evaluation, dimensional analysis is employed for determining pull up and cell ratio for the modified SA topology. The study is examined in supplementing part of this paper. The modified SA topology is designed based on the different SA topologies already reported in the literature. The different categories of the SA topology include single and double ended, voltage mode, current mode, charge transfer mode and latch type SA etc. [4-6]. Amongst the different SA topologies, the cross coupled voltage mode SA (VMSA) is reported to have optimal performance. The feature that deems the cross coupled

* Correspondence e-mail: divyaa.dutt13@gmail.com
† 17nehagoel@gmail.com

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latch type SA better than others due to its no static current through the circuit. Therefore, low power cache implementation requires extensive analysis and planning, as well as the output of the highest performing VMSA and appropriate circuit operation. Power, speed, transistor count area, and aspect ratio are the primary design factors to be taken into account [7-8]. Transistors are typically utilized in circuits with fewer space requirements in lower numbers. The impact of adding or removing head and foot switch sleep transistors has been studied in order to investigate the same. High speed and low power, energy, and area SAs are regarded as the best SA topologies.

This paper focuses on the development of modified DSLR-VMSA based on an LRC. Based on a single supply circuit, the design was created. LRCs offer the necessary positive feedback network for short circuit dissipation. The efficacy of DSLR-VMSA is contrasted with prominent extant SAs.

The paper is structured into various sections. The introduction is covered in the first section. Section II provides an explanation of the circuit design, dimensional analysis, features, temperature analysis and impact of sleep transistors on the modified SA topology. Finally, last section concludes the finding of the paper.

2. MODIFIED SENSE AMPLIFIER TOPOLOGY

SA is a component of CMOS memories' read circuits. Its main function is to amplify the low differential signal developed on the bit line pair due to discharge current during the read operation, to develop the desired output level to define the data value stored in the memory cell. VMSA are the SA that identifies the bit lines voltage differences. In cross coupled VMSA, back-to-back inverters are connected; the input of first CMOS inverter is connected to output of second and input of second is connected to output of first inverter.

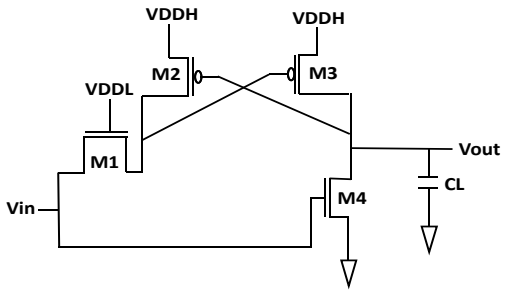

Fig. 1 – Basic LRC along Pass Transistor Logic

A level restoration circuit (LRC) behaves as a voltage swing between a low and a high valid logic level. Fig. 1 depicts basic LRC along Pass Transistor Logic. The stand-by power consumption increases further when the low-swing signal is converted to a full-swing signal using a standard CMOS inverter. Therefore, in order to correctly switch the low-swing signal to a high-swing signal without creating an extreme short-circuit DC current, a LRC must be used as a receiver. Because of their simplicity, the circuits are widely used, although they aren't active enough. Moreover, there is a significant amount of short-circuit dissipation [9].

2.1 Schematic Design of Modified SA

In this paper, Dual Switch Level Restoration Voltage-mode Sense Amplifier (DSLR-VMSA) suggested [10]. The circuit topology for DSLR-VMSA consists of five PMOS transistors (M1, M2, M3, M4 and M5) and five NMOS transistors (M6, M7, M8, M9 and M10).Fig. 2 shows the circuit diagram for the DSLR-VMSA circuit. The design and working of DSLR-VMSA is inspired from the Dual Tail Cross Coupled Voltage Mode SA, with the exception of a LRC, formed by two additional PMOS transistors (M1 and M2) [11-12].

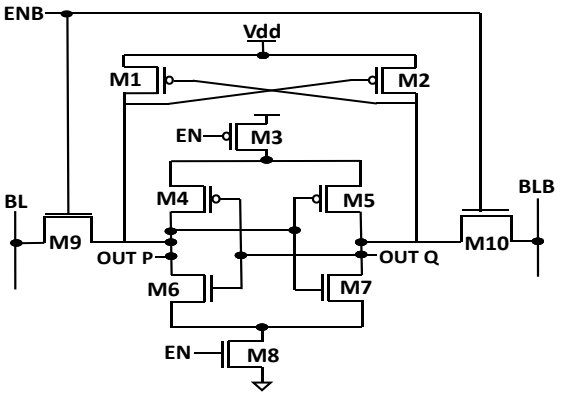

Fig. 2 – Schematic design of Modified SA

The LRC topology used in the modified SA topology is composed of pass transistors (M1 and M2) connected in a latch type topology. The inputs to the two PMOS transistors are connected to the drain voltages of transistors (M4, M6, M7 and M8).It is also the input node for the modified SA topology, therefore during the read operation, a small differential voltage is developed on the BL-BLB pair [13-14]. When EN is "1" and ENB is "0", the sleep transistors M3 and M8 are turned "ON". Assuming initially bit line BL is high and bit line bar BLB is low and switching transistors are turned "OFF", then output nodes will charge and provide low to high voltage swing.

2.2 Characteristics Analysis of Modified Sense Amplifier

The first round of evaluation for an SA topology is its ability to perform fast sensing operation for minimal differential input voltage on the input nodes. The modified DSLR-VMSA topology's output waveform at 32 nm node is depicted and examined in Fig. 3.

The modified SA topology is analyzed for all the important parameters necessary for best design considerations such as power, energy, delay, and current [15]. The simulation waveforms corresponding to each of

the evaluated parameters for the modified SA topology are depicted in Fig. 3. The modified SA topology is designed for 32 nm technology node and is simulated at 1.8 V supply voltage.

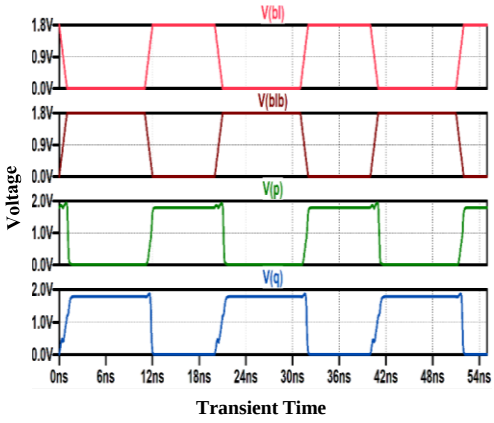

Fig. 3 – Output Analysis Of DSLR-VMSA

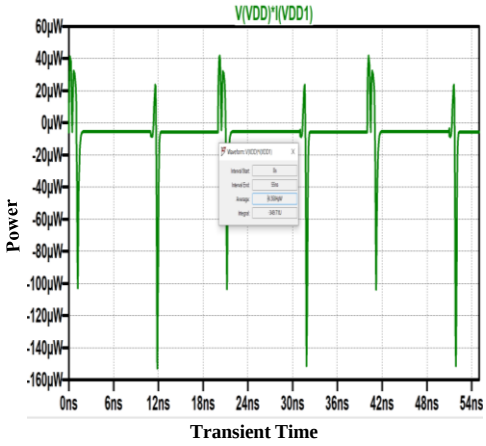

Fig. 4 – Power and Energy output Of DSLR-VMSA

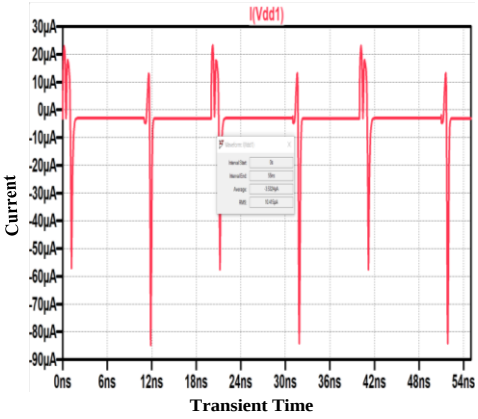

Fig. 5 – Current output of DSLR-VMSA

When EN and BL signal both are active high, the output node OUTP follows the BL voltage. Similarly, when the ENB is active low and BL signal is high, the output node OUTQ follows the BLB voltage. The modified SA topology's output waveform can also be used for verification of the same. Another essential parameter while designing an SA topology is its power consumption. With the decreasing technology node, the focus on power consumption has grown exponentially.

Here, Power (P) = $V \times I$

The power consumption, energy performance for the modified SA topology is depicted in Fig. 4.

The current performance for the modified SA is depicted in Fig. 5. As can be inferred from Figure, the modified SA tends to consume more power and current during the transient operation.

2.3 Effect of Sleep Transistor on Modified SA

An SA topology's power consumption is a significant factor. Power gating is a widely used low power approach in VLSI devices [16]. It relies on switching off the unused portion of circuit to save power consumption for the circuit. Therefore, to reduce the power consumption for the modified SA topology, As a power switch, PMOS and NMOS transistors are added between the supply voltage and ground pins [17]. Power gating technique is also known as sleep transistor technique.

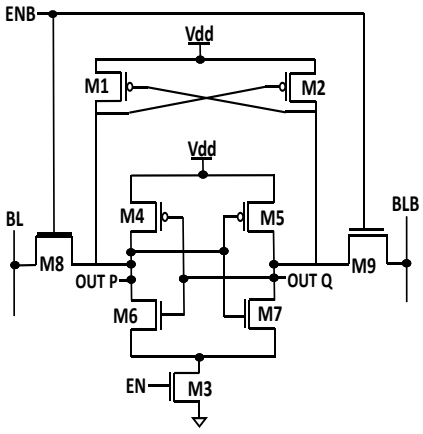

Fig. 6 – Modified SA without head switch

To understand the impact of head switch transistor on the performance of the modified SA, a modified SA without head switch PMOS is analyzed. The circuit design for modified SA is represented in Fig. 6. The DSLR-VMSA is compared with the modified SA without a head switch in terms of power, energy, and delay shows in Table 1.

Table 1 – Effect of sleep transistors on SA

	Power (uW)	Energy (fJ)	Delay (ps)
Modified SA	6.3181	347.5	187.14
Modified SA without Head Sleep Transistor	6.7589	371.74	338.48

2.4 Temperature Analysis

As elaborated in the previous sections, SAs are the heart of CMOS memories in VLSI industry. A wide variety of digital circuits are made to function reliably in a temperature ranges. With the ability to carry devices anywhere and utilize them in any kind of environment, temperature evaluation is an essential [18]. Devices can have different temperatures. In order to investigate how the modified SA design performs differently depending on temperature, a temperature variation analysis is performed.

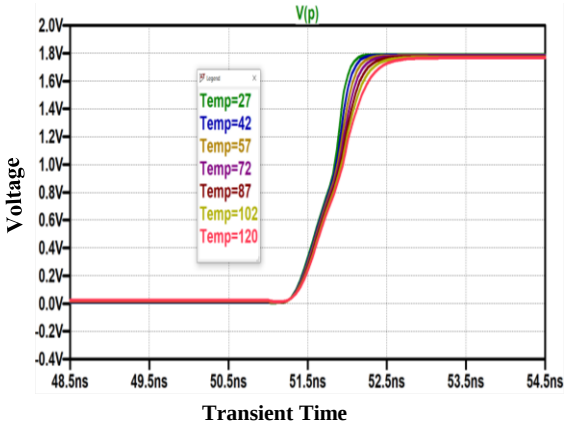

Fig. 7 – Temperature variation of output P

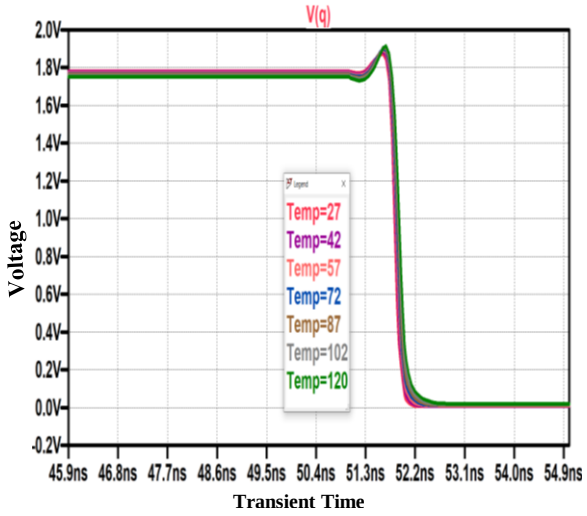

Fig. 8 – Temperature Variation of Output Q

This analysis is used to ensure the performance reliability for the modified DSLR-VMSA circuit. The temperature variation study is carry out at temperatures varying from (27°-120°) °C. The simulation results obtained for the temperature variation analysis is depicted in Fig. 7 and 8. It can be inferred from Fig. 7 and 8 that the impact of temperature variation on the performance of the SA is within the reliable range, as it does not show high variation in its performance. SA's output voltage level varies from 0 V to 1.8 V. While the modified SA's typical operating range is approximately 84 mV.

2.5 Dimensional Analysis of Modified Sense Amplifier

The operational speed for an SA is determined as the time elapsed in charging the output nodes of the SA. Therefore, to ensure faster operation, it is mandatory to correctly design the circuit topology to charge output nodes through pre-charge transistors in minimum time.

To achieve the same, dimensional analysis is performed for the modified DSLR-VMSA circuit. The range of aspect ratios and their best values for transistor are tabulated in Table 2. The output waveform corresponding to variation in aspect ratio of driver transistors and load transistors is depicted in Fig. 9 and Fig. 10. The same is done to identify the perfect pull-up ratio and cell ratio for the modified DSLR-VMSA circuit. The channel length for all driver and load transistors is maintained at 180 nm. While the width for the transistors M4, M5, M6, and M7 are maintained at 900, 900, 300, and 300 nm respectively.

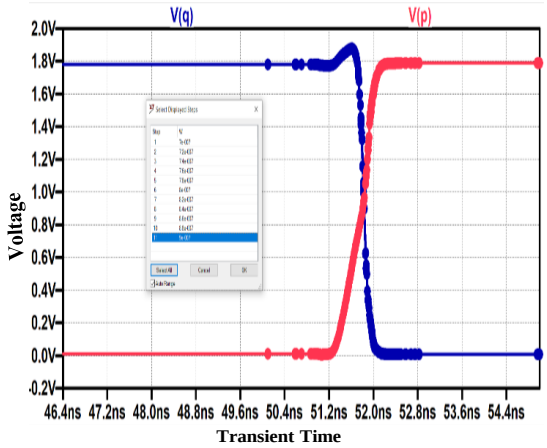

Fig. 9 – Output waveform when width is varied for *P*mos(700-900nm)

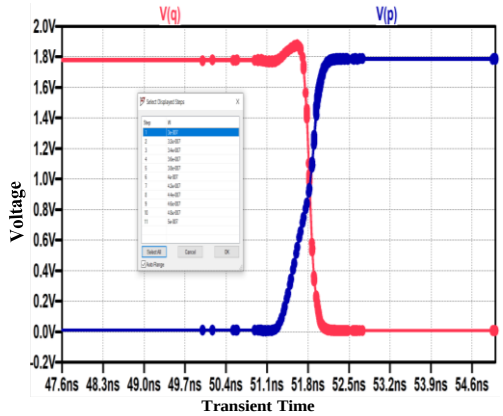

Fig. 10 – Output waveform when width is varied for *N*mos(300-500nm)

Table 2 – Aspect Ratios of Transistors

Transistor	Range (nm)	Best Dimension (nm)
M4, M5 (W)	700-900	900
M6, M7 (W)	300-500	300
M4, M5 (L)	180	180
M6, M7(L)	180	180

The modified SA is developed by modifying the pre-existing SA topologies in order to create a SA that can minimize the amount of time needed to charge the output nodes and store and amplify low voltage variations to the necessary logic level. From Fig. 9 and 10, it can be deduced that the fastest output node charging occurs when the aspect ratios of the driver and load transistors are, respectively, 900/180 nm and 300/180 nm. This approach can increase SA's speed.

3. CONCLUSION

In this paper, Dual Switch Level Restoration Voltage-mode Sense Amplifier (DSLR-VMSA) has been reported to reform the performance of sense amplifiers. The SA is developed using a 1.8 V power supply and a 32 nm technology node. Using a 55 ns pulse width, a transient analysis is performed for modified SA. For high speed and low power consumption, the (DSLR-VMSA) is primarily modified. The simulated findings modified that the improved SA has the lowest power, measuring 6.358 μW. When considering the current SAs examined in the paper, this is a significant improvement. For DSLR-VMSA, four more analyses have been conducted, and the results indicate that the updated design is the best option. The power increases, exactly like in the case without sleep transistors. Circuits requiring less power are intended to use the DSLR-VMSA.

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Покращений підсилювач малої потужності з використанням техніки відновлення рівня за технологією 32 нм

Divya, Neha Goel, Renu Rani, Hashmat Usmani

Department of ECE, Raj Kumar Goel Institute of Technology, Ghaziabad, India

Підсилювачі чутливості (SA) є важливими в периферійних схемах статичної пам'яті з довільним доступом (SRAM). Вони підвищують швидкість роботи, мінімізують енергоспоживання та скорочують час доступу. У цьому документі представлено модифікований і вдосконалений підсилювач чутливості в режимі напруги з подвійним перемикачем відновлення рівня (DSLR-VMSA). Робоча напруга 1,8 В і технологічний вузол 32 нм використовувалися для моделювання конструкції, що демонструє чудову продуктивність DSLRA-SA. Примітно, що ця вдосконалена схема забезпечує споживання електроенергії 6,7 мкВт, що вдвічі менше, ніж у звичайного підсилювача фіксації напруги з крос-зв'язком (CCVLSA). Показники енергії та затримки також демонструють помітні покращення. Дослідження включає поглиблений аналіз, такий як аналіз розмірів і температури, а також оцінки впливу транзисторів в режимі сну, щоб підтвердити покращену продуктивність SA. Включення транзисторів в модифіковану конструкцію додатково зменшує потужність, затримку та споживання енергії, значно підвищуючи загальну продуктивність. Результати підкреслюють придатність і перевагу вдосконаленої SA, особливо для додатків CMOS SRAM з низьким енергоспоживанням.

Ключові слова: Підсилювач чутливості, Відновлення рівня, Транзистор в режимі сну, Затримка, Струм, Температура.