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REGULAR ARTICLE

A 1-GHz 180 nm CMOS Power Amplifier for UHF RFID Reader Systems

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This paper describe a CMOS single-ended power amplifier (PA) designed for use in a UHF (Ultra-High Frequency) RFID (Radio Frequency Identification) reader system-on-chip (SoC). CMOS technology is used in this work thanks to its low power consumption, high integration capabilities, and compatibility with digital logic circuits. Moreover, RFID is a rapidly growing field with numerous emerging technologies and applications. RFID is a technology that uses radio waves to identify and track objects, people, or animals through the use of RFID tags or transponders. These tags contain electronically stored information that can be read remotely using RFID readers or scanners. RFID systems rely on various components, including power amplifiers, to efficiently read and transmit information between RFID tags and readers. Indeed, power amplifiers play a crucial role in these systems by boosting the signal strength, which can significantly impact system performance. In this paper, we present a PA for a RFID system and more particularly the design of a passive RFID reader in the UHF band at a frequency of 1000 MHz and in CMOS 180 nm technology. The proposed amplifier is highlighted for its outstanding efficiency, making it suitable for RFID applications requiring long reading ranges and operation in challenging environments.

Keywords: Radio frequency identification, Power amplifier, CMOS technology, Layout circuit on cadence, 180 nm CMOS.

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1. INTRODUCTION

RFID, also known as Radio Frequency Identification, is a sophisticated wireless communication technology that operates through the utilization of radio waves by a reader to capture and interpret data that has been encoded within tags [1]. The primary purpose of this advanced technology is to streamline and enhance the process of automatically identifying distant objects that have been outfitted with RFID tags, thereby enabling seamless data collection and management. Given the substantial growth of the global RFID market, RFID has become a pivotal focus of research in contemporary industry [2-4]. Because of its benefits in contrast to barcodes and high-frequency (HF) RFID, especially in terms of extended detection range and increased data transfer speed, ultra-high-frequency (UHF) RFID technology has found use in a wide range of fields. These include medical applications, localization services, construction, transportation, security, military applications, and logistics. The utilization of RFID drives hardware developers to include readers in portable devices, benefiting consumers. Efforts in IC design focus on creating a single-chip solution for RFID systems [5-7]. Designing a CMOS power amplifier for RFID systems is challenging due to inherent limitations. The amplifier must have high output power, efficiency, and linearity, which is a formidable task.

Research carried out to proposed a highly efficient PA for UHF RFID system. Authors of Ref. [8] introduced a new of a fully integrated CMOS power amplifier (PA) operating in the frequency range of 860-960 MHz for UHF RFID transmitters. The design employs a three-stage differential structure, which includes the following key elements: a Common-Source Structure with RC Feedback and a Cascade Structure with Self-Biased Cascode and SFBB Technique. In [9], authors proposed power amplifiers that is characterized by low power consumption, high efficiency, and integration is a crucial area of research with substantial implications for both communication and circuit studies. To enhance the power and integration while keeping costs down, authors of Ref. [9] introduced a CMOS power amplifier designed to operate in the 3.5 GHz to 4.5 GHz frequency range. The design incorporates a cascode driver stage, which confers upon the power amplifier an impressive output gain capability. The simulation results demonstrate that the proposed power amplifier in [9] outperforms others, offering a 31.2 % increase in power-added efficiency (PAE) and an output power gain of 12.6 dB, respectively. This PA could be used for applications such as RFID and the Internet of Things (IoT). Ibrahim et al. have proposed in [10] a transceiver tailored for passive RFID tags that operates at low power and offers high data rates. To address the power constraints inherent in passive RFID systems while achieving improved data rates, an asymmetric communication link is employed between the reader and the tag. The proposed transceiver is meticu-

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lously designed and rigorously simulated using 28-nanometer CMOS technology. This innovative approach seeks to balance power efficiency with high data rates, making it a promising solution for enhancing passive RFID tag systems. In [11], a fully integrated UHF band differential PA with an output power of 30 dBm has been designed and fabricated using 180nm CMOS technology. The high-power PA design incorporates a transformer-type combiner and involves a comprehensive analysis and optimization of the proposed transformer network and the number of power cells to determine the dimensions of the inductors. This combination results in improved performance characteristics. Specifically, the PA achieves an output power of 29 dBm and a power-added efficiency of 24 %, while also delivering a power gain of 20 dB. These performance metrics take into account the losses introduced by the bond-wire connections. Authors of Ref. [12] discussed a two-stage fully integrated power amplifier (PA) designed for the 802.11a standard. The PA has been fabricated using UMC 180 nm CMOS technology. The amplifier demonstrates noteworthy performance in terms of power gain, P1 dB, PSAT, and PAE, with a particular focus on the design and use of power inductors to enhance efficiency and withstand high current levels. Other researchs findings indicate that fully integrated class-E CMOS power amplifiers can achieve remarkable efficiency, surpassing 40 % [13], and can even reach levels exceeding 60 % when external matching components are introduced [13]. On the other hand, linear power amplifiers implemented in CMOS tend to exhibit significantly lower efficiency when operating at linear output power, various research works have extensively recorded the progress of CMOS linear power amplifiers designed for the specific use in wireless local area network (WLAN) applications. These amplifiers typically exhibit power-added efficiency (PAE) values that vary between 15 % and 25 % at the 1-dB gain-compression point (P1dB) as shown in studies [14, 15].

In this work, a CMOS PA for UHF RFID reader is proposed. The PA has been designed using 180 nm CMOS technology. The amplifier demonstrates noteworthy performance in terms of output voltage in DC-simulation. AC simulation was also given. Moreover, the layout of a CMOS power amplifier is discussed and analyzed in this paper. The layout refers to the physical arrangement of transistors, passive components, interconnections, and metal layers on a semiconductor chip. It plays a crucial role in determining the performance, power consumption, and manufacturability of the CMOS power amplifier. So that, this work described the design process for the layout, including the arrangement of transistors and other components to meet the desired specifications such as power gain, bandwidth, and efficiency. the paper would provide insights into the optimization of the proposed amplifier for UHF RFID applications.

Figure 1 presents a simplified block diagram of the transmitter (Tx) section of the RFID reader. The process begins with the output signal from the reconstruction filter, which is then converted into the UHF band by the up-conversion mixer. Subsequently, the modulated RF signal is transmitted to the antenna via the power amplifier. The power amplifier amplifies the signal to achieve the desired power levels for transmission. It is an important part of ensuring that the signal reaches the antenna with sufficient strength for effective communication.

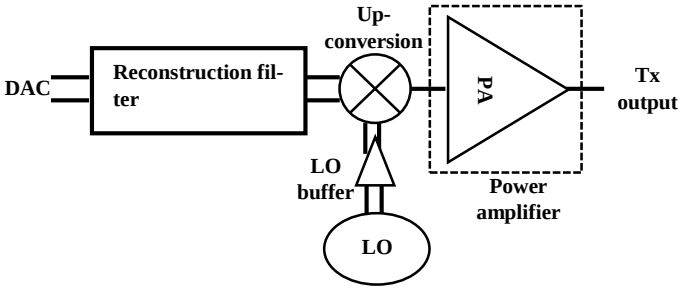

Fig. 1 – The block diagram of RFID reader system

In this paper, the focus is on the design and implementation of a PA specifically intended for RFID reader system-on-chip (SoC) applications. The CMOS-based on-chip driver power amplifier is designed with certain key features and characteristics to enhance the overall performance of the power amplifier. When designing the proposed PA, we determine first the frequency range at which the power amplifier will operate which is in our case 1GHz. CMOS technology is used in this work because it allows for the design of efficient power amplifiers that maximize power conversion from the supply voltage to the RF output power.

2. CMOS POWER AMPLIFIER DESIGN

The power transistor plays a pivotal role in determining the maximum achievable output power and efficiency in this study. To safeguard the transistors from breakdown, a cascade topology is employed. Figure 1 provides an illustration of the 1-GHz CMOS power amplifier, purpose-built for mobile RFID reader applications.

3. SYSTEM MODEL

3.1 DC Simulation

DC analysis is a simulation technique in electronics that makes it possible to calculate the stable state of an electronic circuit after an infinitely long time, that is to say when the transients have disappeared and the circuit has reached an electrical equilibrium. This analysis is essential to understand the static behavior of an electronic circuit under constant polarization or operating conditions. Figure 3 show the DC analysis of the proposed PA.

3.2 AC Simulation

AC analysis, also known as small-signal analysis, is a technique used in electronics to analyze the behavior of electronic circuits with varying (time-varying) input signals. It is particularly useful for understanding how a circuit responds to small changes or variations around a specific operating point, often referred to as the quiescent or bias point. Figure 4 show the AC simulation of the proposed PA.

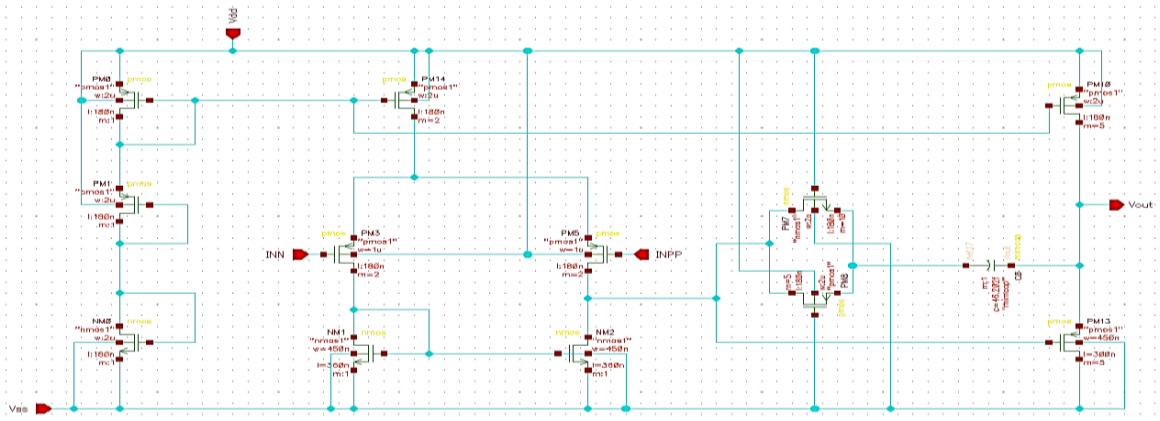

Fig. 2 – Schematic diagram of the proposed amplifier

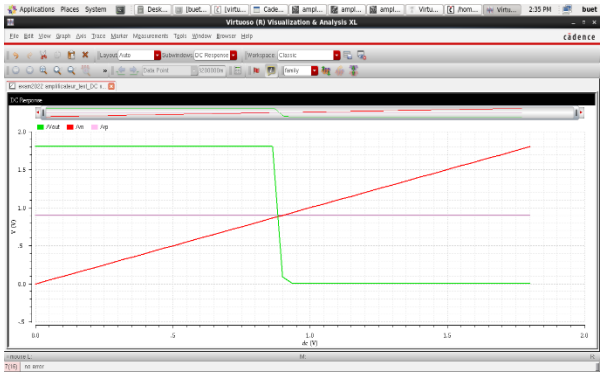

Fig. 3 – DC analysis results

To obtain a low voltage, the characteristics of the sub-threshold MOSFETs are used to implement a low-power, low-voltage circuit and the starting circuit, which causes the voltage reference to start working, consumes almost no energy when the reference circuit is started. In this design, the reference voltage is 500 mV at 27 °C with 21. 6 ppm /°C.

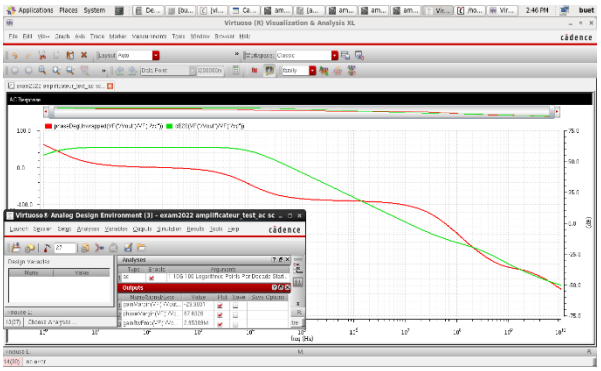

Fig. 4 – AC analysis of the proposed PA

3.3 Layout of the Power Amplifier

The sizes of the power transistors are a critical aspect of the design, as they directly impact the achievable output power of the CMOS power amplifier. In this particular CMOS power amplifier design, the power transistor cells have been meticulously created by combining MOSFETs with a gate finger length of 0.5 µm. Each individual transistor's gate width is set to 70 µm. These dimensions are chosen to optimize the output power. The layout design can have a significant impact on the performance of the power amplifier, particularly when operating at high frequencies. To ensure that the actual performance aligns with the simulated results, it is crucial to meticulously account for the influence of parasitic components, thermal management, and signal coupling during the layout design phase. The layout of the proposed PA on Cadence is shown in Figure 5.

3.4 Design Rule Checker (DRC)

A Design Rule Checker (DRC) in Cadence refers to a tool or feature within Cadence's suite of electronic design automation (EDA) software that is used to check and verify whether a digital or analog integrated circuit layout adheres to the specified design rules. Design rules are constraints and guidelines that ensure the manufacturability and functionality of the integrated circuit. Figure 6 shows the DRC of the layout of the proposed PA.

4. CONCLUSION

This paper discussed the development of a CMOS single-ended power amplifier (PA) tailored for integration into a UHF (Ultra-High Frequency) RFID (Radio Frequency Identification) reader system-on-chip (SoC). The choice of CMOS technology in this research is motivated by its advantages, including low power consumption, high integration capabilities, and compatibility with digital logic circuits. In this paper, we introduce a power amplifier designed for an RFID system, with a specific focus on the development of a passive RFID reader operating in the UHF band at a frequency of 1000 MHz and implemented in CMOS 180 nm technology. Notably, the amplifier stands out for its exceptional efficiency, rendering it well-suited for RFID applications demanding extended reading ranges and reliable operation even in challenging environments.

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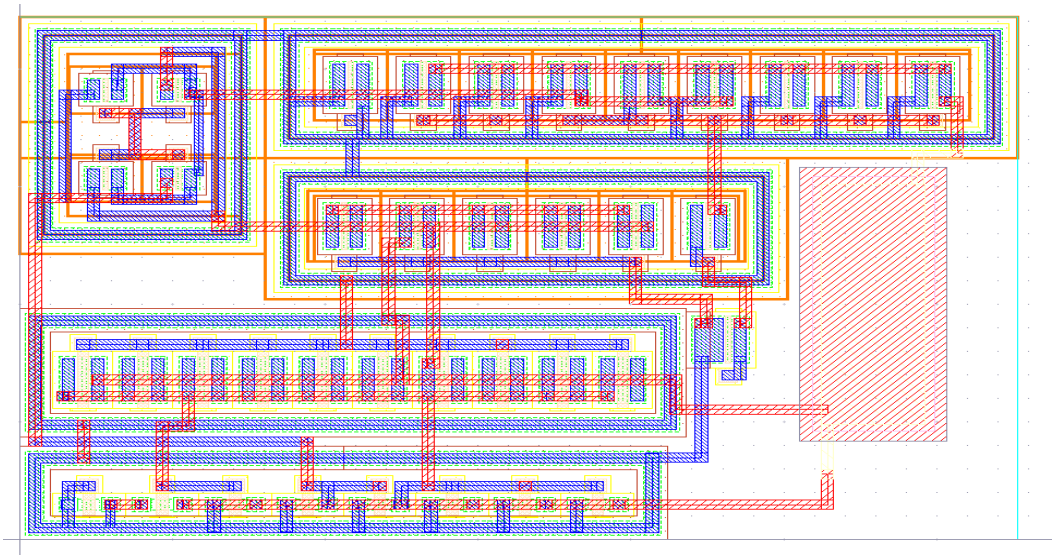

Fig. 5 – Layout of the proposed PA on cadence

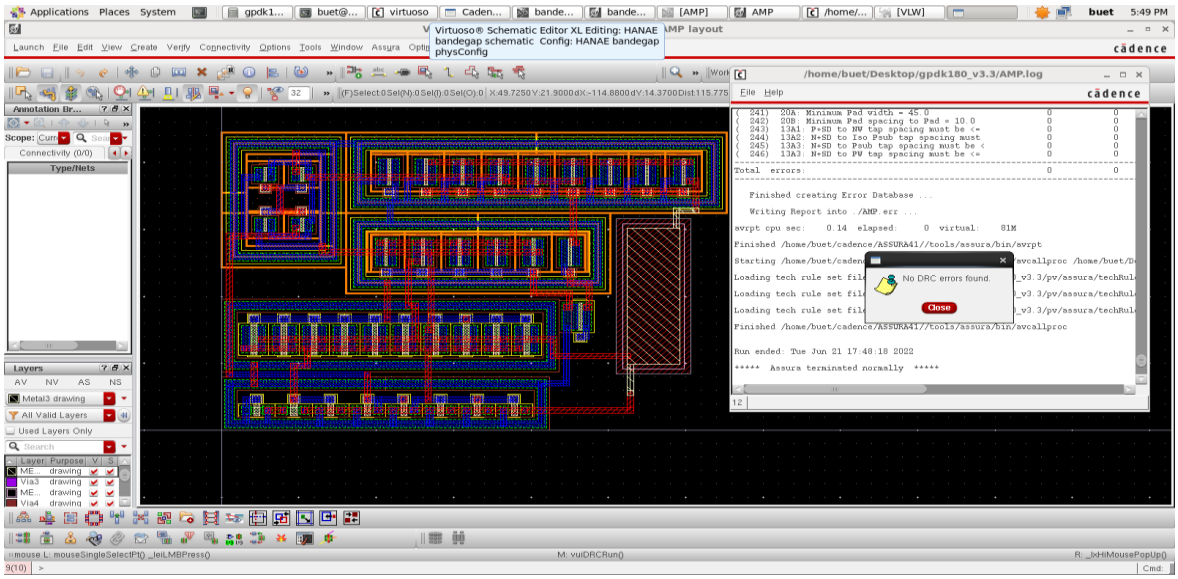

Fig. 6 – Design Rule Checker of the proposed PA

REFERENCES

1. S. Sandoval-Reyes, J.L. Soberanes Perez., *2005 2nd Int. Conf. on Electrical and Electronics Engineering*, 5 (2005).
2. H. Raihani, A. Benbassou, M.E. Ghzaoui, J. Belkadid, *Int. J. Commun. Anten. Propag.* **9** No 3, 172 (2019).
3. G. Li et al., *IEEE Microwave and Wireless Technology Letters* **33** No 9, 1373 (2023).
4. A. El Alami, Y. Ghazaoui, S. Das, S.D. Bennani, M. El Ghzaoui, *Proc. Comput. Sci.* **151**, 1010 (2019).
5. F. Erman, S. Koziel, L. Leifsson, *IEEE Internet Things J.* **10** No 16, 14780 (2023).
6. H. Raihani, A. Benbassou, M. El Ghzaoui, J. Belkadid, *Int. J. Commun. Anten. Propag.* **8** No 2, 95 (2018).
7. S. Haddadian, J.C. Scheytt, G. vom Bögel, T. Grenter, *IEEE J. Radio Frequency Identification* **7**, 556 (2023).
8. Yuxiang Tu, Xiaorong Guo, Chunhua Wang, Jie Jin, Sichun Du, Jingru Sun, *AEU – Int. J. Electron. Commun.* **67** No 7, 574 (2013).
9. Chenyuan Zhao, Jian Liu, Fangyang Shen, Yang Yi, *Comput. Electr. Eng.* **52**, 157 (2016).
10. Ibrahim Abdo, Mutasem Odeh, Fadi R. Shahroury, *Microelectron. J.* **46** No 12, Part B, 1426 (2015).
11. Javad Javidan, S. Mojtaba Atarodi, *AEU – Int. J. Electron. Commun.* **65** No 6, 502 (2011).
12. Héctor Solar, Roc Berenguer, Joaquín de No, Iñaki Gurutzeaga, Unai Alvarado, Jon Legarda, *Integration* **42** No 1, 77 (2009).
13. A. Mazzanti, L. Larcher, R. Brama, F. Svelto, *2005 IEEE Radio Frequency Integrated Circuits (RFIC) Symp., Dig. of Papers* 425 (2005).
14. Y. Eo, K. Lee, *IEEE Microwave Wireless Compon. Lett.* **14** No 11, 504 (2004).
15. Y. Eo, K. Lee, *2004 IEEE RFIC Symp., Dig. of Papers* 575 (2004).

CMOS-підсилювач потужності 1 ГГц 180 нм для систем зчитування UHF RFID

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У цій статті описується однотактний підсилювач потужності CMOS (PA), розроблений для використання в системі зчитування на кристалі (SoC) RFID (радіочастотна ідентифікація) UHF (надвисока частота). Технологія CMOS використовується в цій роботі завдяки її низькому енергоспоживанню, високим можливостям інтеграції та сумісності з цифровими логічними схемами. Крім того, RFID – це галузь, що швидко розвивається, з численними новими технологіями та додатками. RFID – це технологія, яка використовує радіохвилі для ідентифікації та відстеження об'єктів, людей або тварин за допомогою тегів RFID або транспондерів. Ці мітки містять збережену в електронному вигляді інформацію, яку можна зчитувати дистанційно за допомогою зчитувачів або сканерів RFID. Системи RFID покладаються на різні компоненти, включно з підсилювачами потужності, для ефективного зчитування та передачі інформації між RFID-мітками та зчитувачами. Дійсно, підсилювачі потужності відіграють вирішальну роль у цих системах, підвищуючи потужність сигналу, що може значно вплинути на продуктивність системи. У цій статті ми представляємо PA для системи RFID і, зокрема, дизайн пасивного зчитувача RFID в діапазоні UHF на частоті 1000 МГц і за технологією CMOS 180 нм. Пропонований підсилювач виділяється своєю видатною ефективністю, що робить його придатним для додатків RFID, які вимагають великих діапазонів зчитування та роботи в складних умовах.

Ключові слова: Радіочастотна ідентифікація, Підсилювач потужності, Технологія CMOS, Схема компонування на каденції, 180 нм CMOS.