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REGULAR ARTICLE

Optimization of Subthreshold Swing in Vertical Tunnel FET Using Low Work Function Live Metal Strip and Low *k* Material in the Drain

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In this research paper, a Vertical Tunnel FET structure in the presence of a live metal strip & low dielectric constant material is designed and its performance metrics are analyzed in detail. A low dielectric SiO_2 material is incorporated in the channel/drain region. Low work function live metal strip (Molybdenum) is placed in high-*k* dielectric HfO_2 layer in source/channel region. The device is examined by the parameters I_{off}, subthreshold swing, threshold voltage, and I_{on}/I_{off} ratio. The introduction of a live metal strip in the dielectric layer nearer to the source-channel interface results in a minimum subthreshold slope and a good I_{on}/I_{off} ratio. Low dielectric material at drain reduces Cgd-Miller capacitance. Both the SiO_2 layer & low work function live strip show excellent leakage current reduction to 1.4×10^{-17} A/μm. The design provides a subthreshold swing of 5 mV/decade which is an excellent improvement in TFET, ON current of 1.00×10^{-5} A/μm, an I_{on}/I_{off} ratio of 7.14×10^{11} and the threshold voltage of 0.28 V.

Keywords: Dual low work function live strip (DLWLS), Low work function live strip (LWLS), Low-*k* dielectric spacer, Miller capacitance, Molybdenum, Subthreshold swing (SS), Tunnel field-effect transistor (TFET).

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1. INTRODUCTION

Rapid miniaturization of devices has led to an increase in leakage current. Leakage current is a big challenge in miniaturized circuits. Miniaturization at the same time increased the device performance such as speed & reduced the area occupied by the device. The lifetime of the device is reduced due to leakage [1]. Leakage increases as thin SiO_2 is used as gate dielectric material.

The subthreshold swing is 60 mV/dec for thermionic injection of electrons in FET [2]. In practical implementation, SS is greater than it. Thermionic emission affects the off-to-on transition. A small subthreshold swingis needed to turn the device to an off state sharply once VGS drops below the threshold voltage (VTH). Tunnel field-effect transistor (TFET) works on band to band tunneling and not on conventional thermionic emission as the carrier injection mechanism [3]. Band to band tunneling operation enables TFET to have SS < 60 mV/dec [4-7]. The gate-to-drain (C_{gd}) Miller capacitance effecthas an impact on TFET performance. Unwanted TFET effects like overshoot/undershoot in the invertercharacteristics grow when C_{gd} rises [8]. Gate-to-drain capacitance/Miller capacitance increases as a result of the adoption of high-*k* material (HfO_2) in the drain region (C_{gd})) [9]. Ambipolar leakage & Miller capacitance is some of the drawbacks of TFET. Miller capacitance can be reduced because of oxide overlap and low bandgap materials [10].

The solution to reduce gate oxide leakage is high-*k* material. The device's ability to keep a charge is increased by using high-*k* material, which also aids in downsizing. HfO_2 is compatible with a silicon substrate and possesses a high dielectric constant (25), a high adequate band gap (5.68 Ev), band offsets with silicon, a low leakage current, and a lattice parameter that is closer to that of silicon with a modest lattice misfit (5 %) [11].

In this paper, a published VTFET structure is taken for analysis [12]. A large tunnel area & thin channel enhances the device metrics [13]. In addition to the published model, the proposed design uses low-*k* material in the drain region to reduce C_{gd}. Low work function metal strip placed in the source-channel interface causes abruptness in electron concentration, increasing the tunneling rate [14-18]. Molybdenum used as Low work function live strip (LWLS) has a compatible work function with HfO_2 [19, 20] The combination of metal strips & high kmaterial at drain shows minimum Ioff- 1.40×10^{-17}, good I_{on}/I_{off} ratio – 7.14×10^{11}, reduced subthreshold swing – 5 mV/dec lower ambipolarity, and Miller capacitance – C_{gd}.

2. IMPACT OF DIELECTRIC MATERIAL ON GATE-SOURCE & GATE-DRAIN CAPACITANCE

The interelectrode capacitance is caused by the gate-dielectric material, and this work emphasis an increase in source capacitance & a decrease in drain capacitance. By applying potential between the capacitor's electrodes, thecharges there are polarised [9]. Given by is

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the expressionfor the parallel plate capacitor's capacitance.

$$C = q/V = \varepsilon_0 A/d \quad (1)$$

q, ε_0, A, d is the charge on plates, free space permittivity,area of the plate, and distance between plates of capacitor respectively. The electric field is influenced by voltage, charge, and capacitance. The gradient of voltage that characterises the electric field between the plates is indicated by

$$E = dV/dX = V/d \quad (2)$$

dV, dX, V, and d stand for differential voltage, differential length, voltage, and distance between plates. In place of SiO_2,a high k dielectric material (HfO_2) is used to improve capacitance by increasing charge q. The increase in charge stored results in an increased flow of $i(t)$ in the device. At drain/channel region low dielectric (SiO_2) material is inserted in the drain region. This not only reduces the drain region but also reduces the charge held in a parallel plate capacitor (gate-drain). Hence it reduces undesirable C_{gd}.

3. DEVICE STRUCTURE, PARAMETERS, AND SIMULATION MODELS

Figure 1 shows the schematic layout of the proposed dual low work function live strip and spacer vertical TFET (VTFET with DLWLS + Spacer), which uses low work function Molybdenum and low-k SiO_2 in the drain and HfO_2 as a high-k dielectric medium in the source and channelregions. Gate length (LG) is 8 nm, while the gate oxide thickness (t_{ox}) is 2 nm. The component has a dual sourcethat is symmetrical, measuring 50 nm in height and 20 nm oneach side. The drain is 48 nm in length and 5 nm in height.To 3.8 eV, the gate work function is optimised. Highly dopedsource (p^{++}-type), channel (n^{+}-type), and drain (n^{++}-type) are all preserved at 1×20 cm^{-3}, 1×17 cm^{-3}, and 1×19 cm^{-3} of doping concentration, respectively. The Molybdenum live metal strip has a length of 2 nm and a height of 1 nm. The drain region is reduced by adding dielectric SiO_2 to the middle of the drain. Table 1 lists the physical dimensions of the tool used for TCAD simulation.

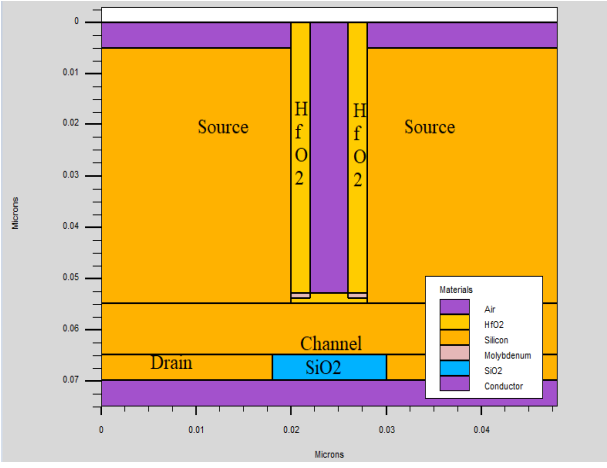

Fig. 1 – Cross-sectional schematics of the proposed VTFETwith DLWLS + Spacer

Table 1 – Device parameters of the VTFET with DLWLS + Spacer

Parameters	Values
Channel doping (N_C)	1×10^{17} cm^{-3}
Drain doping (N_D)	1×10^{19} cm^{-3}
Source doping (N_A)	1×10^{20} cm^{-3}
Gate length	8 nm
Source height	50 nm
Drain height	5 nm
Channel height	10 nm
Source length	20 nm
Drain length	48 nm
Gate oxide HfO_2 thickness	2 nm
Gate work function	3.8 eV
DLWLS-length	2 nm
DLWLS-thickness	1 nm
SiO_2 thickness	5 nm
SiO_2 length	12 nm

The suggested VTFET is compared to VTFET to demonstrate the effects of low work function live strip and low dielectric material [12]. The device parameters used are listed in Table 1. The Silvaco 2-D simulator, technology computer-aided design (TCAD), with bandgapnarrowing model (BGN)- for carrier statistics, recombination model from Shockley Read Hall (SRH), mobility model from Lombardi's model (CVT model), and band-to-band(non-local) modelling implements all simulations.

4. RESULT & DISCUSSION

4.1 Electron Concentration & Electric Field

The electron concentration for each device VTFET with dual low work function live strip and a low-k dielectric SiO_2 spacer in the drain (DLWLS + Spacer), a VTFET with dual low work function live strip (DLWLS), and a VTFET with a low-k dielectric spacer in the drain are shown in Fig. 2. Compared to the other 2 designs,

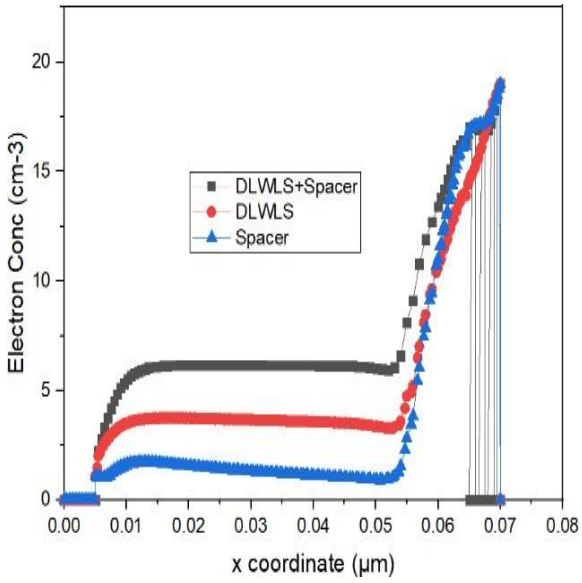

Fig. 2 – Comparison between VTFET with DLWLS + Spacer, DLWLS & Spacer regarding electron concentration

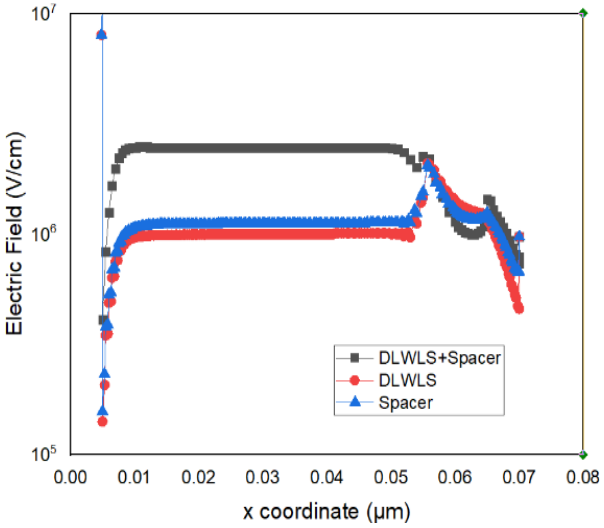

Fig. 3 – Comparison between VTFET with DLWLS + Spacer, DLWLS & Spacer regarding Electric Field

the VTFET with dual low work function live strips and a low k dielectric SiO_2 spacer in the drain has a higher electron concentration. This is because the high-*k* dielectric gate contains a Molybdenum low work function live strip. Due to its low work function, it raises the electron concentration at the source/channel junction. The rise in electron concentration creates abruptness in the source channel. Fig. 3 presents the electric field of VTFET with dual low work function live strip & low*k* dielectric SiO_2 spacer in the drain. It has more electric fields than the other 2 devices due to the increased charge carriers.

4.2 Energy Band

Fig. 4 shows the energy barrier is almost the same for VTFET with DLWLS & VTFET with DLWLS + Spacer The energy band diagram of the VTFET with DLWLS and spacer is shown in Fig. 5 for both the on and off states. When compared to the barrier width between them in the ON state, the distance between the valence band of the source and the conduction band of the channel is greater

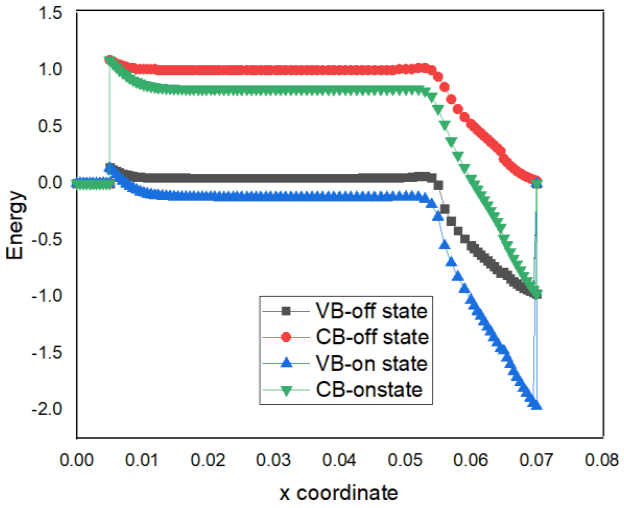

Fig. 4 – Comparison between VTFET with DLWLS + Spacer, DLWLS & Spacer regarding Energy Band Profile

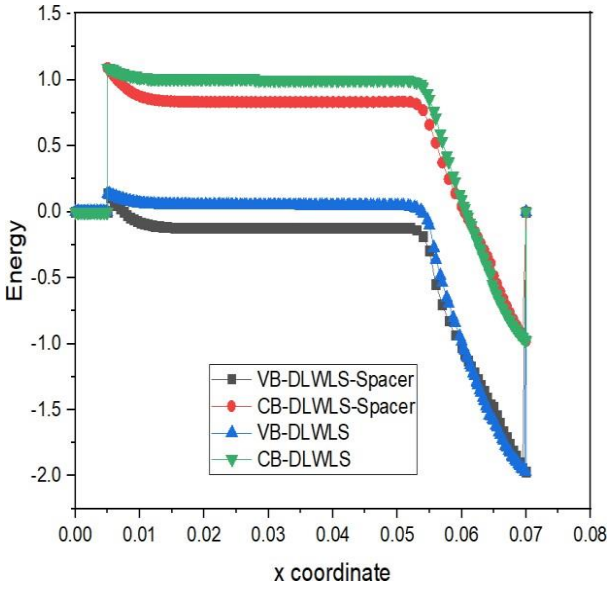

Fig. 5 – Energy band diagrams of proposed Vertical tunnel FET transistorwith DLWLS + Spacer in ON and OFF states

in the off state ($V_{gs} = V_{ds} = 0$). In the ON state, V_{gs} regulates electron motion. V_{gs} is controlling the electron movement in the ON state. Reduction in barrier width enhances electron transfer in the ON state. Leakage current in the off state is reduced by a wide tunnelling barrier.

4.3 Subthreshold Wing

The material present in gate dielectric & geometry of transistor helps in reducing subthreshold swing (SS). The subthreshold swing is 5 mV/dec for VTFET with DLWLS + Spacer, 25 mV/dec for DLWLS & 30 mV/dec for design with spacer alone. Subthreshold swing of a TFET depends on the high-*k* gate dielectric and a thin body to assure that the gate field directly modulates the channel. Maximizing the derivative of the junction electric field on the gate-source voltage [4] is another method for reducing the subthreshold voltage swing. V_{eff} is the tunnel- junction bias, ξ is the electric field, a, b are coefficients based on the junction's material characteristics and the device's cross- sectional area.

$$S = \ln 10 \left[\frac{1}{V_{eff}} \frac{dV_{eff}}{dV_{GS}} + \frac{\xi+b}{\xi^2} \frac{d\xi}{dV_{GS}}\right]^{-1} \quad (3)$$

4.4 Comparison of VTFET with VTFET (DLWLS and Spacer)

The proposed model VTFET with DLWLS and Spacer is compared with simulated published work [12]. The *Id* vs V_{gs} curve of the proposed model is better in terms of leakage current as illustrated in Fig. 6. The off-current of the proposed model is 1.40×10^{-17} A/μm while for the published model is 2.96×10^{-13} A/μm. The threshold voltage is 0.28 V. On state current is 1.00×10^{-5} A/μm.High dielectric constant HfO_2 increases the capacitance at the source/channel junction. This increases C_{gs}. But at sameemploying low dielectric material SiO_2 at drain decreases C_{gd}-Miller capacitance. The transfer characteristics of the 3 devices are presented in Fig. 7. Leakage current is minimum in the proposed model.

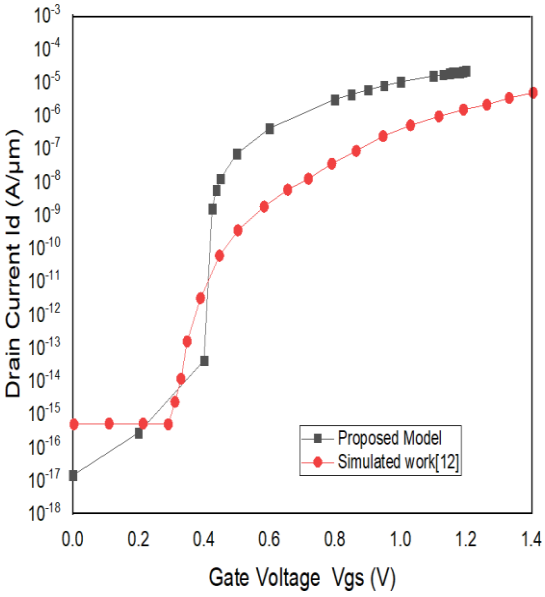

Fig. 6 – *Id*s vs VGS of Vertical-TFET with DLWLS + Spacer & published model [12]

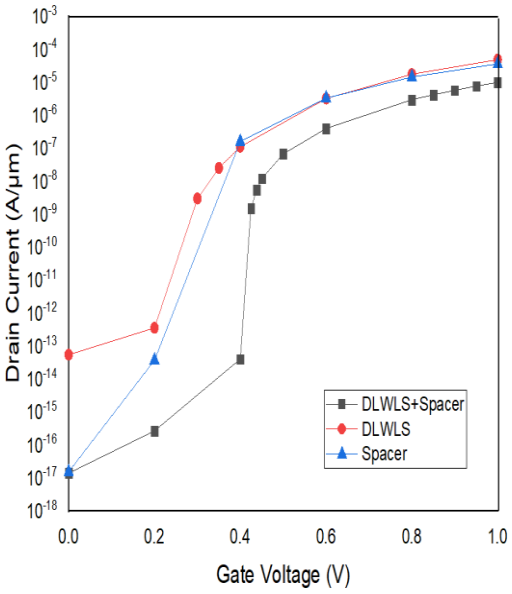

Fig. 7 – Comparison between transfer characteristics of VTFET withDLWLS + Spacer, DLWLS & Spacer

4.5 Miller Capacitance

High dielectric constant HfO_2 increases the capacitance at the source/channel junction. This increases C_{gs}. But at the same time employing low dielectric material SiO_2 at drain decreasesC_{gd}-Miller capacitance a desirable factor for FET [21]. Fig. 8 & Fig. 9 shows the increase & decrease in C_{gs} & C_{gd} respectively for the proposed model.

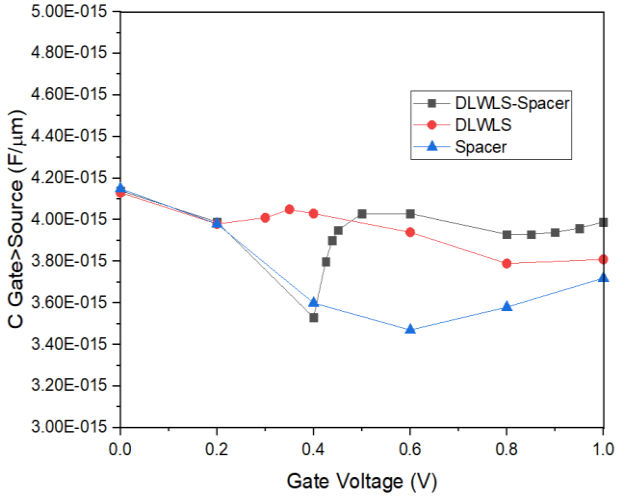

Fig. 8 – Capacitance (C_{gs})–voltage characteristics of the three models

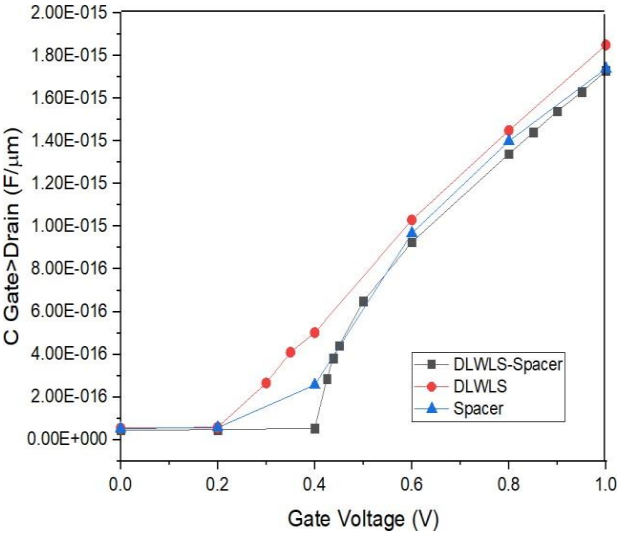

Fig. 9 – Capacitance (C_{gd})–voltage characteristics

5. CONCLUSION

In this proposed work, high-*k* gate oxide with molybdenum metal is designed along with low-*k* material in the drain. As FETs are playing a vital role in the IC industry the lower sub-threshold swing and reduced Miller capacitance with low OFF-state currentis required for power-efficient low leakage memory systems. So, a VTFET with a low work function live strip & spacer is designed for maximum performance by limiting the leakage current. The performance of the proposed VTFET with DLWLS + spacer is presented and compared with standalone DLWLS & spacer structures. The Miller capacitance, subthreshold swing & leakage of the proposed device is improved compared to other architectures because of low work function metal design & low k material in drain design. The suggested model is implemented with the help of the Atlas Silvaco tool.

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Оптимізація підпорогового коливання у вертикальному тунельному польовому транзисторі з використанням металевої стрічки з низьким рівнем робочої функції та матеріалу з низьким рівнем *k* у дренажі

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У цій роботі описано вертикальну тунельну структуру польового транзистора за наявності металевої смуги під напругою та матеріалу з низькою діелектричною проникністю та детально проаналізовано її показники продуктивності. Матеріал з низьким діелектричним вмістом SiO_2 включено в область каналу/стоку. Металева стрічка з низькою роботою виходу під напругою (молібден) поміщається в діелектричний шар HfO_2 з високим коефіцієнтом виходу в області джерела/каналу. Пристрій перевіряється за параметрами I_{off}, підпорогове коливання, порогова напруга та співвідношення $I_{on}/Ioff$. Введення металевої стрічки під напругою в шар діелектрика ближче до межі джерело-канал призводить до мінімального підпорогового нахилу та гарних показників співвідношення I_{on}/I_{off}. Низький діелектричний матеріал у стоці зменшує ємність Cgd-Miller. Як шар SiO_2, так і стрічка з низькою продуктивністю роботи демонструють чудове зниження струму витоку до $1{,}4 \times 10^{-17}$ А/мкм. Конструкція забезпечує підпорогове коливання 5 мВ/декаду, що є чудовим покращенням TFET, струм увімкнення $1{,}00 \times 10^{-5}$ А/мкм, співвідношення I_{on}/I_{off} становить $7{,}14 \times 10^{11}$ і порогова напруга 0,28 В.

Ключові слова: Подвійна динамічна смуга з низькою функцією виходу (DLWLS), Динамічна смуга з низькою функцією виходу (LWLS), Діелектричний шар з низьким *k*, Ємність Міллера, Молібден, Підпорогове коливання (SS), Тунельний польовий транзистор (TFET).