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REGULAR ARTICLE

Performance Enhancement of the Urdhva-Tiryagbhyam based Vedic Multiplier using Fin-FET

P. Vimala* ✉, Soumya G. Hosmani†

Dayananda Sagar College of Engineering, Bangalore, Karnataka, India

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The demand for quick and effective real-time DSP ("Digital Signal Processing") applications has increased as a result of rapidly developing technologies. One of the fundamental mathematical processes that any application needs is multiplication. There are many uses for the Vedic Multiplier in the broad fields of image processing and DSP, notably the several variations of the original Vedic Multiplier topologies that improve speed and performance. The aim of a paper is to design the Vedic multiplier in MOSFET and FinFET technology and reduce the power and time of the design. For reducing the delay and power three different technology of adder is designed which are "GDI", "Dual domino rail adder" and "Traditional adder". The GDI technology has a better performance like lower power, delay and number of transistors so that using the GDI technology is used as the logic to design as full adder half adder and AND gate. To design the 2-bit multiplier it required four AND gate and two half adders to obtain the partial product. Later by using the 2-bit multiplier and 4-bit Ripple Carry Adder the 4-bit multiplier is mapped. Later using the 4-bit multiplier design the 8-bit multiplier is mapped. The proposed design is designed in MOSFET and FinFET technology as the result FinFET technology consume lower power and delay because of its lower leakage, higher drain current and higher performance. By using the FinFET technology overall performance will be 433.05 mW power and 0.981ns delay and MOSFET consumes 657.65 mW and 1.367 ns.

Keywords: Fin Field Effect Transistor (FinFET), Metal Oxide Semiconductor Field Effect Transistor (MOSFET), Gate Diffusion input (GDI) technology.

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1. INTRODUCTION

Moore developed his law based on empirical observations. It was predicted that the number of transistors on a microchip grows two times every year based on observable statistics. The complexity of semiconductor process technologies has always risen. The growth of complexity has accelerated recently. Nowadays, transistors behave in ways that are neutralize for three-dimensional objects. To accurately duplicate the extremely small feature sizes of modern manufacturing techniques on a silicon wafer, numerous patterning was necessary. The design process has become considerably more difficult as a result. Device scaling, which leads to denser and quicker device integration, is a crucial component of "Very Large Scale Integration" (VLSI) design to advance the industry's success. Leakage current and circuit reliability become the main challenges as technology node goes into the extremely deep submicron level. Both are getting worse with each new technology generation and have an impact on how well the logic circuit functions as a whole. With the scaling of a transistors, the power dissipation and circuit performance must remain balanced by the VLSI developers. Different devices are proposed for reducing leakage current and power dissipation [1-4]. FinFET technology is one of most important technology for VLSI design [5-8].

In several applications, particularly digital filtering and digital transmission, the multiplication is an essential primary role in arithmetic logic process. Every customer wants a quicker gadget with less power usage. Performance is improved by the device's high-speed elements and lower power consumption. The desire for portable electronics configurations, which utilize various forms of "Digital Signal Processing" (DSP), is rapidly rising nowadays. As a response, manufacturing such functionalities necessitates thoughtful consideration of the small and quick multiplier [9-11].

In this work, we proposed an optimized Vedic multiplier using FinFETs. FinFET technology helped for the multiplier to have impact in the performance by reducing delay time and power dissipation.

2. VEDIC MULTIPLIER

The Vedic technique typically yields immediate solutions to large quantities of money or "tough" challenges [12]. These elegant and stunning techniques are simply a small portion of a much broader and more coherent mathematical system than the current system. The approaches used in Vedic Mathematics provide a mathematical framework that is complimentary, straightforward, and unified. In vedic technique there are 16 sutras and 13 sub-sutras they are namely "Ekadhikina Purvena", "Nikhilam Navatashcaramam

* Correspondence e-mail: ervimala@gmail.com
† soumyahosmani98@gmail.com

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dashatah","urdhva-tiryagbyham" etc, Out of this sutras in my project we will be using the "Urdhva-Triyagyham" sutra which is also referred as "Vertically and crosswise" which is mainly used in multiplication

2.1 4-bit vedic multiplier

With the use of 2-bit Vedic multipliers and adders, a 4-bit Vedic multiplier may be created. This partial product term is formed using a 2-bit Vedic multiplier, proceeded by such a partial reduction and terms of adding step using a simple adder circuit. It is feasible to utilize a straightforward 4-bit RCA circuit. Consider that M and N are the two four-bit values, respectively: M = "m_3 m_2 m_1 m_0" and N = "n_3 n_2 n_1 n_0". "f_7 f_6 f_5 f_4 f_3 f_2 f_1 f_0" is the resultant of the multiplication. Say "m_3 m_2" & "m_1 m_0" for M and "n_3 n_2" & "n_1 n_0" for N when dividing M and N into two parts. Now it is assumed that the number of bits to be multiplied by the 2×2 vedic multiplier is two bits added together and regarded as a single bit. Four bits will be the outcome of the multiplication. The input for the first 2-bit multiplier are "m_1 m_0" & "n_1 n_0" (Vertically), the final block is a 2-bit multiplier using the "m_3 m_2" & "n_3 n_2" (Vertically) and the two 2-bit multipliers with inputs "m_3 m_2" & "n_1 n_0" and "m_1 m_0" & "n_3 n_2" are in the center (Crosswise). In the end, there are 8-bits total: "f_7 f_6 f_5 f_4 f_3 f_2 f_1 f_0" and "c_0," which serves as the carry bit.
The operation is flow as following,

$$f_0 = m_0 n_0 \quad (1)$$

$$c_1 f_1 = m_1 n_0 + m_0 n_1 \quad (2)$$

$$c_2 f_2 = c_1 + m_2 n_0 + m_1 n_1 + m_0 n_2 \quad (3)$$

$$c_3 f_3 = c_2 + m_3 n_0 + m_2 n_1 + m_1 n_2 + m_0 n_3 \quad (4)$$

$$c_4 f_4 = c_3 + m_3 n_1 + m_2 n_2 + m_1 n_3 \quad (5)$$

$$c_5 f_5 = c_4 + m_3 n_2 + m_2 n_3 \quad (6)$$

$$f_7 f_6 = c_5 + m_3 n_3 \quad (7)$$

The 4-bit vedic multiplier is as shown in Fig. 1

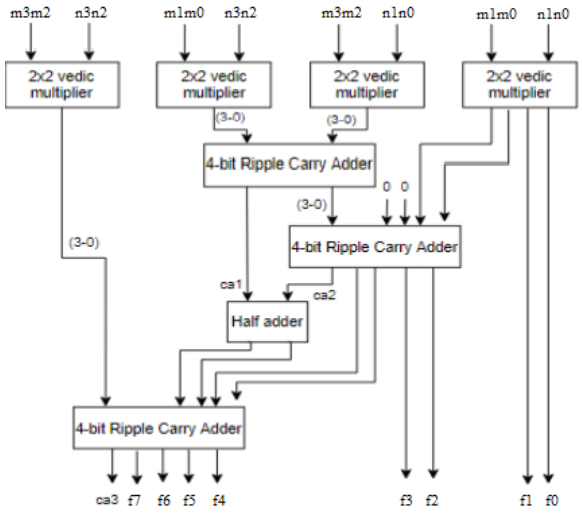


Fig. 1 – Schematic Drawing of 4-bit vedic multiplier

2.2 8-bit vedic multiplier

With the use of 4-bit vedic multiplier and RCA adder, a 8-bit vedic multiplier is may be created. The partial product formed by 4-bit vedic multiplier is given to adder circuit. Consider M and N are two 8-bit value, "M = m_7 m_6 m_5 m_4 m_3 m_2 m_1 m_0" and "N = n_7 n_6 n_5 n_4 n_3 n_2 n_1 n_0". The M is divided into two part as MH ("m_7 m_6 m_5 m_4") and ML ("m_3 m_2 m_1 m_0"), similarly N is NH ("n_7 n_6 n_5 n_4") and NL ("n_3 n_2 n_1 n_0"). The operation can be formed to obtain the partial product is

$$F = MxN$$

$$= (MH - ML)x(NH - NL)$$

$$= MHxNH + (MHxNL + (MLxNH) + MLxNL\,.$$

The block diagram 8-bit vedic multiplier is shown in Fig. 2.

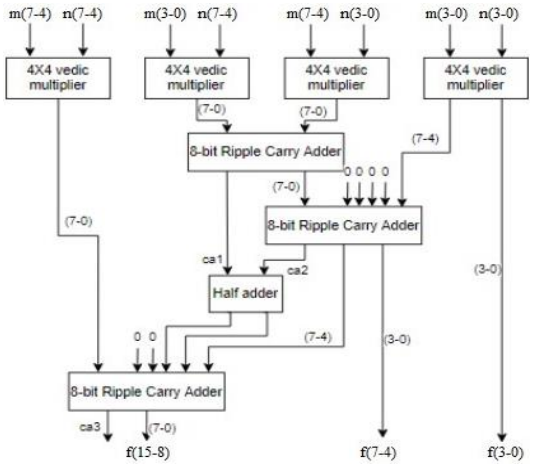


Fig. 2 – Block diagram of 8-bit vedic multiplier

3. SIMULATION AND RESULT

3.1 4-bit vedic multiplier

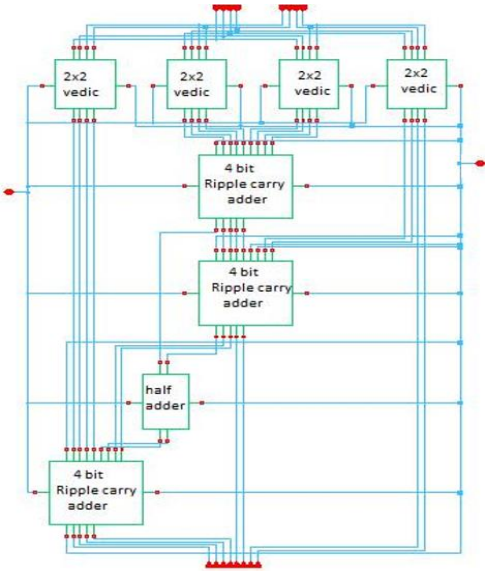


Fig. 3 – Diagrammatic representation of 4-bit vedic multiplier

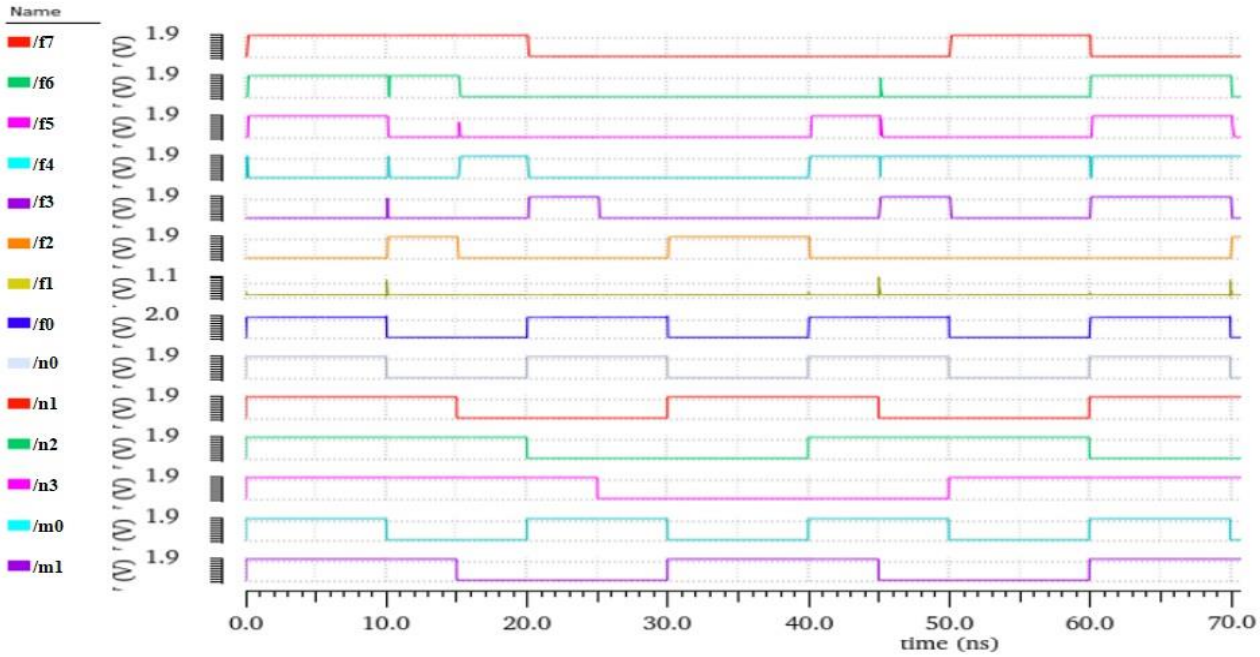


Fig. 4 – Waveform of 4-bit vedic multiplier

The Diagrammatic representation and output waveform of 4-bit multiplier's is as shown in Fig. 3 and Fig. 4 respectively. For inputs of "m_3 m_2 m_1 m_0" and "n_3 n_2 n_1 n_0". Various test cases are generated for the inputs by pulse waveforms, each of which has a different pulse width and time. The outputs are represented by "f_7 f_6 f_5 f_4 f_3 f_2 f_1 f_0", where "f_7" is the "MSB" and "f_0" is the "LSB".

Table 1 – Power and Delay of vedic multiplier of 45 nm for MOSFET and FinFET for 4-bit multiplier

Product terms	MOSFET		FinFET	
	Power (mW)	Delay (ps)	Power (mW)	Delay (ps)
f_7	900.3	14.42	225.4	155.5
f_6	0.3896	10030	238.2	114.8
f_5	450.8	35.53	549.9	92.79
f_4	490	10060	178.7	88.52
f_3	720.5	25.49	471.7	145.4
f_2	709.6	129.5	522.5	10190
f_1	582.3	87.91	0.2958	80.20
f_0	359.5	62.88	501.8	75.34

Table 2 – Power and Delay of vedic multiplier of 45 nm and 22 nm for FinFET for 4-bit multiplier

Product terms	45 nm		22 nm	
	Power (mW)	Delay (ps)	Power (mW)	Delay (ps)
f_7	225.4	155.5	46	236.1
f_6	238.2	114.8	269	160.2
f_5	549.9	92.79	504.1	115.8
f_4	178.7	88.52	114.3	111.4
f_3	471.7	145.4	535.6	234.8
f_2	522.5	10190	644.8	10230
f_1	0.2958	80.20	0.433	100.3
f_0	501.8	75.34	600	94.74

The power and delay are calculated for 45 nm with respected to FinFET and MOSFET is tabulated in Table 1 for 4-bit. As an overall result MOSFET consume 526.69 mW and 2555.718 ps whereas FinFET consume 336.06 mW and 1367.818 ps from the table the optimized results are obtained for FinFET technology compare to available technology (MOSFET). To have better results the analysis are carried out for 22 nm FinFET technology. The comparisons between 45 nm and 22 nm FinFET technology is listed in Table 2.

3.2 8-bit vedic multiplier

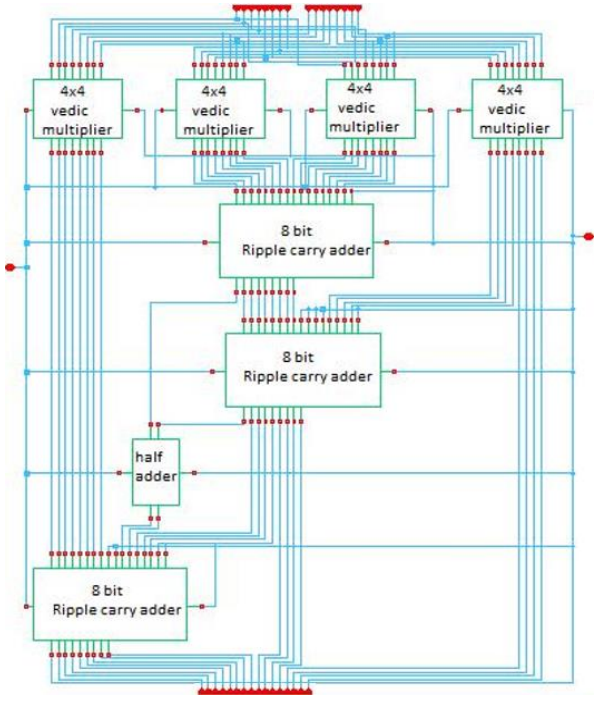
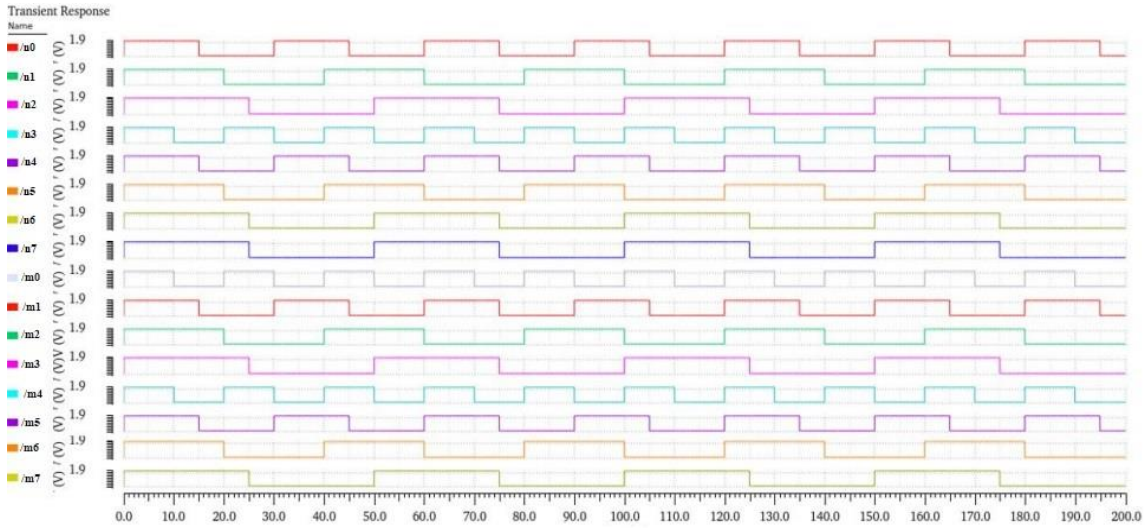
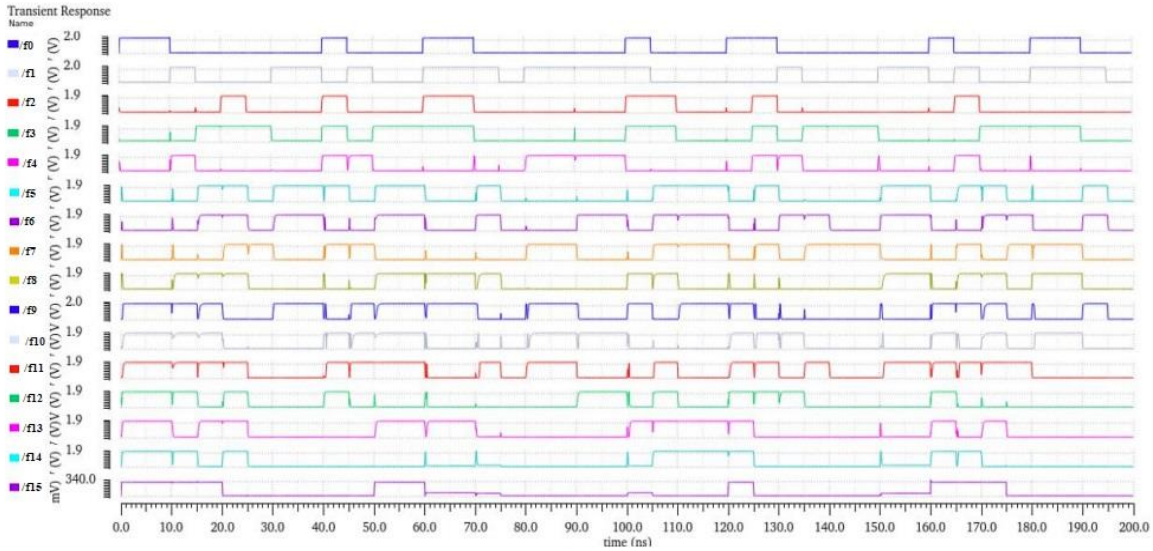


Fig. 5 – Diagrammatic representation of 8-bit vedic multiplier



a



b

Fig. 6 – Waveform of 8-bit vedic multiplier inputs are in (a) and product terms are in (b)

Table 3 – Power and Delay of vedic multiplier of 45 nm for MOSFET and FinFET for 8-bit multiplier

Product terms	MOSFET		FinFET	
	Power (mW)	Delay (ps)	Power (mW)	Delay (ps)
f_{15}	79.54	83.48	466.4	184.1
f_{14}	468.9	94.76	616.8	273.4
f_{13}	662.9	140.2	543.3	501.5
f_{12}	542.5	32.98	567.5	106.8
f_{11}	953.7	337.9	613.9	171.8
f_{10}	829.6	47.86	378.4	1017
f_9	938.5	337.4	726.4	92.76
f_8	708.7	18.14	286.3	88.52
f_7	759.4	90.41	347.2	203.3
f_6	853.7	148.4	222.9	423.3
f_5	757	43.66	236.5	150.6
f_4	449.4	51.14	551.4	191.4
f_3	809.2	10070	197.9	145.3
f_2	359.2	33.02	1.438	12010
f_1	855.2	10020	374.2	80.20
f_0	495.1	11.92	798.3	75.34

Table 4 – Power and Delay of vedic multiplier of 45 nm and 22 nm for FinFET for 8-bit multiplier

Product terms	45 nm		22 nm	
	Power (mW)	Delay (ps)	Power (mW)	Delay (ps)
f_{15}	466.4	184.1	112.5	10550
f_{14}	616.8	273.4	301.8	120.5
f_{13}	543.3	501.5	393.9	197.8
f_{12}	567.5	106.8	589.6	56.38
f_{11}	613.9	171.8	463.1	88.04
f_{10}	378.4	1017	564.4	375.4
f_9	726.4	92.76	591.3	59.65
f_8	286.3	88.52	215.7	57.59
f_7	347.2	203.3	391.1	101.1
f_6	222.9	423.3	202.1	168.3
f_5	236.5	150.6	203.9	80.55
f_4	551.4	191.4	582.6	89.54
f_3	197.9	145.3	198.1	79.21
f_2	1.438	12010	201.3	15150
f_1	374.2	80.20	0.827	53.55
f_0	798.3	75.34	600	51.66

The diagrammatic representation and waveform of 8-bit multiplier are shown in Fig. 5 and Fig. 6 respectively. For input of "m_7 m_6 m_5 m_4 m_3 m_2 m_1 m_0" and "n_7 n_6 n_5 n_4 n_3 n_2 n_1 n_0" for various test cases. The output is "f_{15} f_{14} f_{13} f_{12} f_{11} f_{10} f_9 f_8 f_7 f_6 f_5 f_4 f_3 f_2 f_1 f_0". The power and delay are calculated for 45 nm with respected to FinFET and MOSFET is tabulated in Table 3. for 8-bit. As an overall result MOSFET consume 657.65 mW and 1358.86 ps whereas FinFET consume less power and delay time as 433.05 mW and 981.58 ps. To have better results the analysis are carried out for 22 nm FinFET technology. The comparisons between 45 nm and 22 nm FinFET technology is listed in Table 4.

4. CONCLUSION

In the VLSI an effective Vedic multiplier is built utilizing an antiquated Vedic algorithm. The vedic multiplier is low power, high-speed multiplier compare to another multiplier. The design is implemented in MOSFET and FinFET as a result FinFET has the better performance as a power and delay. 8-bit vedic multiplier in MOSFET consumes 657.65 mW and 1.367 ns whereas FinFET have 433.05 mW power and 0.981 ns delay which is less than the MOSFET technology.

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Підвищення продуктивності ведичного множника за допомогою FinFET

P. Vimala, Soumya G. Hosmani

Dayananda Sagar College of Engineering, Bangalore, Karnataka, India

Попит на швидкі й ефективні програми DSP («цифрової обробки сигналів») у реальному часі зріс у результаті швидкого розвитку технологій. Одним із фундаментальних математичних процесів, необхідних будь-якій програмі, є множення. Vedic Multiplier можна використовувати у багатьох сферах обробки зображень і DSP, зокрема кілька варіантів оригінальних топологій Vedic Multiplier, які покращують швидкість і продуктивність. Метою статті є розробка ведичного помножувача в технології MOSFET і FinFET і зменшення потужності та часу розробки. Для зменшення затримки та потужності розроблено три різні технології суматора: «GDI», «Dual Domino Rail Adder» і «Traditional adder». Технологія GDI має кращу продуктивність, наприклад меншу потужність, затримку та кількість транзисторів, тому використання технології GDI використовується як логіка для проектування як повного суматора, напівсуматора та вентиля I. Для проектування 2-розрядного множника та отримання часткового добутку знадобилося чотири вентилі I та два напівсуматори. Пізніше за допомогою 2-розрядного множника та 4-бітового суматора переносу пульсацій відображається 4-бітовий помножувач, а за допомогою конструкції 4-бітного множника відображається 8-бітний множник. Запропонована конструкція розроблена за технологією MOSFET і FinFET, оскільки технологія FinFET споживає меншу потужність і затримку через менший витік, вищі струм стоку та продуктивність. Завдяки використанню технології FinFET загальна продуктивність становитиме 433,05 мВт, час затримки - 0,981 нс, відповідно для MOSFET 657,65 мВт і 1,367 нс.

Ключові слова: Fin польовий транзистор (FinFET), Метал-окисел-напівпровідник польовий транзистор (MOSFET), Технологія GDI.