Journal of Nano- and Electronic Physics
Vol. **16** No 1, 01010(5pp) (2024)

Журнал нано- та електронної фізики
Том **16** № 1, 01010(5сс) (2024)

REGULAR ARTICLE

Investigation of the Influence of Technological Factors on High-Voltage p^0–n^0 Junctions Based on GaAs

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(Received 05 January 2024; revised manuscript received 14 February 2024; published online 28 February 2024)

A technology has been developed and an optimal solution has been found for obtaining p^0-n^0 junctions based on lightly doped GaAs layers, with high values of electrical parameters and specified thicknesses of the base layers for creating ultra-high-speed high-voltage pulsed three-electrode switches with a photon-injection mechanism for the transfer of no ne quorum charge carriers. The dependence of the switching stability relative to the control pulse of the created high-voltage photonic-injection switches in a wide current and frequency mode of their operation, its sensitivity to various external and internal influences of these parameters has been studied. Those on the thickness of the p^0-layer, on the transfer coefficient α, on the breakdown voltage Utrial, high-voltage p^0-n^0 transition, on the thickness of the solution-melt, on the temperature of the onset of crystallization, as well as the dependence of the transfer coefficient on the thickness of the p^0-layer.

Keywords: Liquid-phase epitaxial (LPE), Heterostructures, High-voltage p^0-n^0 transition, Hall effect, Background doping, Solution-melt.

DOI: 10.21272/jnep.16(1).01010 PACS numbers: 073.63.Hs, 73.21.Fg, 73.21. – b

1. INTRODUCTION

As is known, to create subnano - and picosecond photon-injection switches based on GaAs and AlGaAs heterostructures, the main need is:

1. Determination of the optimal temperature-time regime for the reproducible production of an n^+-p^0-n^0 transistor structure with a high-voltage p^0-n^0 junction, in liquid-phase epitasis (LPE), formed due to background doping with specified parameters and the creation of sub nanosecond powerful switches based on them.
2. Study of the influence of the main technological factors: the temperature of the onset of crystallization tn.cr., the thickness of the solution-melt h, the hydrogen flow rate F, the static turn-on voltages U_{on}, the control current I_{up}, and the dynamic parameters – current rise time, turn-on delay time relative to the control impulse, the stability of switching on switching structures [1-15].

Conducting research on the creation of high-power high-voltage switching device structures based on lightly doped gallium arsenide is associated with the need to search for alternative principles for switching electrical power in the sub nanosecond and picoseconds time ranges. Since modern laser, accelerator and location technology, thermonuclear energy, picosecond spectroscopy of liquids and solids, topography, radio engineering, digital technology and a number of areas of converter technology require the creation of semiconductor switches of this power range, which have the traditional advantages of semiconductor devices: long service life, reliability, high efficiency and, which is extremely important for a number of applications, resistance to external influences (radiation, temperature) and instant readiness for operation.

Due to the need for location technology, defense, digital technology, two new switching principles have been developed - using a control plasma layer and using a delayed shock-ionization wave, which made it possible to increase the power switched by devices in the nanosecond range by almost two to three orders of magnitude and in the picosecond range by almost four orders of magnitude [16, 17].

The speed, the magnitude of the absolute and specific power switched by semiconductor devices largely depends on the processes of filling the region with electron-hole plasma, which has a high resistance in the initial state and blocks the applied external voltage. Such a region is the region of the space charge, depleted by the strong field of the reverse-shifted p-n junction.

Powerful semiconductor devices developed on the basis of silicon, such as pulse sharpeners of diode, transistor and thyristors types, operating on the principle of switching using a delayed shock-ionization wave, required the development of new circuitry, a new direction of research using new materials, primarily GaAs and hetero structures on its basis [18, 19].

Currently, epitaxial methods for obtaining single-crystal layers are widely used for the manufacture of various semiconductor devices. Epitaxial growth methods make it possible to combine in time the process of

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Cite this article as: A.M. Sultanov et al., *J. Nano- Electron. Phys.* 16 No 1, 01006 (2024) https://doi.org/10.21272/jnep.16(1).01010

crystallization of a semiconductor material and the production of a device structure. Gas-transport, molecular-beam and liquid-phase epitaxial have received the main distribution.

When developing high-voltage diodes, transistors and thyristors, it is necessary to use GaAs with a concentration of the main charge carriers of 10^{15}cm^{-3} or less. A fairly common technology for obtaining such a material is LPE, carried out in a quartz container with forced cooling of a solution-melt of GaAs in Ga [20, 21]. This method, in comparison with other methods for growing epitaxial layers, makes it possible to obtain efficiently injecting junctions. This is due to the fact that, when GaAs is grown by this method, the internal quantum yield of radioactive recombination is much higher than when GaAs is grown from stoichiometric melts [22, 23]. This opens up the possibility of an unconventional approach to the design of high-voltage devices based on hetero structures. In addition, this method has the following advantages over gas-transport and molecular epitaxial: simplicity of equipment, higher growth rates, the possibility of reducing the impurity background, etc. The physicochemical foundations of LPE are well described in a number of monographs [24] and books [25].

2. METHOD

LPE is an oriented crystallization of single-crystal layers of semiconductor materials from solutions of these materials. There are several methods of epitaxial growth from a solution-melt: growth from a limited volume and growth from a semi-limited volume of a solution-melt. The method of growing epitaxial layers from a limited volume of a solution-melt has received the main distribution.

Under conditions of crystallization from limited volumes of solutions-melts, both a significantly higher reproducibility of obtaining layers with a given thickness is achieved compared to crystallization from semi-limited volumes, as well as a higher degree of their planarity. In addition, the growth of layers from a limited volume of a solution-melt makes it possible to control the crystallization rates and conduct the process under conditions closer to quasi-equilibrium.

Thanks to the development of technology for obtaining high-voltage *p-n* junctions based on lightly doped GaAs, it became possible to create pulsed transistors and thyristors based on GaAs-AlGaAs hetero structures. Studies have shown the prospect of using photon-injection mechanisms of coupling between *p-n* junctions in high-voltage multilayer structures, the possibility of switching high powers by three-electrode semiconductor devices in the sub nanosecond range of durations [18].

Therefore, the improvement of the main parameters and characteristics (increasing the operating voltage, improving the speed, reproducibility and dependence of the temperature effect, radiation) of switches is associated with an understanding of the technological processes for the formation of high-voltage *p-n* structures, the choice of the optimal geometry and the search for new designs [19, 21].

The analysis of the literature data shows [1, 22-28] that the production of lightly doped GaAs layers and the formation of high-voltage *p-n* junctions in the process of growth have not been clarified, the nature of residual impurities is not entirely clear, the influence of technological factors on the electrical properties has not been studied, which makes it difficult to create high-voltage switches with subnano and picoseconds speed.

The static and impulse characteristics of such device structures obtained under various technological conditions have not been studied at all.

The aim of our work is to obtain high-voltage p-n junctions based on lightly doped GaAs layers, to study the influence of technological factors on their main dynamic parameters and characteristics, to create powerful photon-injection pulse switches based on them with subnano and picoseconds speed, to elucidate the possibility of increasing the power of the switched gallium arsenide transistors and thyristors in the sub nanosecond range.

3. METHODOLOGY

The proposed technologies for obtaining high-voltage *p-n* junctions based on lightly doped GaAs allowed the creation of pulsed transistors and thyristors based on GaAs-AlGaAs hetero structures. We have optimized technologies for obtaining high-voltage *p-n* junctions based on lightly doped GaAs layers and creating subnano and picoseconds speed photon-injection switches based on the principle of photon transfer of non equilibrium charge carriers. The main attention is paid to the features of obtaining device structures, the influence of technological factors on the static and dynamic parameters of switching structures in the mode of high currents and voltages.

Liquid-phase epitaxial is the method of growing epitaxial layers from a limited volume of a solution melt to obtain and fabricate device structures. Under conditions of crystallization from limited volumes of solutions-melts, both a significantly higher reproducibility of obtaining layers with a given thickness is achieved compared to crystallization from semi-limited volumes, as well as a higher degree of their planarity. In addition, this method makes it possible to control the crystallization rates, conduct the process under conditions closer to quasi-equilibrium, and obtain "pure" and doped layers of high-quality *p-n* junctions and multilayer device structures with specified electro physical parameters with sufficiently high reproducibility.

The main problem in creating subnano and picoseconds switches based on GaAs is to obtain layers with a given thickness of the base regions and a low dopant concentration. A study was made of the influence of technological factors on the properties of epitaxial layers and p^0-n^0 junctions.

To ensure the optimal impurity distribution profile in a quartz container, from a limited volume of an arsenic melt solution in gallium on n^+-GaAs substrates oriented in the (100) plane, p^0- and n^0-GaAs layers with specified thicknesses were grown, which are the basic regions of the structure.

The position of the *p-n* transition, the concentration profile in the p^0- and n^0-layers, the thickness of the p^0-region in depending on the conditions for the formation of an impurity background in the solution-melt were obtained in advance planned limits.

The lifetime of minority charge carriers (NCC) is an important dynamic characteristic of a semiconductor device. In lightly doped GaAs, the CC lifetime is determined mainly by the concentration of deep levels. Its value in lightly doped regions of transistor and thyristors structures was determined by measuring the dissipation time of the charge accumulated in these regions and was 50-500 ns. Such a scatter in the values of the CC lifetime is due to the concentration and capture cross section of uncontrollably introduced recombination centers.

The concentration of carriers in the p^0- and n^0- regions ranged from 1.0×10^{15} cm^{-3} to 0.1×10^{15} cm^{-3}, the mobility of charge carriers was, $\mu_n = (5\text{-}6) \times 10^3$ cm^2/V/Vs in the n^0-layer and $\mu_p = (400\text{-}450)$ cm^2/V/Vs at 300 K. The charge carrier motilities were determined by measuring the Halle effect in the grown epitaxial layers.

The thickness of the n^0-layer, exceeding the dimensions of the space-charge layer at zero mixing of the p-n junction, was (30-35) μm and provided the possibility of effective separation of electron-hole pairs created by absorbed radiation. The control of the position of the p-n transition, the estimation of the size of the space charge region was carried out by a method based on the observation of the electro-optical effect in gallium arsenide during the passage of plane polarized infrared light through the crystal.

For the efficient operation of thyristors and transistors, the thickness of the p^0-part should be as small as possible, therefore, for them manufacturing can only be used n^+-p^0-n^0 structures with certain thicknesses p^0- areas that provide high transfer coefficient values. Defined the temperature dependence of p^0-layer on temperature the beginning of crystallization (Fig. 1), and coefficients segregation of fine acceptor and donor impurities the level of concentration and the degree of compensation. In order to optimize the growth technology and the design of thyristors, the dependences of the transfer coefficients of structures on the thickness of the low-resistance part of the p^0-region and on temperature were studied (Fig. 2).

It can be seen that the transfer coefficient α of transistor n^+-p^0-n^0 structures drops sharply already at a thickness $p^0 = 30$ μm regardless of the temperature onset crystallization. At the same time, the thickness of the high-resistance parts hi - areas up to hi-120 μm are not has a significant impact on the value transmission coefficients.

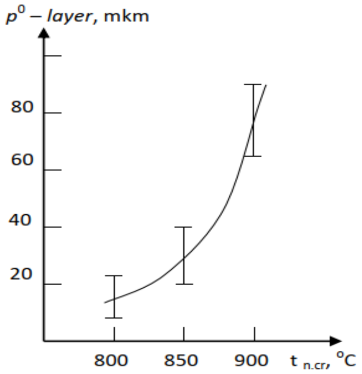

Fig. 1 – Dependence of the thickness of the p^0-layer on temperature

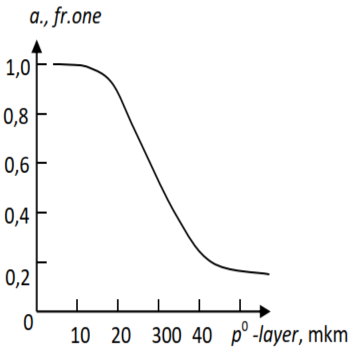

Fig. 2 – The dependence of the transfer coefficient on the p^0-layer

In the region of low values of α and large thicknesses of p^0-layer, there is a connection between α and production technology.

It can be seen that the choice of liquid phase annealing is preferable, which is justified due to the higher values of the transfer coefficient.

This is especially important for technological control of p^0. Figure 3 shows dependence of the transfer coefficient n^+-p^0-n^0 structures on temperature. It can be seen that α decrease with increasing temperature.

The decrease in α with increasing temperature can be explained by the temperature dependence of the capture cross section $G^A{}_n$ and $G^B{}_n$, which increase in this temperature range by factors of 5 and 20, respectively.

The effect of temperature at the beginning of crystallization and growth technology on the breakdown voltages ($U_{\text{trial.}}$) of a high-voltage p^0-n^0 junction was studied in n^+-p^0-n^0 structures for the possibility of obtaining maximum voltages at the collector junction (Fig. 4). The breakdown voltages increased significantly when p-n junctions turned out to be displaced from the metallurgical boundary and formed during growth.

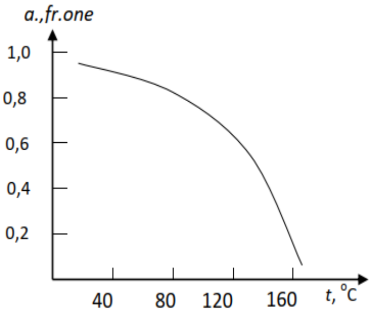

Fig. 3 – The dependence of the transfer coefficient n^+-p^0-n^0 structure on temperature

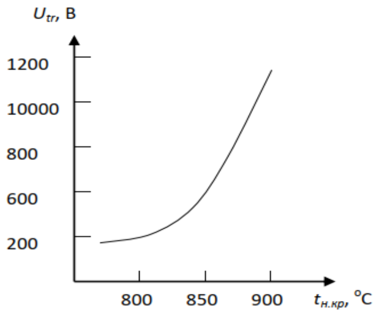

Fig. 4 – The dependence of $U_{tr.}$ high voltage p^0-n^0 transition on temperature

From Fig. 4 it can be seen that the values of U_{trial} is increase when using a higher temperature, the onset of crystallization. The growth of U_{trial} is explained. a decrease in the carrier concentration gradient in the region of the p-n junction. However, with an increase in the temperature of the onset of crystallization, the transfer coefficient of the resulting n^+-p^0-n^0 structures decreases. In high-voltage p^0-n^0 junctions, the allowable voltages are determined by the impurity concentration gradient in the space charge region (SCR) of the junction and the thickness of the n^0 region. Therefore, the carrier concentration gradient and the thickness of the n^0 region determine the breakdown voltages of the p-n junction. All research methodology developed and created in the course of the work performed is given in [31].

CONCLUSION

Thus, the above features of obtaining lightly doped layers and p-n junctions based on them show a real possibility of creating high-speed pulse transistors and thyristors. Optimization of the technology for obtaining high-voltage p-n junctions based on lightly doped GaAs layers, development of new principles for the generation and transport of charge carriers in semiconductor structures based on materials with a high proportion of radioactive recombination made it possible to obtain high-voltage three-electrode switches with sub nanosecond turn-on times. The studies carried out and the results achieved indicate broad prospects for the use of gallium arsenide and its solid solutions in the development of high-speed transistors and thyristors with a photon-injection coupling mechanism between p-n junctions.

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Дослідження впливу технологічних факторів на високовольтні p^0–n^0 переходи на основі GaAs

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Розроблено технологію та знайдено оптимальне рішення для отримання p^0-n^0 переходів на основі слаболегованих шарів GaAs з високими значеннями електричних параметрів і заданими товщинами базових шарів для створення надшвидкісних високовольтних імпульсних трьох -електродні перемикачі з фотонно-інжекційним механізмом перенесення безкворумних носіїв заряду. Досліджено залежність комутаційної стійкості від керуючого імпульсу створених високовольтних фотонно-інжекційних перемикачів у широкострумовому та частотному режимі їх роботи, його чутливість до різноманітних зовнішніх та внутрішніх впливів цих параметрів. Від товщини p^0-шару, від коефіцієнта передачі α, від напруги пробою Uтріал, високовольтного переходу p^0-n^0, від товщини розчину-розплаву, від температури початку кристалізації, а також як залежність коефіцієнта передачі від товщини p^0-шару.

Ключові слова: Рідкофазна епітаксія (РФЕ), Гетероструктури, Високовольтний p^0-n^0 перехід, Ефект Холла, Фонове легування, Розчин-розплав.