

Analysis of Charge Plasma Based Hetero Junction Nanowire Multi Channel Field Effect Transistor for Sub 10 nm

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This paper describes the design and development of a Nano Wire Multi Channel Field Effect Transistor (NWMCFET) with a gate length of 5 nm. The NWMCFET is created by splitting the Nanowire MCFET into four channels, and the charge plasma concept is employed during the design process using the Sentaurus TCAD simulation tool. To enhance the performance of the NWMCFET, Silicon Carbide (SiC) is utilized for the source and drain regions. The integration of SiC, combined with the utilization of a multi-bridge channel and the device's Ultra-Thin Body (UTB) technology, leads to an increased current drive capability. The Current-Voltage (I - V) characteristics of the device are plotted, and it is observed that these techniques result in a notable enhancement in current drive and overall performance. Additionally, the inclusion of hetero junction phenomena in the NWMCFET design further improves its performance. Consequently, the device incorporating the multi-channel and electrostatic doping idea demonstrates comparable results to manually doped devices. This finding highlights the potential of the proposed device design. Particularly, in the context of sub-10 nm devices, further development in this direction holds significant advantages. In summary, this paper presents a comprehensive exploration of a Nano Wire Multi Channel Field Effect Transistor design, utilizing the charge plasma concept, SiC material, and a multi-bridge channel configuration. The experimental results indicate improved current drive and overall device performance. Furthermore, the incorporation of hetero junction phenomena is found to be beneficial. The proposed design offers promising prospects for the development of sub-10 nm devices in the future.

Keywords: NWFET, Technology Computer-Aided Design (TCAD), UTB, MCFET, SiC, Charge plasma.

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1. INTRODUCTION

As the channel length of nanoscale devices is reduced, the task of creating nanoscale devices with remarkably high doping concentration gradients becomes more challenging. This increased difficulty results in higher levels of leakage current and the emergence of short-channel effects. In contrast, undoped intrinsic channels lack the ability to generate greater current in nanoscale devices when compared to their doped counterparts [1, 2].

The charge plasma (CP) method is a highly effective technique for introducing n-type and p-type carriers into intrinsic semiconductors. Numerous articles show how the CP approach was first used for a PN diodes in scientific and theoretical contexts. [3] and [4]. Since then, this notion has been effectively applied in other intricate devices, such as bipolar junction transistors (BJTs) [5-7], Junction less transistors, and Tunnel Field-Effect Transistors (TFETs) [8-10]. In such devices, the CP method concentrates on the Drain (D) and Source (S) electrodes by introducing metal in those regions, as the gate region cannot be positioned as in traditional devices.

The charge plasma concept finds potential application in the channel region along with the gate in the Multi Channel MOSFET (MCFET). The MCFET is a device that vertically stacks multiple channels on top of each other, and it has been successfully implemented in MOSFETs, Junction less transistors [11-13]. But it's important to remember that the CP method has only Using a Multi-Channel (MC) device's unique architecture,

which permits the positioning of the gate in the middle of the channel, the work being discussed introduces the application of the charge plasma approach especially in the channel region. This method has many advantages, particularly for very small nanometre-scale devices. The introduction of p^+ carriers happen as a result of employing the charge plasma concept in the channel region, resulting in the production of a p -type semiconductor. Due to the development of four Metal Oxide Semiconductor (MOS) structures as a result, the output current is increased and Short Channel Effects (SCE) are lessened in a single device.

The next phase of this paper has been split into subsequent sections: The proposed structure is extensively explored in Section Two, and the presentation and analysis of outcomes are dealt with in Section Three.

2. DEVICE STRUCTURE

The Sentaurus simulation in TCAD involves the formation of an n-channel Nanowire Field-Effect Transistor (NWFET) cylindrical structure, as shown in Fig. 1. The simulation parameters included a gate voltage (V_G) of 1.5 V, a drain voltage (V_D) of 1 V, and a gate length of 5 nm. To implement the Multi-Channel (MC) structure, four channels were introduced into the NWFET, and a heterojunction was created by replacing the original homo-junction structure. Specifically, 4H-SiC was used as the Source/Drain Material in place of Si. This heterojunction introduces a band offset between the junctions, resulting in a band-offset ΔE_c .

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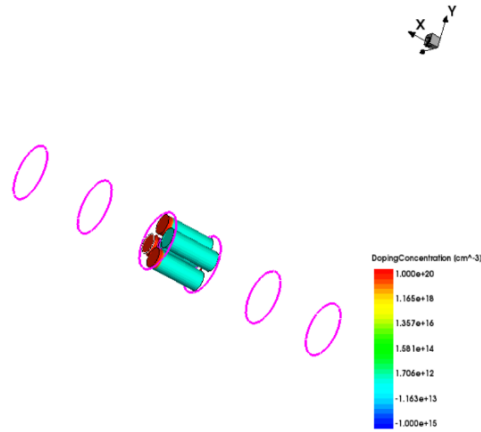


Fig. 1 – Device structure

Two distinct metal electrodes with various work function values make up a charge plasma. The metal electrode that is connected to the p-type region of the semiconductor is known as the "gated anode," and the metal electrode that is connected to the n-type region of the semiconductor is known as the "gated cathode." There is a potential difference between the two electrodes because the work function of the gated anode is higher than that of the gated cathode. A p-n junction is created as a result of the electric field that this potential difference creates in the semiconductor material.

After combining the multi-channel (MC) and heterojunction principles, simulations were carried out using TCAD software to compare the output current of the 5 nm device with that of the conventional device. Four nanowire channels, each with the same conduction area as the single-channel cylindrical construction, made up the suggested structure.

An oxide layer encircled each channel, and the gate was a direct metal contact with a 4.6 eV work function. The four channels were evenly spaced to maintain electrostatic integrity. The primary intent of this approach was to enhance the device's current-output driving capability without stretching it.

Figure [3] shows the SiC-Si-SiC heterojunction's conduction band diagram. Si and 4H-SiC have energy bandgaps (E_g) of 1.1 eV and 3.3 eV, respectively. When both the drain voltage (V_D) and gate voltage (V_G) are set to 0 V, the heterojunction barrier is initially high whilst the n-channel Multichannel MOSFET (MCFET). The barrier height is nonetheless decreased as the V_D voltage is raised. The better carrier injection from the source is made possible by this reduction, which raises the drain current.

By utilizing these features, a prospective CMOS device might be made that would improve neural networks and wireless applications, especially in low-power devices.

To simulate minority carrier recombination in the device architectures, which are depicted in Fig. 1, the Lombardi mobility model, Shockley-Read-Hall (SRH), and Auger recombination models are utilized. Quantum confinement effects on the device are also made possible by incorporating the Density- Gradient model [14]. Similar to the last simulation, the same model is used here because the proposed device also addresses quantum effects at shorter gate lengths.

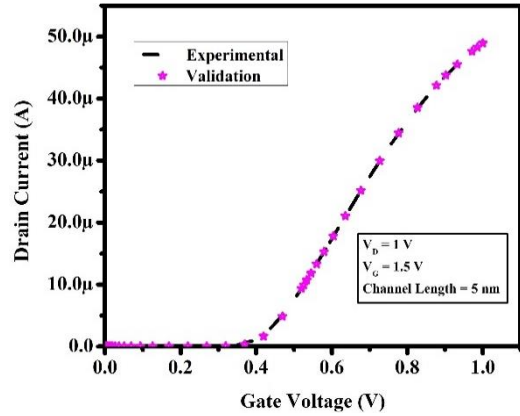


Fig. 2 – Validation of MBCFET structure

3. RESULTS AND DISCUSSION

3.1 Heterojunction

By substituting Silicon (Si) with Silicon carbide (SiC) in the source and drain regions to form hetero junctions, the band-offset ΔE_C is created which optimizes the velocity of electrons from the source. The hetero-junction theory states that because the source region's conductivity band is higher than the channel regions, the current drive is augmented. Additionally, the SiC areas in the source and drain regions act as stressors, elevating electron mobility by generating lateral tension and vertical compression in the channel. The output current drive eventually levitates as a result of an upsurge in electron mobility.

The device that has been proposed has a L_g of 5 nm which generates twice the current of the traditional one. Five nm in thickness channels of four different types are created.

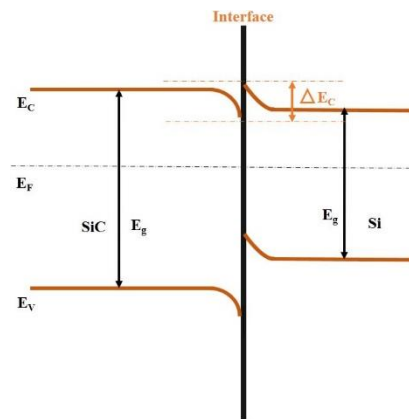


Fig. 3 – Heterojunction formation

Likewise, the experimental work [13] in Fig. 2 validated the MBC structure. The proposed design increases drain current as a result of MBC and Charge plasma. In Fig. 4, the output current is illustrated in which there is a similarity in between Nickel (work function = 4.6 eV) and Palladium (work function = 4.7 eV).

Fig. 5 illustrates the variations in the Threshold Voltage of the proposed structure for changes in the different work functions of the metal. The metalwork function, which ranges from nickel to tungsten, plays a significant role in these variations. The study includes two

different values: one with V_G set to 1.5 V and V_D set to 1.2 V, and the other with V_G set to 1.5 V and V_D set to 2 V. In both cases, the drain voltages are kept constant and higher than the applied gate bias. The analysis investigates how the metalwork function affects the Threshold voltage and I_{off} value of the devices

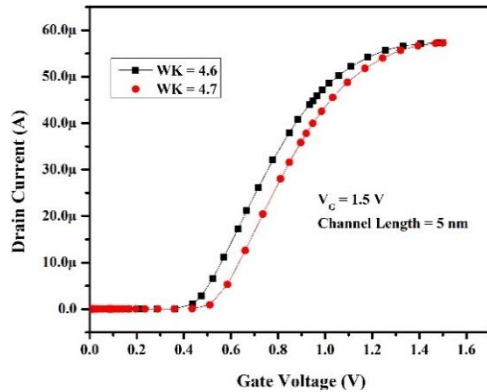


Fig. 4 – Output Characteristics of Device Structure

The determined Subthreshold Swing (SS) for a gate length of 5 nm is 87 mV/decade, and the corresponding I_{off} value is 4.4×10^{-10} A/ μm .

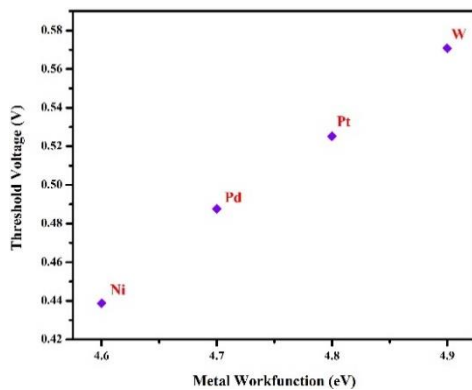


Fig. 5 – Analysis of the Threshold Voltage of the proposed structure for different metalwork functions

Table 1 – Analysis of Proposed Structure with Varying Gate Lengths

Lg	I _{off} (A)	SS (mV)
30 nm	4.72×10^{-15}	73
20 nm	1.8×10^{-14}	69
10 nm	1.4×10^{-13}	64
5 nm	4.6×10^{-10}	87

Up to a gate length of 10 nm, the SS increases to a larger value due to the narrow channel. However, beyond this threshold, the SS starts to decrease for decreasing gate lengths, indicating improved control over the leakage current and more efficient switching behaviour.

4. CONCLUSION

The study involves the integration of the charge plasma concept into a Nano Wire Multi Channel Field Effect Transistor (NWMCFET) with a gate length of 5 nm. In order to investigate the potential benefits of this approach, a four-channel NWMCFET with a 5 nm gate length was created using TCAD simulations. The device incorporates a multi-bridge channel and SiC, resulting in improved current-voltage (I - V) characteristics compared to conventional devices. Specifically, I - V characteristics were studied for metal work functions of 4.6 eV and 4.7 eV and found to exhibit superior drain current. It is anticipated that this approach will provide even greater benefits in the development of future devices with gate lengths of 5 nm and 3 nm.

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Аналіз багатоканального польового транзистора розміром менше ніж 10 нм на основі гетеропереходу на основі плазми електричних зарядів

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У статті представлені результати проектування та розробки нанодротового багатоканального польового транзистора (NWMCFET) із довжиною затвора 5 нм. NWMCFET створюється шляхом поділу нановолокна MCFET на чотири канали. Щоб підвищити продуктивність NWMCFET, карбід кремнію (SiC) використовується для областей витоку та стоку. Інтеграція SiC у поєднанні з використанням каналу з кількома мостами та технологією пристрою Ultra-Thin Body (UTB) приводить до збільшення потужності за струмом. Характеристики струм-напруга (I - V) пристрою дають змогу зробити висновок про те, що ці методи приводять до помітного покращення струму та загальної продуктивності. Крім того, включення явища гетеропереходу в конструкцію NWMCFET додатково покращує його продуктивність. Пристрій, що будується за принципом багатоканального та електростатичного легування, демонструє результати, порівняні з пристроями, легованими вручну. Зокрема, у контексті пристроїв із технологією менше 10 нм подальший розвиток у цьому напрямку має значні переваги. У роботі представлено дослідження багатоканального польового транзистора з нанодротом із використанням концепції зарядової плазми, з SiC та багатомостової конфігурації каналів. Експериментальні результати свідчать про покращення загальної продуктивності пристрою. Запропонована конструкція відкриває багатообіцяючі перспективи для розробки пристроїв із технологією менше 10 нм у майбутньому.

Ключові слова: NWFET, Технологія автоматизованого проектування (TCAD), UTB, MCFET, SiC, Плазма зарядів.