Performance Analysis of Charge-plasma Based Doping less Nanowire Field Effect Transistor

P. Raja*, P. Naveen Chander, B. Mohamed Faisal, V. Prakash

Department of ECE, Sri Manakula Vinayagar Engineering College, Puducherry, India

(Received 25 April 2023; revised manuscript received 23 June 2023; published online 30 June 2023)

The proposed work focuses on the outcomes brought about by the inclusion of Charge Plasma (CP) concept in a cylindrical Nanowire Field Effect Transistor (NWFET) for sub 10 nm. The Gate is surrounded by an oxide layer, which is further surrounded by a channel layer. The concept of charge-plasma is introduced in the channel by surrounding an oxide layer around the channel, and a different work functions metal layer around the oxide. The performance of device parameters like the electric potential and transfer characteristics have been described. Analysis of Threshold Voltage, drain current and Ion/IOFF ratio have been carried for 35 nm and 10 nm channel length. Sentaurus Technology Computer Aided Design (TCAD) has been used to evaluate and analyze this device for sub 10 nm. To calculate tunneling and recombination, the TCAD simulates the Lombardi mobility model, Shockley-Read-Hall (SRH), Density Gradient model, and Auger recombination models. This device generates twice times more output current by using the CP-based NWFET as compared to the conventional NWFET. The parasitic leakage has been reduced and the Ion/IOFF ratio has been stabilized. Also, the scalability is enhanced, and the Schottky junction’s high vertical field lowers the lateral coupling between the source and drain field lines. This can be used to implement in memory devices such as Inverter, 6T SRAM, 8T SRAM in future.

**Keywords:** Charge plasma, Gate-all-around, NWFET, Sentaurus TCAD, Doping less, Hole plasma.

DOI: 10.21272/jnep.15(3).03031 PACS numbers: 85.30.Tv, 81.07.Gf

1. INTRODUCTION

Device miniaturization to the nanometre-scale dimensions comes with a lot of challenges in fabrication. At the junction of the devices, obtaining a sharp doping concentration gradient is becoming a very challenging task as state-of-the-art MOSFETs scale down. This results in Short Channel Effect (SCE) of devices which gets more severe. As a result, a variety of structures have been suggested by the International Technology Roadmap for Semiconductors (ITRS), which include Gate-All-Around (GAA) Nanowire MOSFETs and Junction-less Fin field-effect transistors (JL FinFET). For getting a great performance among nano-level devices, GAA NWFET has a better possibility [1]. The GAA NWFET's geometric design might reduce short channel effects such as Drain Induced Barrier Lowering (DIBL), Sub-threshold Swing (SS), and Threshold Voltage (VTH) roll off [2-3]. Because of its greater electrostatic control ability over the channel and transport property, the Cylindrical GAA Transistor device has been chosen over other multi-gate MOSFET device structures [4].

To suppress short channel effects, the channel is completely surrounded by the metal gate in the GAA NWFET device [5]. It is regarded as one of the greatest multi-gate architectures due to its superior gate controllability and CMOS compatibility [6]. Although, GAA NWFET offers the best tolerance to SCE, achieving sharp doping concentrations on a small scale still remains problematic. To overcome this, the Charge Plasma (CP) technique offers an effective solution for introducing p-type as well as n-type carriers into the intrinsic semiconductor. This technique has been successfully applied to various devices, including the PN diode, BJT, JL transistor, TFET [7-9], and Multi Bridge Channel MOSFET (MBCFET). In MBCFET, the CP technique is utilized in the channel in conjunction with the gate, where the channels are stacked vertically one over another. The CP technique entirely demonstrates on the Source region and Drain region (S/D) [9-13].

This study proposes using the concept of charge plasma inside the channel of a GAA Nanowire FET (GAA NWFET) device in the form of a cylinder, with the gate being situated the channel, which would be particularly a benefit for ultra-small nanoscale devices. The aim is to use the CP concept to create a p-type semiconductor by inducing carriers of p-type in the channel region and vice-versa. This will result in the creation of carriers in the channel region without doping, boosting the overall device performance. The article is structured into two sections: Section 2 outlines the proposed structure, while Section 3 presents the results and discussion.

2. DEVICE STRUCTURE

The validation has been with the experimental data taken from Nayar [14] as depicted in Fig. 1. The designed device has a 5 nm thick channel area, a gate oxide thickness of 1.5 nm, and a gate length of 30 nm. The undoped silicon channel has a carrier concentration of about 10^{10} cm^{-2} and for S/D regions, the doping concentration is about 10^{16} cm^{-3}, with the gate metal having a work function of 4.7 eV. Channel thickness in the gate construction is 10 nm. The p+ channel area in the proposed structure is formed using the CP technique. To employ the charge-plasma approach, the following two conditions should be satisfied [9]: (i) The metallic contact work function in a channel should be greater than that of silicon in such a way that

\[ \varphi_m > \chi + (E_G/2q), \]  

where q is the charge of an electron, \( E_G \) is the bandgap
of Silicon, and $\chi_S$ is the Electron Affinity of Silicon. (ii) The channel thickness needs to be less than the Debye length $L_D = \sqrt{\varepsilon_i V_T q N}$, Where, $\varepsilon_i$ is the dielectric constant of silicon, $V_T$ is a Thermal Voltage, $N$ is carrier concentration.

To meet the first requirement, the channel metal contact is made of Cobalt, Gold, Palladium and Platinum with a corresponding work function of 5 eV, 5.1eV, 5.12 eV and 5.65 eV respectively. A channel with 5 nm thickness, which is thinner than $L_D$, satisfies the second criterion of the CP technique. To reduce the likelihood of silicide formation, a metal contact has been made in the device with a 0.5 nm gate length ($L_g$) between the channel and the source. Using a 0.5 nm thick HfO$_2$, the remaining silicon channel has been separated from the metal layer. The fabrication of the cylindrical structure using the CP method has been explained well by Nayak [14-16].

The proposed device as shown in Fig. 2 consists of a source terminal, a thick metal layer in the middle, and a drain terminal. Fig. 3 shows the 2D representation of the cylindrical structure consisting of a gate, surrounded by a gate oxide layer, which in turn is surrounded by an induced $p^+$ channel, followed a layer of oxide. This entire structure is enclosed by a metal layer, which has a contact with the channel near the source region in order to satisfy condition (i).

The device was designed and evaluated using Sentaurus TCAD, which is a computer-aided design tool commonly used in the semiconductor industry to aid design tool

![Fig. 1 – Comparison of NWFET with CP based NWFET of 35 nm](image1)

**Fig. 1** – Comparison of NWFET with CP based NWFET of 35 nm

![Fig. 2 – Proposed structure of charge-plasma based Doping-less Nanowire Field Effect Transistor](image2)

**Fig. 2** – Proposed structure of charge-plasma based Doping-less Nanowire Field Effect Transistor

![Fig. 3 – 2D representation of the cylindrical CP-NWFET structure simulate and optimize the processing and performance of different devices. The simulation models used to predict the behavior of carriers in the device and their recombination rates include the Lombardi mobility model, Shockley-Read-Hall (SRH) model, Auger recombination models and Density-Gradient model [17].](image3)

**Fig. 3** – 2D representation of the cylindrical CP-NWFET structure simulate and optimize the processing and performance of different devices. The simulation models used to predict the behavior of carriers in the device and their recombination rates include the Lombardi mobility model, Shockley-Read-Hall (SRH) model, Auger recombination models and Density-Gradient model [17].

3. RESULTS AND DISCUSSION

3.1 Electric Potential

The comparison between the potentials of the upper and lower part of the channel has been simulated as depicted in Fig. 4.

![Fig. 4 – Comparison of electric potential between upper and lower portion of channel in CP based NWFET](image4)

**Fig. 4** – Comparison of electric potential between upper and lower portion of channel in CP based NWFET

Due to the impact of the gate, the electric potential remains equal on both portions of the channel, which clearly indicates that the channel is controlled entirely by the gate even though the gate is placed in the middle of the channel. The graph has been plotted with a gate voltage of 0.02 V and a drain voltage of 0.2 V.

3.2 IV Characteristics

The CP based NWFET structure has been compared with the traditional NWFET [14] in Fig. 5. The validation was done for gate and drain voltages of 1.5 V each. The proposed device has a channel length of 10 nm and as indicated by the plot, it produces almost twice the current obtained by the conventional device, which is due to the work function of the metal layer formed on the outer surface of the device. Due to a high value of HfO$_2$ affinity value, the sub-threshold leakage is reduced, which in turn leads to reduced threshold voltage ($V_{TH}$).

The proposed device has an induced $p^+$ channel region that has carriers which is almost equal to the conventional doped channel devices. This in turn increases
the current flow which is mainly caused by the charge-plasma. As the drain voltage increases, the tunneling width becomes less dependent on the drain voltage, resulting in a saturation region in the output characteristics. The $I_{on}/I_{off}$ ratio gets influenced vastly by the charge-plasma. The ratio is higher in the CP-based NWFET with a value of $10^{10}$ as compared to that of NWFET with a value of $10^6$.

4. CONCLUSION

A NWFET structure based on charge-plasma has been demonstrated and compared to a NWFET structure. The suggested device provides nearly twice the output current compared to the traditional one by using the charge-plasma technique. The SS and the $I_{on}/I_{off}$ ratio are regulated by the metal layer generated for hole plasma. In short channel devices, performing manual doping is very complicated. Because of the charge plasma technique, the suggested device will be beneficial to overcome the difficulties of doping in the sub-10 nm. The proposed device can be used to implement SRAM and inverter circuits in future.

REFERENCES


Аналіз ефективності легування на основі зарядової плазми нанодротяного польового транзистора

P. Raja, P. Naveen Chander, B. Mohamed Faisal, V. Prakash

Department of ECE, Sri Manakula Vinayagar Engineering College, Puducherry, India

Запропонована стаття зосереджена на результатах, отриманих завдяки включенню концепції зарядової плазми (СР) у уламковий нанодротяний польовий транзистор (NWFET) для менше 10 нм. Ворота оточені шаром оксиду, дали – шар каналу. Концепція зарядової плазми вводиться в канал, оточуючи оксидний шар навколо каналу, і інший робочий рівень формує металевий шар навколо оксиду. Описано роботу таких параметрів пристрою, як електричний потенціал і характеристики передачі. Аналіз порогової напруги, струму витоку та співвідношення $I_{on}/I_{off}$ проводився для каналів діапазону 35 і 10 нм. Технологія Sentaurus Computer Aided Design (TCAD) була використана для вимірювання та аналізу цього пристрою для менше ніж 10 нм. Для обчислення туннелювання та рекомбінації, TCAD моделює модель мобільності Ломбарді, модель Шоклі–Ріда–Холла (SRH), модель градієнта щільності та моделі рекомбінації Оке. Цей пристрій теж створює вдвічі більший вихідний струм за допомогою NWFET на основі СР порівняно зі звичайним NWFET. Паралепігаритр витісняє зміни, а співвідношення $I_{on}/I_{off}$ стабілізоване. Крім того, покращується масштабованість, а високе вертикальне поле переходу Шоттки знижує бічний звільняє між силовими лініями витоку та стоку. У майбутньому це можна використовувати для реалізації таких пристроїв пам'яті, як інвертор, 6Т SRAM, 8Т SRAM.

Ключові слова: Зарядова плазма, Gate-all-around, NWFET, Sentaurus TCAD, Легування, Діркова плазма