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# Low Voltage Symmetric Dual-Gate Organic Field Effect Transistor

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Dual-gate organic field effect transistors (DG-OFETs), where two separate channels are formed at the organic semiconductor-dielectric interface, have attracted much attention owning to their high performance in comparison to single-gate OFET (SG-OFET). In this paper, an organic module of Atlas device simulator for a low voltage SG-OFET has been used to predict the electrical characteristics and performance parameters. Thereafter, an additional dielectric and gate electrode has been introduced to SG-OFET to achieve better performance. Electrical behaviors of low-voltage (≤ 3 V) DG-OFET have been studied by employing a symmetric configuration. This architecture exhibits a high drive current due to injection of sufficient charge carriers in both channels. The simulation results show higher drive current, carrier mobility and current on-off ratio, lower threshold voltage and subthreshold slope. These results demonstrate that the proposed symmetric configuration provide better performance when compared to the single gate.

**Keywords:** Organic Field Effect Transistors (OFET), Low voltage, Single-gate (SG), Dual-gate (DG), Symmetric, Numerical simulation.

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## 1. INTRODUCTION

Nowadays, organic electronics has attracted great attention since it has become the next promising generation of technology due to its advantages over inorganic electronics. Hence, using organic materials has become an important topic in the development of low-cost, flexible, large area, and lightweight devices [1]. Organic electronics is one of the fastest growing technology sectors, with a wide variety of applications already on the market, organic field-effect transistors (OFETs), organic light-emitting diodes (OLEDs), and Organic photovoltaics (OPVs) are now the most researched device applications. Lots of efforts have been devoted to improving performance and stability of OFETs, which is the key component of various flexible circuits; have led to the development of organic devices with high performance comparable to amorphous silicon-based semiconductors Si: H TFTs [2]. Research is going on to improve the OFET performances, in terms of high carrier mobility ($\mu$) and on-current (ION), low operating voltage, scaled down of channel length ($L$) and gate dielectric thickness [3, 4].

Also, the improvement in the OFET parameters can be achieved by variations in the structural placements [5]. OFETs are a construction containing an organic semiconductor (OSC) as active layer, an insulating layer, and source-drain-gate electrodes. These layers and electrodes are arranged in different devices structure, four OFET structures can be defined by the positions of the gate, source and drain electrodes according to the gate dielectric and organic semiconductor layer respectively, which is known as top gate (TG) and bottom gate (BG), top contact (TC) and bottom contact (BC). One other solution is the dual-gate (DG) configuration, the secondary gate helps to improve the performance of OFET in comparison to the single gate (SG) such as, higher device mobility and current on-off ratio, lower threshold voltage and subthreshold slope [6]. Extensive research in which field, process development and device optimization have shown that the characteristics of organic transistors can be certainly improved when the OFETs operated in a dual gate mode [7].

OFETs operate in the accumulation mode, source and drain electrodes are meant for charge carriers injection and extraction, respectively from the OSC layer whereas; the biasing of the gate electrode induces the charging of the insulator-OSC interface. The DG OFET can be operated in two different modes, such as single gate (top gate or bottom gate) and dual gate mode. So, there can be two conducting channels for this configuration, which are formed at both top and bottom insulator-OSC interface when an adequate biasing is applied to both electrodes gate [6]. OFET low-voltage operation can be achieved by increasing the capacitance of gate dielectric, i.e. a dielectric having either a small thickness of dielectric layers and/or a high-k dielectric permittivity [8]. Low-voltage operation with low leakage current including $Al_2O_3$ as gate dielectric has been studied, which is indicated the high quality of the $Al_2O_3$ dielectric. The merit of $Al_2O_3$ is that is can be fabricated at low temperature as well as does not damage the active layer [9]. Shiwaku et al. [10] was the first to report the low voltage (< 5 V) DG-OTFT in 2018, to obtain a high-performance with charge carrier distributions was imaged.

Analysis behaviors of low-voltage and high-voltage dual gate organic thin-film transistors have been produced with an asymmetric contact configuration, whereas the source and drain electrodes are placed under or the above the OSC. Most of charge carriers accumulate in the first monolayer next to the insulator-OSC interface in both sides, and thus justifies forming two separate channels in DG OFET. However, the charge carriers have different concentration even with similar gate biasing due to thickness of dielectric resulting in a higher or lower capacitance.

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This paper presents the performance of low-voltage organic transistor in TC configuration. The OFET simulation was performed using finite element device simulator, the electrical characteristics obtained by simulation are verified with experimental results. Thereafter, SG-OFET is analyzed with an additional dielectric and top gate electrode. The proposed DG-OFET with symmetric contact configuration is analyzed using organic module of Atlas device simulator to present the performance of the device in terms of electrical parameters such as mobility $\mu$, on-off current, threshold voltage $V_{Th}$, and subthreshold $SS$.

## 2. METHODS AND SIMULATION SETUP

Silvaco (Atlas) 2-D numerical device simulator has been used to investigate the transfer and output characteristics of the single gate p-type OFET. Then, we exploit the results obtained and suggest a dual-gate OFET with symmetric configuration, for predicting electrical behaviors and properties which are linked with physical structure and biasing conditions

The device structure of low-voltage SG-OFET is formed by stacking several layers as shown in Fig. 1, $Al_2O_3$ is used as dielectric with capacitance of 0,7 μF/cm² [11].

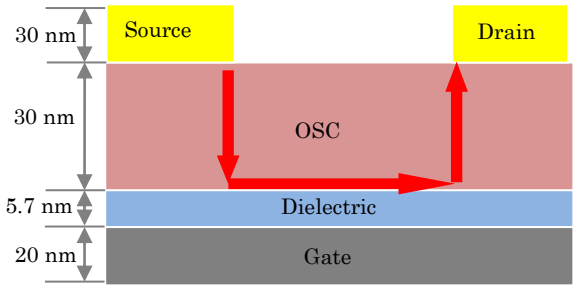



**Fig. 1** – Schematic structure of single gate top contact organic field effect transistor

The simulation was based on the Poisson's and carrier continuity equations, which is done with a one-carrier model of the hole.

$$\varepsilon\nabla^2\psi = -pq\,, \tag{2.1}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla.j_p + G_p - R_p\,, \tag{2.2}$$

where $\varepsilon$ is dielectric constant, $\psi$ is electrostatic potential, $p$ is hole carrier concentration, $q$ is the elementary charge, $J_p$ is the hole current density, $G_p$ and $R_p$ are the carrier generation and recombination rate.

The drift and diffusion charge transport model for the hole current density is given by:

$$j_p = pq\mu_p F + qD_p\mu_p\,, \tag{2.3}$$

where $\mu_p$ is the hole mobility, $F$ is the electric field, and $D_p$ is the hole diffusion coefficient.

To analyze the static and dynamic behavior of the device, Poole-Frenkel mobility model for holes is applied to define the dependency of mobility capability due to electric field $\mu$(E), which is expressed as [12,13].

$$\mu(E) = \mu_0 \exp\left[-\frac{\Delta}{KT} + \left(\frac{\beta}{KT} - \gamma\right)\sqrt{E}\right], \tag{2.4}$$

Here $\mu_0$ is the zero field mobility (when the drain voltage $V_D = 0$), E is the electric field, $k$ and $T$ represent the Boltzmann constant and temperature, respectively. Parameters Δ, $\beta$ and $\gamma$ is the activation energy and hole Poole-Frenkel factor respectively, whereas, $\gamma$ is used as the fitting parameter.

**Table 1** — Device dimensions of SG-OFET [11]

| Dimensional parameter | Value |
|---|---|
| Channel length | 10 μm |
| Channel width | 100 μm |
| Thickness of OSC (Pentacene) | 30 nm |
| Thickness of Dielectric ( $Al_2O_3$) | 5.7 nm |
| Thickness of gate electrode (Aluminum) | 20 nm |
| Thickness of S/D contact (Gold) | 30 nm |

**Table 2** — Parameters used in 2-D numerical device simulator

| Material | Parameters | Value |
|---|---|---|
| Pentacene | Band gap ($E_g$) | 2.2 $eV$ |
| | Affinity ($\chi$) | 2.8 $eV$ |
| | Permittivity ($\varepsilon_r$) | 4.0 |
| | Density of conduction band ($N_C$) | $2 \times 10^{21}$ $cm^{-3}$ |
| | Density of valence band ($N_V$) | $2 \times 10^{21}$ $cm^{-3}$ |
| | Acceptor doping concentration ($D_A$) | $4 \times 10^{17}$ $cm^{-3}$ |
| | Activation energy ($\Delta$) | 0.018 $eV$ |
| | Hole Poole–Frenkel factor ($\beta$) | $7.758 \times 10^{-5}$ eV (cm / V)$^{0.5}$ |
| Aluminum oxide ($Al_2O_3$) | Dielectric constant (K) | 4.5 |
| $Al_2O_3$ / pentacene interface | Interface charge ($Q_F$) | $2 \times 10^{12}$ $cm^{-2}$ |
| Gold (source & drain) | work function | 5.1 |
| Aluminum (Gate) | work function | 4.3 |
| - | Temperature (T) | 300 $K$ |

The material and model parameters of SG-OFET used in the simulation are summarized in Table 1 and Table 2.

## 3. RESULTS AND DISCUSSION

### 3.1 Performance of Single Gate OFET

When the bias voltage is applied to the gate electrode, a thin accumulation region constitutes the major current flow near the OSC-dielectric interface, which is called the accumulation layer of the OFET. The 2D simulation visualizes the current flow lines contour and hole concentration at dielectric interface in the OSC of the SG-OFET, as illustrated in Fig. 2.

Fig. 2 shows the simulated structures of SG-OFET, where a thin accumulation layer at OSC–dielectric interface can be clearly observed, that representing channel formation from source to drain contacts.

The hole concentration is higher and homogeneous in

the linear regime than the saturation regime as depicted in Fig. 3. Moreover, the hole concentration degrades from the drain side due to the depletion mode.

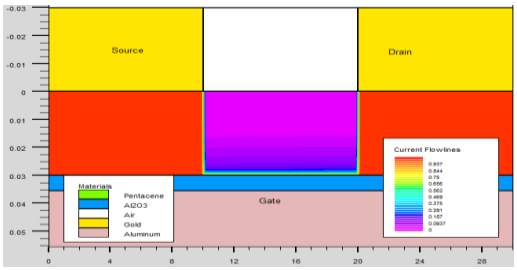



**Fig. 2** – Current flow lines contour profile on the SG-OFET structure at $V_{gs} = -3$ V and $V_{ds} = -0.1$ V

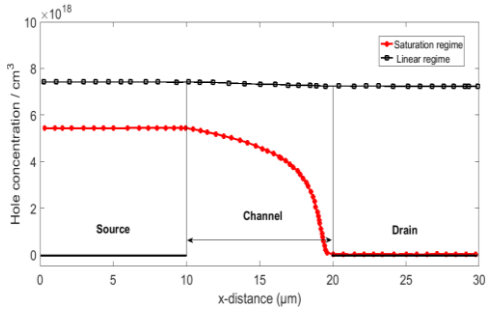



**Fig. 3** – Hole concentration along x-distance at the insulator/OSC interface for linear regime ($V_{ds} = -0.1$ V), and saturation regime ($V_{ds} = -3$ V)

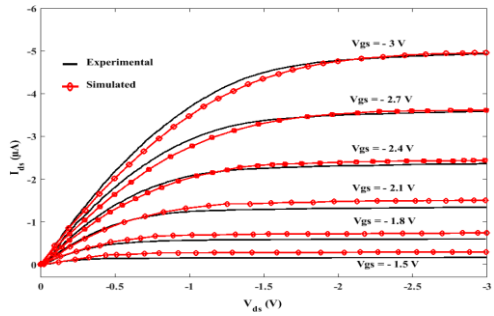



**Fig. 4** – Comparison of experimental and simulation: (a) output characteristics, (b) transfer characteristics of SG-OFET

The output and transfer characteristics of p-type SG-OFET are shown in Fig. 4 a, b, respectively. It is observed that the simulation results predicted from the Atlas 2D numerical device simulator are in good agreement with the experimental data.

The performance parameters for SG-OFET structure are verified with reported experimental results, as summarized in Table 3. We note that the difference in the simulation results is caused by several parameters fittings in the device simulator.

**Table 3** – Simulated and experimental parameters of SG-OFET

| Parameters | SG-OFET [$V_{gs} > -2.5$ V, $V_{ds} = -1.5$ V] | |
|---|---|---|
| | Simulated | Experimental [11] |
| Threshold voltage, $V_{TH}$ (V) | – 1.305 | – 1.2 |
| Mobility, $\mu$(cm$^2$ / V·s) | 0.57 | 0.4 |
| Subthreshold slope, SS (mV / dec) | 86.72 | 100 |
| Transconductance, $g_m(\mu S)$ | 4.13 | 4 |
| Current on-off ratio, $I_{on}/I_{off}$ [$V_{gs} = V_{ds} = -3$ V, $V_{gs} = 0$] | $5.88 \times 10^7$ | $10^7$ |

The performance parameters for SG-OFET structure are verified with reported experimental results, as summarized in Table 3. We note that the difference in the simulation results is caused by several parameters fittings in the device simulator.

### 3.2 Performance of Symmetric dual gate OFET

Structural modification of placements of contact is a well-known scheme to improve the performance of dual-gate organic transistors. DG-OFET structure is classified as top contacts organic field effect transistors (TC-OFETs) and bottom contact organic field effect transistors (BC-OFETs), depending on the placements of source/drain (S/D) electrodes above or below the OSC. Therefore, two separate channels can be formed within a few nanometers from the gate dielectric-OSC interface. This configuration exhibits a large difference of charge injection from source to the OSC in both channels [14].

The improvement in the performance of DG-OFET can also be achieved by forming a good interface at OSC/dielectric, which is leading to lesser traps and benefits the charge transport interface in device. $Al_2O_3$ is good for low-voltage operation of OFETs due to its low trap density, low temperature fabrication which has the advantage of avoiding damage the organic semiconductor layer [9, 14]. The proposed dual-gate symmetric-contact device structure of the low-voltage OFET was obtained by placing two *S*/*D* electrodes either in the middle of active layer, as shown in Fig. 5.

The performance of SG-OFET and DG-OFET configurations is analyzed in terms of parameters and electrical characteristics with geometric symmetry, same materials and operating conditions to make an appropriate comparison between them (Table 1 and 2).

Atlas 2D numerical device simulator displays the current flowlines contour and hole concentration along x-distance at the insulator/OSC interface in the DG-OFET while transistor is operated in the top, bottom and dual-gate modes, respectively as shown in Fig. 6 a, b, and c. However, it should be mentioned that the bottom and top gate electrode was connected each other for the dual-gate mode ($V_{TG} = V_{BG} = V_{GS}$).

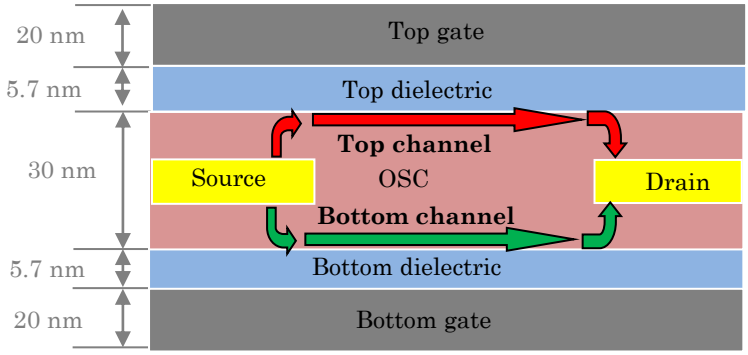
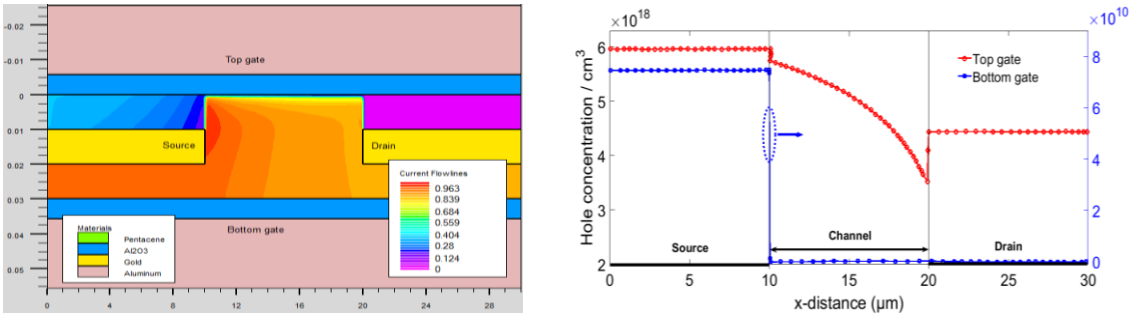
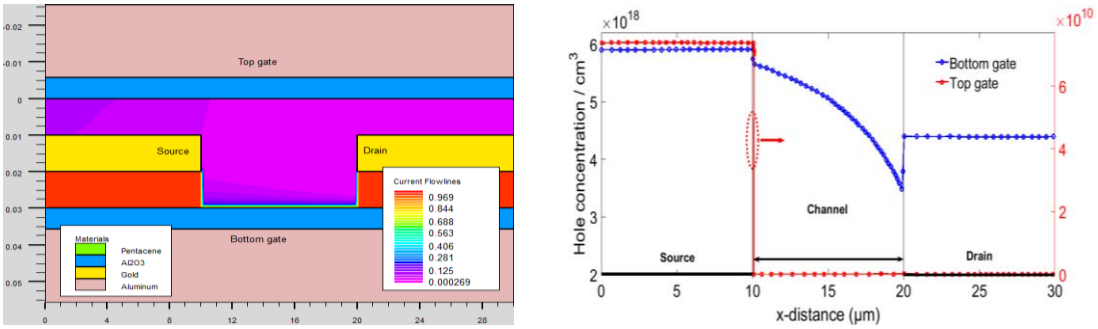


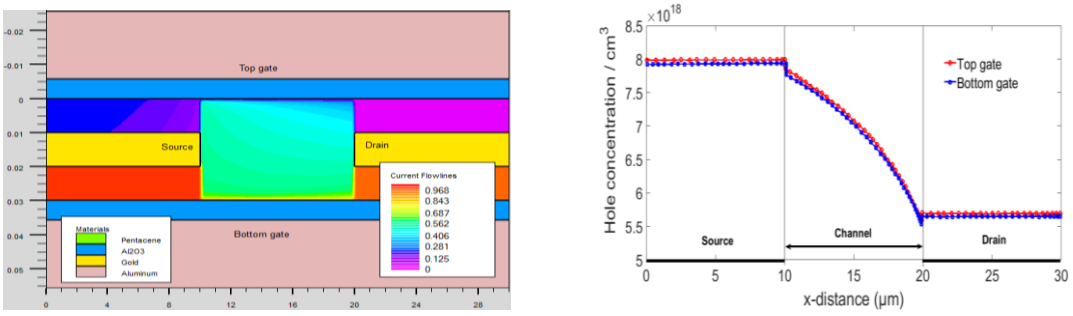

**Fig. 5** – Schematic structure of the proposed Symmetric dual organic field effect transistor




a




b




c

**Fig. 6** – Simulated contour of current flowlines and hole concentration nearby the dielectric interface of the DG-OFET with three different configurations at $V_{DS} = -1$ V: (a) Top gate mode ($V_{TG} = -3$ V, $V_{BG} = 0$ V), (b) bottom gate mode ($V_{TG} = 0$ V, $V_{BG} = -3$ V) and (c) dual gate mode ($V_{TG} = V_{BG} = -3$ V)

The hole concentration is equally in both single-gate mode (top gate or bottom gate modes), which means that the majority charge carriers is concentrate properly at the dielectric-OSC interface (accumulation layer) while biasing is applied at the gates as shown in Fig. 6, whereas it is higher for dual-gate mode in both channels.

The output and transfer characteristics of DG-OFET with three different configurations under differ-

ent $V_G$ values are shown in Fig. 7. It can be observed that during TG or BG mode, the proposed dual-gate exhibited identical transfer and output characteristics, which leads to symmetric operation.

According to the output characteristics of Fig. 7 a, b, and c, the on-current of DG-OFET mode $I_{ONDG}$ (at $V_{ds} = V_{TG} = V_{BG} = -3$ V) is higher by 2.8 times than the $I_{ONTG}$ in TG mode or $I_{ONBG}$ in BG mode ($I_{ONDG} \approx (I_{ONBG} + I_{ONTG}) \times 1.4$).

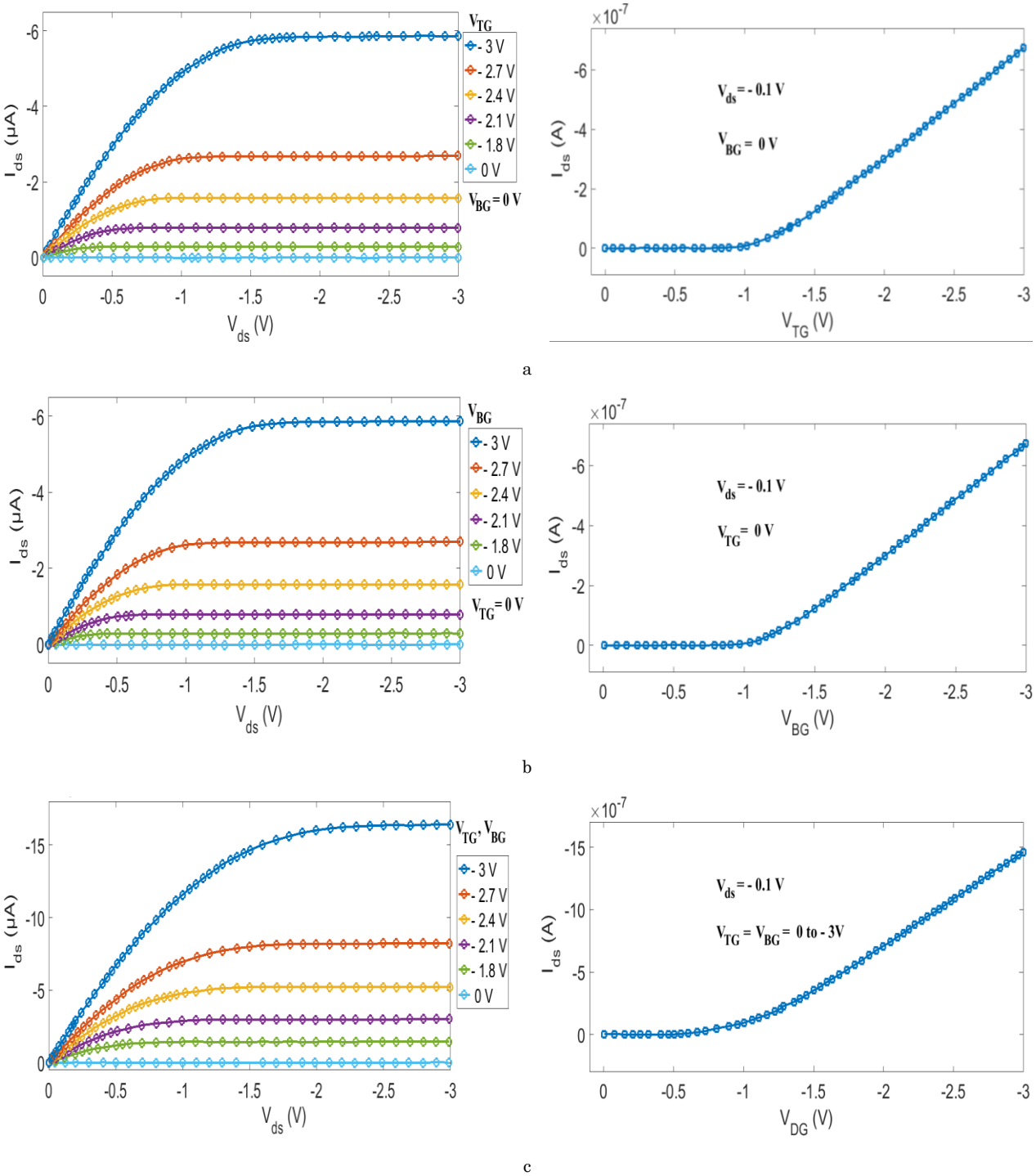



**Fig. 7** – Output and transfer characteristics of DG-OFET with three different configurations: (a) Top-gate (TG), (b) Bottom-gate (BG), and (c) Dual-gate (DG)

The extracted performance parameters, such as $V_{TH}$, $\mu$, $SS$, $g_m$ and $I_{on}/I_{off}$ of the low-voltage Symmetric DG-OFET for different operating modes are summarized in Table 4.

It is observed that DG-OFET configuration shows the superior result when compared with TG and BG modes. The DG-OFET demonstrates an increment of 2.6 and 5 times for hole mobility and current on-off ratio, respectively in comparison to the TG and BG modes.

**Table 4** – Simulated parameters of Symmetric DG-OFET operating in top, bottom, and dual gate configurations

| Parameters | [$V_{gs} > -2.5$ V, $V_{ds} = -1.5$ V] | | |
|---|---|---|---|
| | TG | BG | TG |
| Threshold voltage, $V_{TH}$ (V) | − 1.215 | − 1.215 | − 0.75 |
| Mobility, $\mu$(cm² / V.s) | 0.543 | 0.539 | 1.42 |
| Subthreshold slope, SS (mV / dec) | 204 | 212 | 153 |
| Transconductance, $g_m$ (μS) | 5.648 | 5.639 | 11.49 |
| Current on-off ratio, $I_{on}/I_{off}$ [$V_{gs} = V_{ds} = -3$ V, $V_{gs} = 0$] | $3.634 \times 10^7$ | $3.627 \times 10^7$ | $1.79 \times 10^7$ |

Additionally, a reduction of 38 % in threshold voltage is observed, the transconductance in the DG mode is also higher by two times than the TG and BG modes. Besides this, sub-threshold slope is reduced by 25 and 28 % for TG and BG modes.

Compared to single-gate (Table 3), the OFET in dual-gate mode demonstrates an improvement of 44 % and 60 % in threshold voltage and hole mobility, respectively. Also, the current on-off ratio and transconductance are higher by 3 and 2.8 times for DG respectively, due to formation of channel at both bottom and top gate side.

## 4. CONCLUSION

In this paper, we present the performance of SG-OFET using Silvaco (Atlas) 2D numerical device simulator, which is evaluated and verified with the reported experimental results. Then, we propose a symmetric dual-gate OFET configuration to address the effect of the proposed structure on the device behavior.

By using a thin high capacitance dielectric layer combined with a secondary gate, the resulting transistor produces a dual-channel within the OSC at the interface with the dielectric layer, and that allows achieving better charge carrier modulation, which leads to better performance of DG-OFET. Compared to single-gate, the OFET in dual-gate mode demonstrates higher performance parameters such as, higher mobility ($\mu$), higher on/off current ratio, higher transconductance ($g_m$), and lower threshold voltage. Such set significant information is much desirous for the better comprehension of a low-voltage DG organic transistors behavior, and a key motivation to improve the performance of the devices.

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## Низьковольтний симетричний двозатворний органічний польовий транзистор


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Двозатворні органічні польові транзистори (DG-OFET), де два окремі канали формуються на межі поділу органічний напівпровідник-діелектрик, привертають велику увагу завдяки своїй високій продуктивності порівняно з однозатворними OFET (SG-OFET). У цій статті органічний модуль симулятора пристрою Atlas для низьковольтного SG-OFET використовувався для прогнозування електричних характеристик і параметрів продуктивності. Після цього в SG-OFET було введено додатковий діелектрик і електрод затвора для досягнення кращої продуктивності. Електрична поведінка низьковольтного (≤ 3 В) DG-OFET досліджувалась із застосуванням симетричної конфігурації. Ця архітектура демонструє високий струм приводу через інжекцію достатньої кількості носіїв заряду в обидва канали. Результати моделювання показують вищий струм приводу, рухливість несучої та коефіцієнт увімкнення/вимкнення струму, нижчу порогову напругу та підпорогову крутизну. Запропонована симетрична конфігурація забезпечує кращу продуктивність в порівнянні з транзистором з одним затвором.



**Ключові слова:** Органічні польові транзистори (OFET), Низька напруга, Однозатворні (SG) транзистори, Двозатворні (DG) транзистори, Симетричні транзистори, Чисельне моделювання.