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Performance Analysis of Incorporating a Buried Metal Layer in a Junction-Less Multi-Channel Field Effect Transistor

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This work focuses on the outcomes brought about by the incorporation of Buried Metal Layer (BML) in a Junction-less Multi-Channel Field Effect Transistor (JL MCFET). Two stacked channels separated by an inter-oxide layer, one having a Trigate structure and other having a Double gate structure, have been implemented with a BML and it has been formed as Junction-less Buried Metal Layer Multi-Channel Field Effect Transistor (JL BML-MCFET). A Schottky junction is created at the bottom of the device layer by adding a buried metal layer with sufficient work function. The performance of device parameters like the electric potential and IV characteristics have been described. Sentaurus Technology Computer Aided Design (TCAD) was used to evaluate this device. To calculate tunneling and recombination, the TCAD simulates the Lombardi mobility model, Shockley-Read-Hall (SRH), and Auger recombination models. This device generates four times more output current by employing buried metal layer. The parasitic leakage has been reduced and the I_{ON}/I_{OFF} ratio has been stabilized. Even though the gate voltage has been raised to greater levels, the subthreshold swing (SS) value has been kept at an Ideal value of about 60 mV/dec. Also, the scalability is enhanced, and the Schottky junction's high vertical field lowers the lateral coupling between the source and drain field lines.

Keywords: Junction less transistor, Multi channel, Buried metal layer, Sentaurus TCAD.

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1. INTRODUCTION

Due to their simplicity in manufacture and lesser thermal budget concerns compared to traditional devices, junction-less transistor devices have been the focus of researchers. In 2010, the first junction-less nanowire transistor was created [1]. Later, the JL concept was used in numerous devices, including FinFET, gate-all-around, thin film transistor, Tunnel FET, double gate, tri-gate and double gate devices [2]. Device layer having n^+-source, n^+-channel, and n^+-drain without any source/channel/drain junctions laterally makes up an n-channel junction-less transistor. Be-cause the channel carriers are depleted during the OFF state of the p-type high gate work function, the device layer has an inherent n^+-i-n^+ structure. Volume conduction makes it possible for the drain current to flow while the switch is in the ON-state. Nonetheless, it is noted that erroneous turn-off and excessive leakage (high sub-threshold swing) have drawbacks [3-4]. The junction-less transistors were shown to be more sensitive to the T_{Si}/W_{Si} ratio and to produce lesser I_{ON} when compared to junction transistors.

The multi-channel idea has been adopted to boost the drain current [5-6]. Even if the channel length has been decreased, the current may still be increased by stacking channels on top of one another [7]. The device was constructed using the SOI (Silicon-on-insulator) fabrication method, in which a semiconductor layer is deposited on top of a buried oxide layer to minimize substrate leakage [8]. A BML is included to improve the reduction of leakage current even more. With the aid of a Schottky junction, it creates a depletion layer that extends the entire bottom of the device layer and aids in attaining carrier volume depletion in the OFF-state. Therefore, it is anticipated that I_{OFF} will decrease. Furthermore, a considerable decrease in parasitic leakage is shown in [9]. Moreover, by dramatically decreasing Short Channel Effects (SCEs) such as threshold voltage (V_{th}) roll-off and drain induced barrier lowering (DIBL), BML enhances the scalability of the device.

In this work, two channels have been formed one over another with intermediate gate oxide. Tri-Gate structure is present in the top channel and the bottom channel has a Double gate structure [10-11]. The BML has been incorporated in this JL multi-channel structure which makes the proposed structure is suitable for suppressing leakage currents. The rest of the paper is divided into device structure, Result and Discussion and Conclusion.

2. DEVICE STRUCTURE

Using the parameters from [12], a junction-less transistor has been created and simulated in Sentaurus TCAD as seen in Fig. 1. V_{GS} and V_{DS} are kept at 1.3 and 1.5 Volts, respectively, while the device is being examined. As per Fig. 2, the JL Multi-channel transistor has been constructed. For both channels, the width is 20 nm, and has a 1000 nm and 10 nm channel length and thickness, respectively. The thickness of the inter-oxide layer is chosen as 40 nm. A $2 \times 10^{17}\,\mathrm{cm}^{-3}$ doping concentration was uniformly deposited on the source, drain, and channel. For the gate oxide and inter-oxide layer, HfO_2 was used [13]. For the buried oxide layer, SiO_2 was used [14]. Two stacked channels separated by an inter-oxide layer is introduced.

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Due to inter-oxide, the channel 2 is covered with three sides which act as like Tri-Gate and Channel 1 act as a double gate since channel 1 covered only with two sides. A buried metal layer was introduced in between the channel 1 and the buried oxide layer shown in the Fig. 3. $Ø_{BM} > Ø_{Si}$, where, $Ø_{Si}$ is the work function of n-doped Si. With barrier height equal to the work function of buried metal layer minus the electron affinity of Si, this creates the Schottky junction at the BML/*n*-Si device layer interface [15]

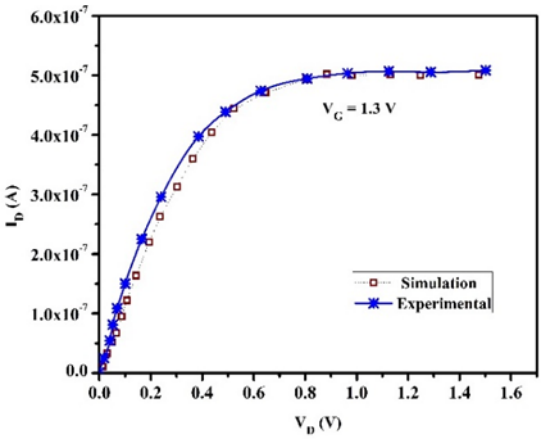

Fig. 1 – Validation with experimental work [1]

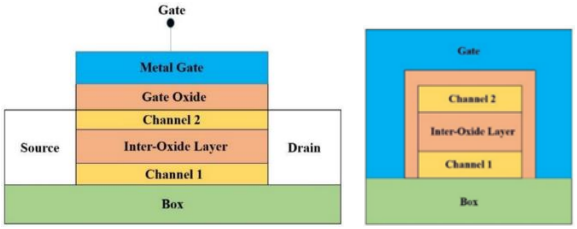

Fig. 2 – Multichannel in a junction-less thin film transistor

As a result, this device features a vertical Schottky junction isolation [3]. With the aid of a Schottky junction, a depletion layer is formed at the bottom device layer by the buried metal layer.

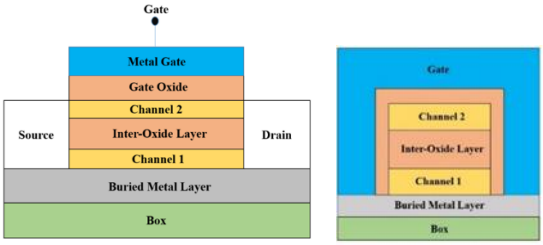

Fig. 3 – Multichannel junction-less transistor with Buried Metal Layer

Sentaurus Technology Computer Aided Design (TCAD) was used to construct and evaluate the device. TCAD is utilized to execute computational simulations to create and assess semiconductor processing methods for various sorts of devices. Minority carrier recombination in the device designs is simulated using the Lombardi mobility model, SRH, and Auger recombination models [16-17].

3. RESULTS AND DISCUSSION

3.1 Electric Potential

After the inclusion of BML to the multi-channel JL, the potential comparison between channel 1 and chan-nel 2 was simulated and shown as illustrated in Fig. 4. Due to the impact of the Tri-Gate structure, channel 2 has a slightly higher electric potential than channel 1. The graph has been drawn with a 0.02 V gate voltage and a 0.2 V drain voltage. The graph demonstrates that channel 1 and channel 2 are entirely under the control of the gate [18].

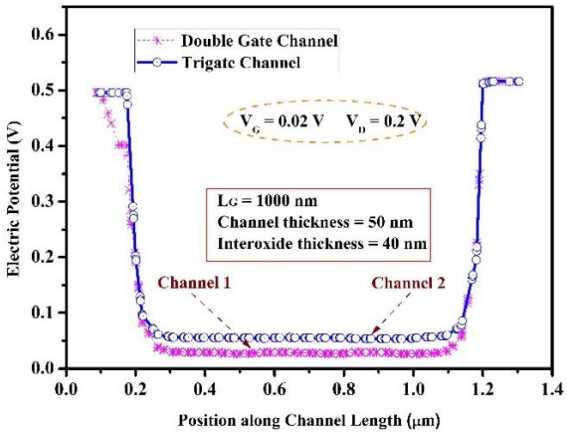

Fig. 4 – Comparison of electric potential between channel 1 & channel 2 in JL BML-MCFET

3.2 Drain Current

Based on a comparison between the JL multi-channel transistor with and without a buried metal layer, the transfer characteristics are presented in Fig. 4. By starting with V_{DS} at 1 V and changing V_{GS} be-tween 0 and 1.5 V, transfer characteristics are plotted. The effect of double channel has led to an increase in drain current in JL MCFET. In JL-BML MCFET, the drain current has grown to around 4 times better cur-rent than JL MCFET as a consequence electrons tunneling from the valence band to the conduction band of the channel.

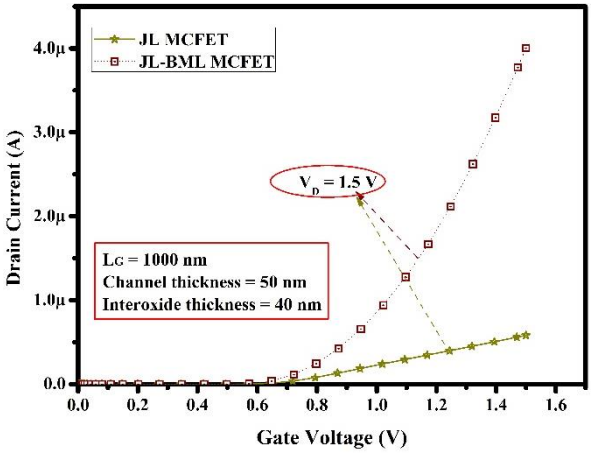

Fig. 5 – Transfer characteristics comparison JL MCFET and JL BML-MCFET

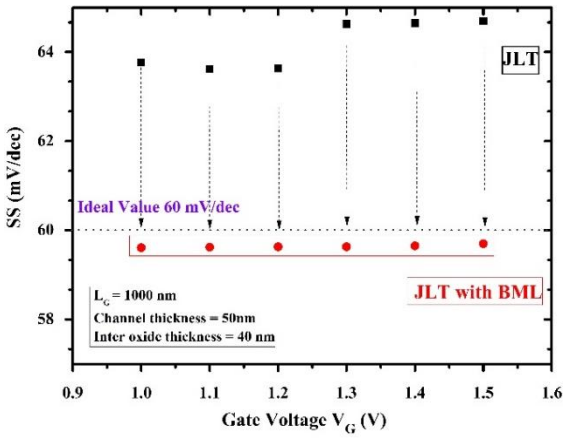

Fig. 6 – Comparison of the SS between JL MCFET and JC BML-MCFET

The I_{ON}/I_{OFF} ratio is influenced by the BML length reduction since it causes more parasitic leakage. Due to that, throughout the simulation, the BML length is maintained as a constant. JL BML-MCFET IOFF current leakage controlled 6 times better than JL MCFET. A transistor's behavior in the sub threshold region is determined by a value called the sub threshold swing [19]. The values of subthreshold swing for JL-MCFET and JL BML-MCFET are displayed against gate voltage in Fig. 6. The optimum subthreshold swing at room temperature is 60 mV/dec. The difference is clearly observed that for Double channel JLT without BML goes beyond the ideal value and the one with BML is around the ideal value of sub-threshold swing.

4. CONCLUSION

In this work, the novelty structure of a Junction-less Multi-Channel Field Effect Transistor employing a Buried Metal Layer has been implemented. At the bottom of the device layer, a concept of a Schottky junction-induced depletion layer is utilized to improve the I_{ON}/I_{OFF} ratio in the device. A four times increase has been achieved by the drain current compare with JL MCFET. As, the subthreshold swing remains in the ideal value, parasitic leakage is controlled. Being a thin film transistor with high driving current capabilities, this device can be employed in AMOLED applications.

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Аналіз продуктивності включення прихованого металевого шару в безперехідний багатоканальний польовий транзистор

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Дана робота зосереджена на результатах, отриманих завдяки введенню металевого шару (BML) у багатоканальний польовий транзистор (JL MCFET) без переходів. Два складені канали, розділені міжоксидним шаром, один із яких має структуру Trigate, а інший має структуру подвійного затвора, були реалізовані за допомогою BML, і він був сформований як багатоканальний польовий ефект заглибленого металевого шару без спаїв. ідеальний транзистор (JL BML-MCFET). Перехід Шотткі створюється в нижній частині шару пристрою шляхом додавання прихованого металевого шару з достатньою робочою функцією. Описано роботу таких параметрів пристрою, як електричний потенціал і *I-V* характеристики. Технологія Sentaurus Computer Aided Design (TCAD) була використана для оцінки цього пристрою. Для обчислення тунелювання та рекомбінаціъ, TCAD моделює модель мобільності Ломбарді, моделі Шоклі-Ріда-Холла (SRH) і моделі оже-рекомбінації. Цей пристрій генерує в чотири рази більший вихідний струм, використовуючи захований металевий шар. Паразитарний витік зменшено, а співвідношення I_{ON}/I_{OFF} стабілізовано. Незважаючи на те, що напруга на затворі була підвищена до більш високих рівнів, підпорогове значення коливання зберігається на ідеальному значенні приблизно 60 мВ/дек. Крім того, покращується масштабованість, а високе вертикальне поле переходу Шотткі знижує зв'язок між силовими лініями витоку та стоку.

Ключові слова: Безперехідний транзистор, Багатоканальна структура, Прихований металевий шар, Sentaurus TCAD.