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Implementation of a Linearly Graded Binary Metal Gate Work Function VTFET with Air Pocket

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In the present paper, the linearly graded work function (LG-W) characteristics are explored by using binary metal alloy $a_\sigma b_{1-\sigma}$ gate electrode composition in a high-k gate stack with a dielectric pocket in vertically aligned TFET (VTFET). The VTFET device is constructed using a binary metal alloy gate electrode with a linearly graded work function and an air pocket. The proposed structure performance metrics are evaluated and compared to the state-of-the-art. The integration of LG-W with gate-stack VTFET along with air pocket, namely SG-LG-VTFET with air pocket, reveals performance improvement via metrics such as device ON-current (I_{ON}), subthreshold swing (SS), transconductance (g_m) as well as transconductance generation efficiency (TGE). SG-LG-VTFET with air pocket generates SS of 13.92 mV/dec. Further, the device exhibits a higher I_{ON} ($3.6 \cdot 10^{-5}$ A/μm) with an I_{ON}/I_{OFF} ratio of 10^{12}. Due to the inclusion of the LG-W and air pocket, a narrow band-bending is observed, thus resulting in higher tunneling and steeper SS. A high-k stacked dielectric material enhances the capacitive coupling. The performance of the device is compared with the VTFET device in the absence of a dielectric pocket. The dielectric pocket increases the electric field, which is a desirable phenomenon for increasing the ON-current. For future applications, the scaling in SS is further possible that can increase the electron tunneling rate.

Keywords: Tunnel FET, Linearly-graded structure, Subthreshold swing (SS), Vertical TFET, Transconductance generation efficiency.

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1. INTRODUCTION

Tunnel field effect transistors (TFETs) have achieved a subthreshold swing (SS) value below the Boltzmann limit (i.e., 60 mV/dec), which is not achievable in conventional MOSFETs [1-3]. The transistor has shown potential in low-power VLSI applications due to its smaller I_{OFF} value [4]. The gate stacking and high-k gate oxide usage with SiO_2 with less EOT is a key metric to attain an improvement in the leakage and SS of short channel TFETs [5]. The semi-ideal switching metrics are attained via gate stacking TFETs. On contrary, in the miniaturization era, TFETs cannot be scaled down as in the nanometer region, the drain affects the device channel and consequently the gate control upon the channel gets lost [6]. Vertical TFETs (VTFETs) are preferred to replace TFETs because vertically developed topologies reduce TFETS scaling constraints [7]. Besides such scaling restrictions, a low value of I_{ON} is a drawback of TFETs due to reduced carrier tunneling [8]. Thus, to acquire a higher I_{ON} and steeper SS, different modified structures are utilized via the introduction of heterojunction engineering over the source-channel interface or by using work function engineering [9-11]. In order to enhance the TFET performance, both double and multi-gate methods are grown to another level, where instead of independent metals with a single work function, a binary metal alloy $a_\sigma b_{1-\sigma}$ with linearly graded work functions are considered to be gate electrodes [12]. For designing linearly graded work functions, a molar fraction 'σ' in a binary metal is changed from source to drain that metal 'A' shows a 100 % effect upon the source side, which reduces continuously via shifting towards the drain side. On the other hand, metal 'B' shows a 100 % effect upon the drain side that continuously reduces towards the source side. A linear change in the work function value reveals symmetric potential spread upon channel and performance enhancement with reduced short channel impacts [12]. The ZnCdSSe nanowire is effectively constructed by employing a continuous change in the molar fraction of constituted metals. With SS < 25 mV/dec, few advanced structures are designed that can meet the criteria of steepest SS with an improvement in performance with regards to linearly graded gate electrode art.

In the present work, an impact of a binary metal $a_\sigma b_{1-\sigma}$ (with σ as a continuous mole fraction change in metal A) is implemented over a VTFET device supplemented with a dielectric pocket in the channel region. The designed structure shows an improvement in performance at 13.92 mV/dec SS and $3.6 \cdot 10^{-5}$ A/μm I_{ON}, which is a novelty of the present work without any impact on the device OFF-current. Thus, it is preferred for advancing-powered circuits with an upgraded level of transistor switching. In addition, both oxides SiO_2 and HfO_2 and hafnium/zirconium alloy films are developed via phase vapor deposition (PVD) as well as chemical vapor deposition (CVD) process [13].

2. DEVICE GEOMETRY AND DESIGN SPECIFICATIONS

The improvement in device performance to acquire optimized results is done in terms of designing and simulating two VTFET structures.

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2.1 Gate Stacked Linearly Graded Metal Work Function VTFET with No Pocket (GS-LGW-VTFET No Pocket)

A gate stacked linearly graded work function SG-VTFET with dual gate electrodes (M1, M2) with 3 nm high-k gate oxides (HfO_2) inside the stack at 0.5 nm SiO_2 is constructed. The entire device is framed upon bulk silicon with the source on the downside and the drain on the upside.

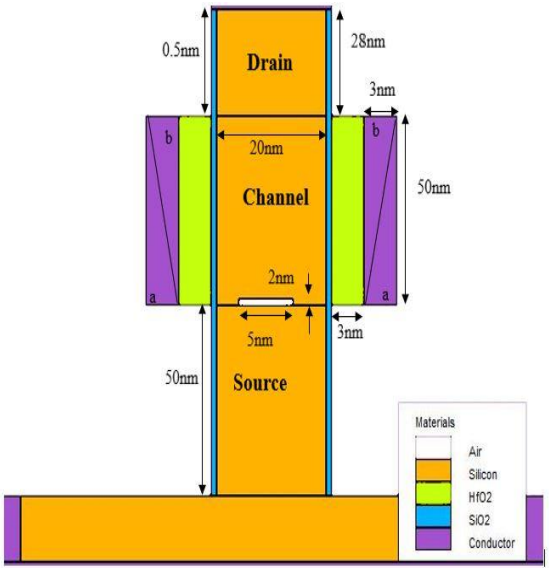


Fig. 1 – Gate stacked linearly graded binary metal electrode $a_\sigma b_{1-\sigma}$ device (GS-LGW-VTFET with air pocket) device schematics

2.2 Gate Stacked Linearly Graded Work Function Metal Electrode VTFET and Air Pocket (GS-LGW-VTFET with Air Pocket)

The device structure is implemented using a binary metal gate alloy ($a_\sigma b_{1-\sigma}$) electrode linearly graded work function with a dielectric pocket. It is a gate stacked linearly graded work function VTFET (SG-LGW-VTFET with air pocket) such that it varies unceasingly and linearly with 'σ' (mole division) metric of combined metals (A and B). This can be given as follows [14]:

$$\varphi(\sigma) = \sigma\varphi_B + (1-\sigma)\varphi_A + \sigma\left[\frac{(\varphi_B - \varphi_A)(\rho_B - \rho_A)}{\sigma\rho_B + (1-\sigma)\rho_B}\right], \quad (1)$$

where φ_A and φ_B are the work functions of metals A and B, while ρ_A and ρ_B are the densities of state found for metals A and B. With the unity value of the electronic specific heat ratio, the metric $\varphi(\sigma)$ of a metal alloy is further evaluated as [14]:

$$\varphi(\sigma) = \sigma\varphi_B + (1-\sigma)\varphi_A . \quad (2)$$

From (2), a composite metal alloy's work function linearly varies with the work function of A and B. The dual alloy work function linearly differs from low and high work functions. Metal alloys have shown better chemical and thermal stability using hafnium oxide. Work function variation in the range from 4.10 to 4.50 is implemented here. The work function is modulated from 4.10 to 4.50 via linear variation with mole division 'σ'. The binary compound metal alloys ($a_\sigma b_{1-\sigma}$) work function is linearly modulated at tunneling interface fully enforced and influenced via a, whereas 'b' has 100 % impact upon channel-drain interface as illustrated in Fig. 1. A number of researchers have already implemented a linearly graded work function in FETs. In addition, a dielectric pocket is incorporated into the device structure for better tunneling, higher ON current and transconductance.

Table 1 – Device design values and material specifications for simulation

Variables	Specifications
Gate length (Lch)/channel doping	50 nm/1 × 10^{16} cm^{-3} (p-type)
Source region (L_S)/concentration	50 nm/5 × 10^{20} cm^{-3} (p-type)
Drain region (L_D)/concentration	28 nm/1 × 10^{18} cm^{-3} (n-type)
HfO_2	3 nm
SiO_2 width	0.5 nm
Work function at 'A' to 'B' point	4.10 to 4.50 eV
Width of channel	20 nm
Pocket length	5 nm
Pocket width	2 nm

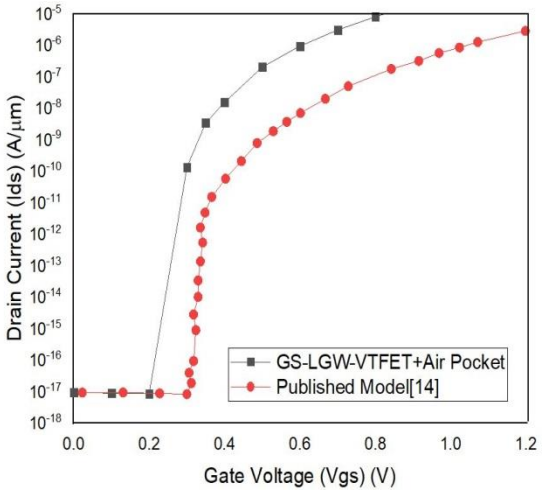


Fig. 2 – Calibration of the simulated device corresponding to the reported data available in [14]

Table 1 lists the device specification. To investigate and compare various performance metrics, the architecture is implemented and simulated using Silvaco 2D atlas device simulator [15]. Fig. 2 shows the comparison of the simulated device with the published model [14], where the $Si_{0.55}Ge_{0.45}$ pocket is used. The calibration is performed keeping the same physical and analytical models used in the reported results [14]. The calibrated I_D vs. V_{GS} results are plotted in Fig 2, which shows an improvement in drain current. The simulation is computed with different models, namely the non-local band to band (BTBT) model, Fermi architecture, Shockley-Read-Hall (SRH), concentration-dependent mobility architecture, bandgap narrowing topology, and CVT [16, 17]. For CVT, the transverse field, doping and temperature-dependent mobility part

are revealed through three components integrated via Matthiessen's rule [18]. The metrics are μ_{AC} (surface mobility lowered via scattering of acoustic phonons), μ_{sr} (surface roughness metric) and μ_b (mobility lowered via scattering with optical inter-valley phonons). The final equation will be:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}. \quad (3)$$

3. RESULTS AND DISCUSSION

The linearly graded and dielectric pocket impact upon the I_D-V_{GS} characteristic is compared with linearly graded work function VTFET structure, so that individual impact can be justified upon various performance metrics. Additionally, a variation in the valence and conduction bands, recombination level, electron and hole BTBT values, device electric field, transconductance g_m, as well as transconductance generation efficiency (TGE) of two structures (GS-LGW-VTFET no pocket and GS-LGW-VTFET with air pocket) are plotted and compared. The changes in the energy band diagram of two devices (GS-LGW-VTFET no pocket and GS-LGW-VTFET with air pocket) are illustrated in Fig. 3. It is noticeable from Fig. 3 that the tunneling region becomes narrower in the proposed GS-LGW-VTFET with air pocket device in comparison to the GS-LGW-VTFET no pocket device. This is because the air pocket causes more slope in band bending. Therefore, it creates a sudden tunneling regime in comparison to a gradual decrease in the tunneling region of the GS-LGW-VTFET no pocket.

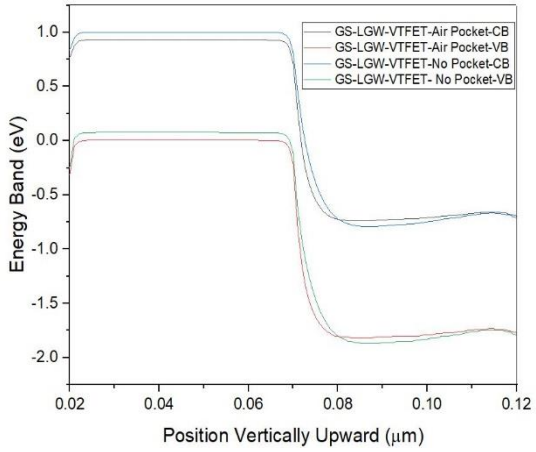


Fig. 3 – Energy band diagram variations of two structures (GS-LGW-VTFET with air pocket and GS-LGW-VTFET no pocket) in the ON-state (V_{GS} = V_{DS} = 1 V)

The I_D-V_{GS} characteristics of the device structures GS-LGW-VTFET no pocket and GS-LGW-VTFET with air pocket are compared. Fig. 4 compares the drive current of GS-LGW-VTFET no pocket and GS-LGW-VTFET with air pocket. It is visible from Fig. 4 that the I_{ON} current improves by 1 order. Also, GS-LGW-VTFET with air pocket shows a 13.92 mV/decade SS which is an improvement over GS-LGW-VTFET no pocket, having 18.75 mV/decade. The SS value and drive current improve with the combination of air pocket and binary metal work function, as observed in Fig. 5.

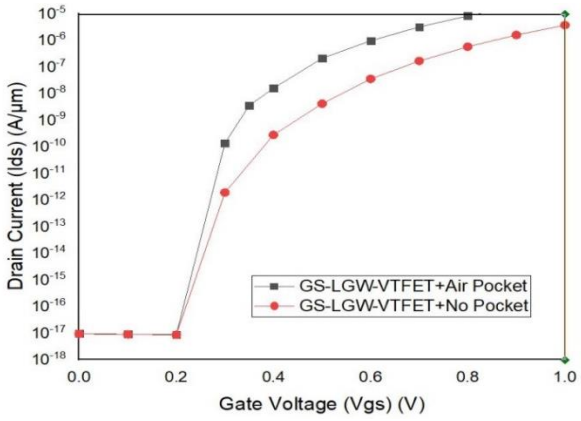


Fig. 4 – Comparison of I_D-V_{GS} characteristics of GS-LGW-VTFET with air pocket and GS-LGW-VTFET no pocket at V_{DS} = 1 V

The introduction of the air pocket improves the SS parameter by 25 %, while I_{ON} improves by 1 order. An improvement in SS, as well as I_{ON}, is observed as the air pocket raises the band-bending slope in addition to the narrowing of the bands. Thus, electron tunneling occurs over the source-channel interface which reduces abruptly beyond the interface to acquire a symmetric distribution in the surface potential. Therefore, GS-LGW-VTFET with air pocket implemented as a transistor shows the best performance with no effect on the I_{OFF}. For a better performance comparison, the metrics such as threshold voltage and SS of the proposed and simulated devices are summarized in a tabular form in Table 2. The threshold voltage (V_{th}) of TFETs is given by the minimum gate voltage such that the barrier width at the source channel intersection is too narrow such that electrons from the source valence band to the channel conduction band initiate tunneling. Also, it can be described as "an applied gate voltage over that narrowing of energy barriers saturates" [19]. The present work shows that the threshold voltage is computed as a gate voltage such that the output current becomes 10^{-7} A/μm.

In Fig. 4, by incorporating an air pocket along with linearly graded binary metal alloy, the device imparts a superior performance. Now it is noteworthy to illustrate that the I_{OFF} stays similar for all the designed structures. The threshold voltages are 0.47 V and 0.67 V for GS-LGW-VTFET with air pocket and GS-LGW-VTFET no pocket, respectively. The electron distribution in a vertically upward direction that is from down to up is illustrated in Fig. 5. The electron concentration for LG-VFET is found higher in Fig. 5 in comparison to GS-LGW-VTFET with air pocket from device source to channel. They reached a smaller peak in the channel vicinity (70 nm) because of the presence of an air pocket in the device. Table 2 compares the simulated parameters for two structures.

The band-to-band tunneling value changes for two devices (GS-LGW-VTFET with air pocket and GS-LGW-VTFET no pocket) located in the vertical direction are observed in Fig. 6. It is seen from Fig. 6a narrow electron tunneling for GS-LGW-VTFET with air pocket device and it is because of higher bending in energy bands that results in a higher tunneling rate. A narrow tunneling region reveals an accompanying slope

in bending energy bands. It causes a steeper SS. Fig. 6b reveals that the hole tunneling is very similar for two designed devices, thus hole tunneling effect is very similar in the determination of device performance metrics. Since the electron concentration increases due to the presence of an air pocket, the electric field is shown in Fig. 7.

$$\frac{1}{SS}=\frac{\Delta\log_{10} I_{DS}}{\Delta V_{GS}}=\frac{1}{\log(10)}\frac{\partial\log(I_{DS})}{\partial V_{GS}}=\frac{1}{\log(10)}\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial V_{GS}}, \quad (4)$$

$$\frac{1}{SS}=\frac{1}{\log(10)}\frac{1}{I_{DS}}g_m, \quad (5)$$

$$\frac{g_m}{I_{DS}}=\frac{\log(10)}{SS}. \quad (6)$$

Table 2 – Comparison of two VTFET structures

Device	GS-LGW-VTFET with air pocket	GS-LGW-VTFET no pocket
Threshold voltage (V)	0.47	0.67
SS (mv/dec)	13.92	18.75
OFF-current (A)	9.33×10^{-18}	9.13×10^{-18}
ON-current c(A)	3.62×10^{-5}	3.61×10^{-6}
I_{ON}/I_{OFF}	3.8777×10^{12}	3.95062×10^{11}

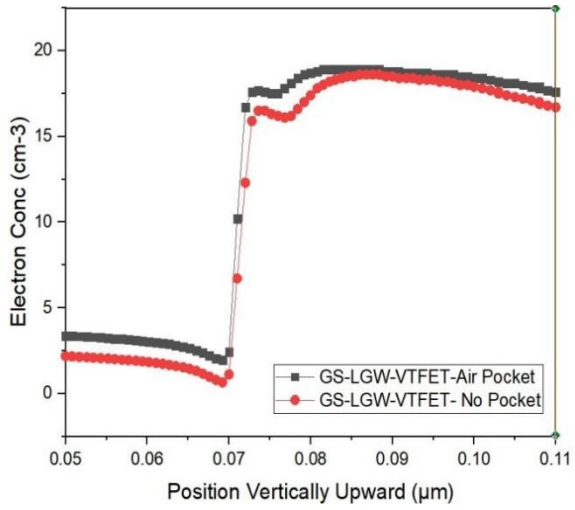
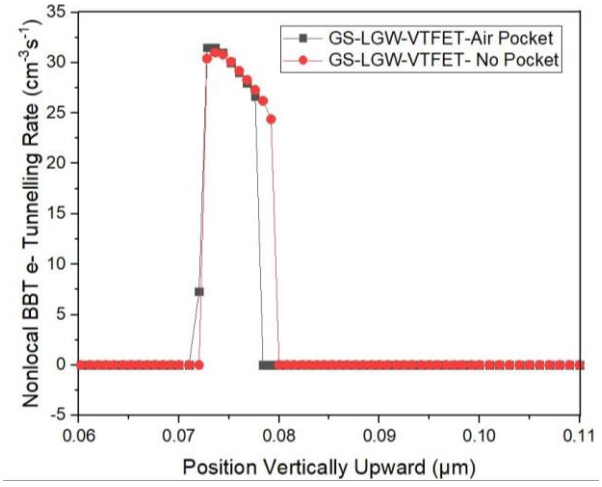
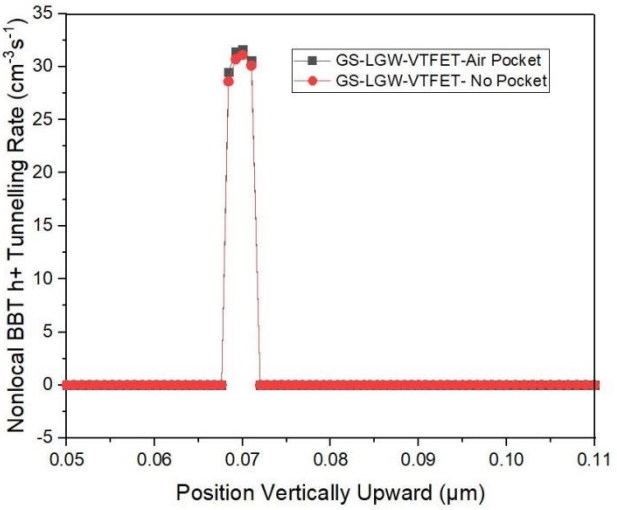


Fig. 5 – Charge carrier concentration distribution for electrons at V_{DS} = 1 V



a



b

Fig. 6 – BTBT: (a) electron tunneling, (b) hole tunneling rate variation of two structures (SG-VTFET and LG-VTFET) at V_{DS} = 1 V

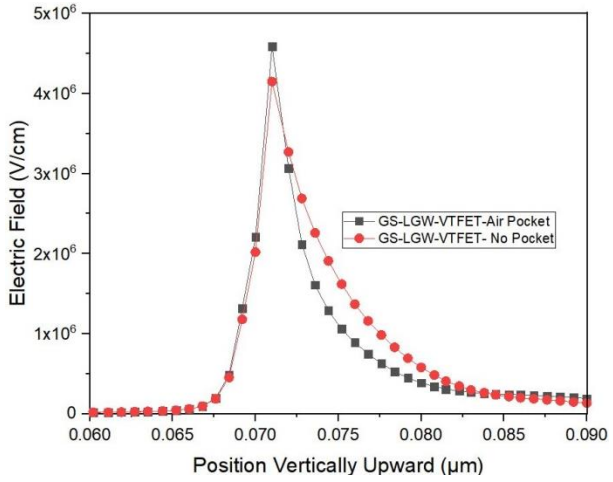
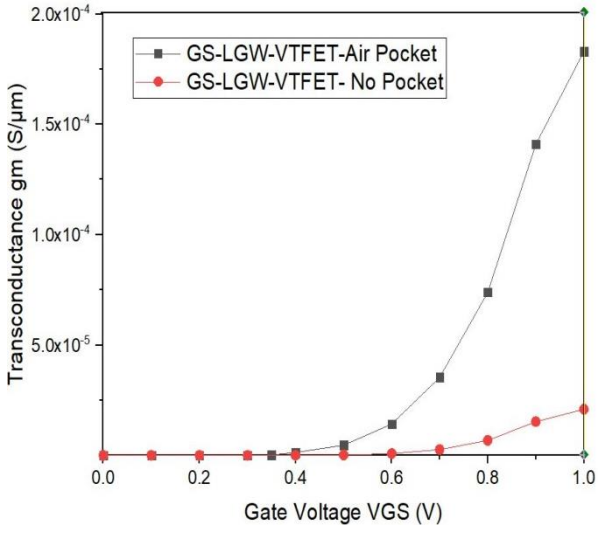


Fig. 7 – Electric field of two structures at V_{DS} = 1 V



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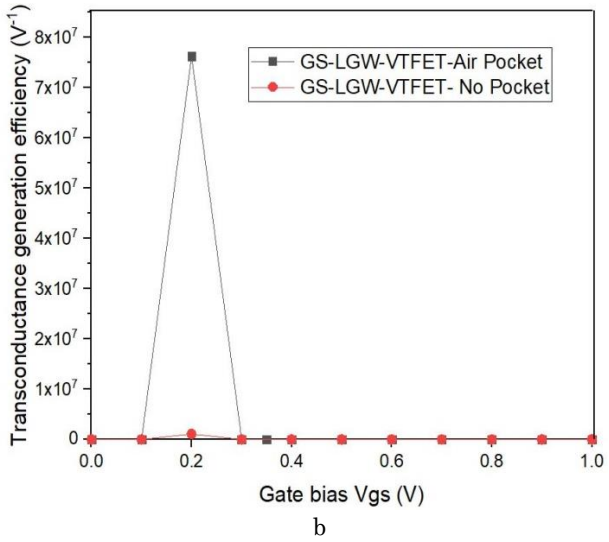

Fig. 8 – Improvement of (a) transconductance and (b) transconductance generation efficiency (TGE) at $V_{DS} = 1$ V

The dependence on SS is obvious from equations (4)-(6). Since GS-LGW-VTFET with air pocket has the lowest SS among the two topologies, it gives the highest transconductance and transconductance generation efficiency TGE = gm/ids, as illustrated in Fig. 8. It is further clear from Fig. 8b that at a lower bias of 0.2 V, the (TGE) is very high for GS-LGW-VTFET with air pocket. Thus, the simulated structure is suitable for low-power memory designs.

4. CONCLUSIONS

The present work explores the linearly graded dual metal electrode ($a_\sigma b_{1-\sigma}$) with air pocket over a linearly graded dual metal electrode in the absence of a pocket while structuring vertical TFETs. The optimum performance of the linearly graded work function with air pocket is compared with the linearly graded work function with no pocket, the simulated outcomes are compared and analyzed. The LG-VTFET with air pocket structure led to performance improvement by offering 13.92 mV/dec SS. The proposed structure sharps the incline of band twisting giving lower SS and higher transconductance. An improvement order of '1' is observed in I_{ON} and transconductance. Thus, the linearly graded proposed device has a good improvement in the transconductance value compared to SG-VTFET. Enhanced transconductance generation efficiency over reduced bias and better SS of LG-VTFET reflects the device's suitability for applications involving low-power circuits.

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Реалізація VTFET із лінійно градуйованою роботою виходу бінарного металевого затвору з повітряною кишенею

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У статті досліджено лінійно градуйовані характеристики роботи виходу (LG-W) за допомогою композиції затворного електрода із бінарного металевого сплаву $a_\sigma b_{1-\sigma}$ у стеку high-k затворів із діелектричною кишенею у вертикально орієнтованому FET (VTFET). Пристрій VTFET побудовано з використанням затворного електрода з бінарного металевого сплаву з лінійно градуйованою роботою виходу та повітряною кишенею. Пропоновані показники ефективності конструкції оцінюються та порівнюються з сучасними аналогами. Інтеграція LG-W з VTFET із стеком затворів разом із повітряною кишенею (SG-

LG-VTFET із повітряною кишенею) показує покращення продуктивності за допомогою таких показників, як струм увімкнення пристрою (I_{ON}), підпорогове коливання (SS), міжелектродна провідність (g_m), а також ефективність генерації міжелектродної провідності (TGE). SG-LG-VTFET з повітряною кишенею генерує SS, рівний 13,92 мВ/дек. Крім того пристрій демонструє вищий I_{ON} ($3{,}6 \cdot 10^{-5}$ А/мкм) із співвідношенням I_{ON}/I_{OFF}, що складає 10^{12}. Завдяки включенню LG-W і повітряної кишені спостерігається вузький вигин смуги, що призводить до більш високого тунелювання та крутішого SS. Багатошаровий high-k діелектричний матеріал підсилює ємнісний зв'язок. Продуктивність пристрою порівнюється з продуктивністю пристрою VTFET за відсутності діелектричної кишені. Діелектрична кишеня збільшує електричне поле, що є бажаним явищем для збільшення струму I_{ON}. Для майбутніх застосувань можливе масштабування SS, що може збільшити швидкість тунелювання електронів.

Ключові слова: Тунельний польовий транзистор (FET), Лінійно-градуйована структура, Підпорогове коливання (SS), Вертикальний TFET, Ефективність генерації міжелектродної провідності.