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Power and Threshold Voltage Analysis of 14 nm FinFET 12T SRAM Cell for Low Power Applications

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Embedded SRAM units are required components in today's SoCs. Due to the increased popularity of portable battery-powered devices, low-power IC design has become a focus in recent years. Traditional SRAM cell designs are both power-hungry and underperforming in this new era of speedy mobile computing. This research focuses on the power dissipation of 14 nm FinFET 12T SRAM read and write operations at various temperatures. The power dissipation of the suggested SRAM cell was calculated and compared to that of various existing technologies. A BSIM4 model with a short channel is offered as the proposed 14 nm FinFET 12T SRAM cell. The proposed 12T SRAM power dissipation was 7.430 μw for reading and 12.278 μw for writing operations at 45 °C. The recommended SRAM cell had a lower power dissipation. However, the threshold voltage was gradually reduced as the FinFET transistor was scaled down from 65 to 14 nm. For 14 nm FinFET simulations, the DSCH 3.8 and Microwind 3.8 tools were used.

Keywords: SRAM, FinFET, Power dissipation, BSIM4, Microwind.

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1. INTRODUCTION

In VLSI technologies, memory is divided into two types based on how information is stored: non-volatile and volatile memory. When data is stored in non-volatile memory, it remains accessible even if the power is turned off. When data is stored in volatile memory, and the power is turned off, the data is gone. Static and dynamic volatile memory are the two types of volatile memory. The frequency of their clocks can be used to classify static and dynamic volatile memory. The slowest clock rate is not required for static memory. Dynamic, on the other hand, necessitates the use of a periodic clock to refresh stored data. SRAM (Static Random Access Memory) is a type of high-speed computer memory used in electronics, microprocessors, and other computing applications. Static RAM is the sort of memory that keeps the data it receives without needing to rewrite it over and over. Due to the need for a battery, SRAM is employed for high-performance VLSI circuits in system-on-chip.

The performance of SRAM in terms of power and delay has been investigated by numerous researchers [1-4]. Y. Morita et al. proposed an 8T memory cell. It can be used instead of a 6T cell in a 45 nm process and later with substantial threshold-voltage fluctuation. The proposed voltage-control technique enhances the write margin and reads current, and the write-back scheme stabilizes unselected cells tested on 8T SRAM [5]. L. Zhiyu et al. proposed a new nine-transistor (9T) SRAM cell to decrease leakage power while improving data stability. During a read operation, the proposed 9T SRAM cell isolates the data from the bit lines. The read static noise margin of the recommended circuit is two times that of a standard six-transistor (6T) SRAM cell [6]. In [7], static noise margin improvement circuitry is offered, which symmetrizes the SRAM cell by altering the body bias of a pull-down NMOS transistor because the noise margin of SRAM cells decreases at low voltages. The 9T SRAM cell was chosen because it has less leakage and is more isolated. Noise margin should be read and held. C. Meng-Fan et al. [8] provided a 9T cell with a data-aware-feedback-cut off (DAFC) strategy to increase the writing margin and a dynamic-read-decoupled (DRD) scheme to prevent read-disturb from achieving deep subthreshold operation. For near-threshold and subthreshold applications, the cell area is 1.64 and 1.8 that of a standard 6T SRAM cell. Fabricated 90 nm 9T 32 kb macros show that the 9T macro can handle 130 mV VDD minimum. Compared to previously published SRAM designs, this work achieves the lowest VDD. A. Teman et al. presented a new 9T bit cell with a new supply feedback method for low voltage operation. During a write, the supply feedback SRAM decreases the bit cell's pull-up network, allowing the high data node to be released. At voltages as low as 250 mV, this method permits the cell to achieve dramatically enhanced write margins while being utterly functional under global and local process changes. Without the need for any additional circuits or methods, this low-voltage operation is completed. The functioning and stability of cells are discussed, and Monte Carlo (MC) statistical distributions demonstrate the notion [9]. In [10], SCMs are used to replace full-custom subsystems. SCMs have several advantages, including robust operation, minimized design effort for the same voltage range as the logic, high throughput, and reasonable energy efficiency for high-speed operation. Compared to entire solutions that operate at the same clock frequency, the cons include increased size and reduced energy efficiency. In [11], a novel 12T subthreshold SRAM cell with data-aware-power-cut-off write-assist is introduced to increase write-ability and avoid rising device fluctuations in deep sub-100 nm technologies at low supply voltage. The suggested 12T SRAM cell is demonstrated via a 4-kilobytes of memory SRAM macro built in 40 nm general-purpose (40 GP) CMOS technology. Vishal Sharma et al. [12] proposed a half-select free 12T SRAM cell that improves writing

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ability and read stability by employing data-dependent feedback cutting approach – designing and assessing the 6T SRAM cell at various technologies utilizing the predictive technology approach model to reduce power dissipation while maintaining stability. Then, in terms of power dissipation (both dynamic and static), latency, power delay product, and static noise margin, the performance of SRAM cells is compared [13]. In [14], a new energy-efficient 12T memory cell with radiation hardening by design that can tolerate single-event multiple-node upsets in the near-threshold voltage domain was presented. The radiation hardness of the proposed memory cell is increased by utilizing dummy access transistors to govern the PMOS devices of the cross-coupled inverters. R. Suresh Kumar et al. [15] presented a 12T SRAM architecture for reducing power leakages and consumption during the sleep transistor. This reduces the amount of leakage in the CMOS transistor. P. Sharma et al. proposed a Schmitt trigger-based 12T SRAM that can execute subthreshold write operations without any support circuitry [16].

This paper aims to design and analyze the 12T SRAM architecture using 14 nm FinFET technology. The following is how the paper is organized: section 2 shows the proposed 14 nm FinFET 12T SRAM architecture, and section 3 shows the software description. The results and discussion are analyzed in section 4, and section 5 summarizes the conclusions.

2. PROPOSED 14 NM FINFET 12T SRAM ARCHITECTURE

2.1 Structure of the 12T SRAM Cell

As illustrated in Fig. 1, the 12T SRAM circuit has twelve transistors (T1 to T12) and is divided into three sections: storage nodes (S, S'), read transistors (T11, T12), and write transistors (T5, T6, T7, T8, T9, T10).

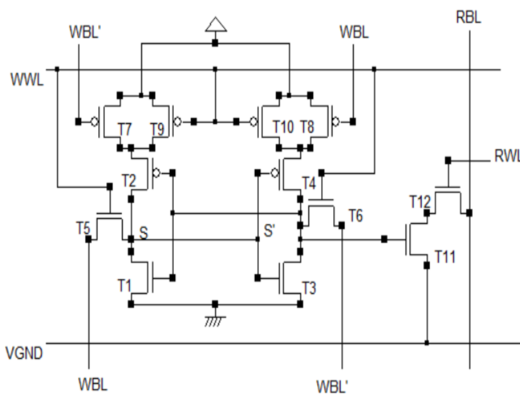

Fig. 1 – The proposed 12T SRAM

Two cross-coupled inverters are formed by four transistors (T1, T2, T3, T4) in the center, as shown in Fig. 2. If we give the first inverter a low input, it will output a high value on the second inverter, amplifying and storing the low value. Similarly, if the first inverter receives a high input value, the second inverter receives low input values and feeds the low input value back to the first inverter. The current logical value of these two inverters will be saved, regardless of how low or high the value is. During writing operations, access transistors T5 to T8 are employed. During data holding and cutting during write operations, T9 and T10 transmit power to inverters. T11, like in a standard eight transistor SRAM cell, decouples the storage node S' from the read bit line, while T12 acts as an access transistor during reading operations.

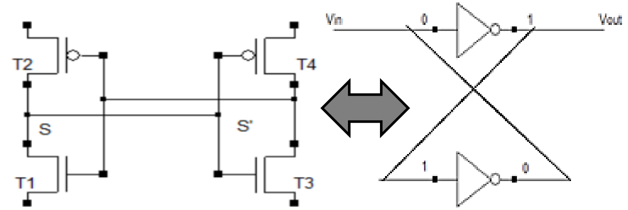

Fig. 2 – Cross-coupled inverters

2.2 Operation of 12T SRAM Cell

SRAM has two operations, namely read and write. The read operation can read the values stored using the write operation. During read and write operations, the 12T SRAM is entirely static.

2.2.1 Write Operation

T5 through T10, a total of six devices, are covered by the write operation. If zero is first saved at node S and one is initially saved at node S', the write operation comprises writing one to node S, maintaining a value of zero at the negative write bit line, while asserting a value of one at the write bit line to turn on T7 and turn off T8. T5 and T6 are activated, whereas T9 and T10 are deactivated when the write word line is asserted. Because a path from the supply to node S' has been cut, the current cannot flow into the storage nodes. Instead, a path is built from node S' to the ground. T5 makes a connection between supply and node S, on the other hand. As a result, T6 is discharged from node S', while T5 is charged from node S. Please be aware that there is a charge discrepancy between T1 and T5. Because of T6's higher gate to source voltage and lack of charge congestion in the discharge channel, writing zero at node S' would finish before writing one at node S. After discharging the node S,' the initial charge dispute between T1 and T5 would be resolved. In other words, this operation turns on T2 while turning off T1, resulting in a transparent connection from supply to node S through T7 and T2 but a closed path to the ground. As a result, T3 becomes transparent while T4 is switched off, and charging node S is helped. Writing one to node S and zero to node S' is now complete. As a result, all asserted signals on the write word line, write bit line, and negative write bit line should be reset to zero. T7 through T10 can now send power to the cross-coupled inverters as a result of this reset, however T5 and T6 are turned off.

2.2.1 Read Operation

To conduct read operations, devices T11 and T12 are used. Device T11, like a standard eight transistor SRAM cell, decouples the storage node S' from the read

bit line. T11 is triggered in this situation. A channel from the read bit line to the virtual ground becomes transparent when the read word line is asserted, and the virtual ground is driven to ground by a driver. Charges on the read bit line begin to discharge through the channel once it is transparent. The read operation comes to a close with this phase. When the SRAM cells attached to this word line are not in use, the read word line is de-asserted, the read bit line is precharged to supply voltage, and the virtual ground is driven to supply voltage. Leakage is reduced since there is no voltage difference between the read bit line and virtual ground. Additional rows of cells are shared in bit lines since leaking has been a stumbling barrier in increasing the number of cells.

3. SOFTWARE DESCRIPTION

3.1 Digital Schematic (DSCH)

DSCH (digital schematic) is a logic editor and simulator in one package. Before starting the microelectronics design, DSCH is used to verify the logic circuit's architecture. DSCH makes it feasible to develop and assess complicated logic structures by providing a user-friendly environment for hierarchical logic design and quick simulation with delay analysis. For the 8051 and PIC16F84 controllers, DSCH additionally provides symbols, models, and assembly instructions. Designers can use DSCH to construct logic circuits and test software applications that connect to these controllers.

3.2 Microwind

Microwind is a one-of-a-kind educational tool for nano CMOS cell creation. Microwind can be configured in various technologies ranging from 1.2 micrometers to 3 nm. Microwind depicts 2D and 3D characteristics of integrated circuits. Microwind uses an embedded simulator to simulate cells and blocks. Microwind employs levels 1, 3, and a simplified form of Berkeley short-channel IGFET model 4 (BSIM4) developed for use with FinFET (Fin Field-Effect Transistor) nanosheet. FinFET models often contain 500 parameters per transistor and over 20,000 lines of C code. Microwind uses Lambda units to operate. Only about 100 basic design rules are checked by Microwind DRC (Design Rule Checker). More than 2500 design rules have been listed in the design kit for 14 nm technology. It is impossible to manufacture a layout without a complete DRC. Starting with the 14 nm node, FinFET is employed. The layout, size, and performance are based on a "typical" 14 nm FinFET. FinFETs use fins instead of a continuous channel, allowing them to be low-power, quick, small, and scalable. FinFETs are tiny transistors that provide the same Ion current. FinFETs have a minor leakage current I_{off}, while maintaining the same I_{on}.

4. RESULTS AND DISCUSSION

Creating a device with several ports could be beneficial in registering files using multi-ported SRAM circuits. The density of the twelve-transistor SRAM comes at the cost of manufacturing complexity. We discovered that 12T SRAM requires less power to operate and occupies a tiny space. The outcome of this proposed structure has been achieved in less time to finish the operation. Static RAM is utilized in a variety of industrial and scientific subsystems. With the help of the Microwind tool and the BSIM4 model, schematic simulations at 14 nm FinFET technology were performed.

4.1 Layout Design

Fig. 3 depicts the proposed 14 nm FinFET 12T SRAM cell's layout design. Microwind generates the layout from a Verilog file created with the DSCH tool. The suggested SRAM cell requires more area than other existing SRAM cells (6T, 8T, 9T, 11T), but the reduced power and greater stability of the proposed 14 nm FinFET 12T SRAM easily exceed this deficit.

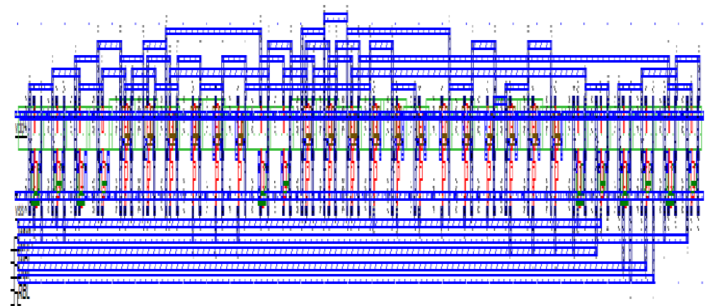

Fig. 3 – Layout design of the proposed 12T SRAM cell

4.2 Power Dissipation Analysis

This section calculates the power dissipation for independent read and write operations of 14 nm FinFET 12T SRAM at various temperatures and compares the results to existing technology. Compared to other existing technologies, the power dissipation of 14 nm FinFET 12T SRAM is quite low.

4.2.1 Power Dissipation Analysis of 12T SRAM Cell for the Read Operation

Table 1 compares power dissipation for the read operation of the proposed 14 nm FinFET 12T SRAM cell at various temperatures and existing technologies.

The power dissipation varies based on temperature as technology improves. At a lower temperature of 5 °C, power dissipation in 65 nm technology is 11.996 μW, whereas power dissipation in 14 nm technology is 7.416 μW. At a higher temperature of 45 °C, power

Table 1 – Comparison of power dissipation at different temperatures for the read operation

Temperature (°C)	Power dissipation of 12T SRAM (μW)			
	65 nm	45 nm	32 nm	Proposed 14 nm
5	11.996	12.281	12.164	7.416
15	12.025	12.296	12.176	7.419
20	12.040	12.304	12.181	7.421
27	12.061	12.314	12.189	7.423
35	12.086	12.327	12.198	7.426
42	12.107	12.338	12.206	7.429
45	12.116	12.342	12.210	7.430

dissipation in 65 nm technology is 12.116 μW, while power dissipation in 14 nm technology is 7.430 μW. As a result, it can be concluded that by reducing technology, power dissipation is likewise reduced. Fig. 4 shows an analog simulation schematic for a read operation.

4.2.2 Power Dissipation Analysis of 12T SRAM Cell for the Write Operation

Table 2 compares the power dissipation for the write operation of the proposed 14 nm FinFET 12T SRAM cell at various temperatures and existing technologies.

Table 2 – Comparison of power dissipation at different temperatures for a write operation

Temperature (°C)	Power dissipation of 12T SRAM (μW)			
	65 nm	45 nm	32 nm	Proposed 14 nm
5	16.430	17.587	20.871	10.929
15	16.581	17.743	21.020	11.025
20	16.940	18.111	21.369	11.251
27	17.357	18.539	21.768	11.516
35	17.350	18.922	22.117	11.753
42	18.00	19.199	22.365	11.925
45	18.552	19.762	22.856	12.278

The power dissipation varies based on temperature as technology improves. At a lower temperature of 5 °C, power dissipation in 65 nm technology is 16.430 μW, whereas power dissipation in 14 nm technology is 10.929 μW. At a higher temperature of 45 °C, power dissipation in 65 nm technology is 18.552 μW, while power dissipation in 14 nm technology is 12.278 μW. As a result, it can be concluded that by reducing technology, power dissipation is likewise reduced. The proposed cell uses less power for read and write activities than existing technologies. Fig. 5 shows an analog simulation schematic for a read operation.

4.3 THRESHOLD VOLTAGE ANALYSIS

Table 3 shows the values of threshold voltage (V_{TH}), ON current (I_{ON}), OFF current (I_{OFF}), and effective current (I_{EFF}) for FinFET transistor with various technology nodes at 27 °C temperature. It has been inferred from Table 3 that as the FinFET transistor is scaled down from 65 to 14 nm, the threshold voltage gradually decreases. For 14 nm FinFET transistor used in this paper, the ON current is found as 0.099, the OFF current is found as 2.207 and the efficient current is found as 0.051. Fig. 6 and Fig. 7 show the I_{ds}-V_{ds} characteristics of n-channel and p-channel FinFETs for various V_{gs}. It is inferred from the figure that V_{ds} increases with I_{ds}.

Table 3 – Values of V_{TH}, I_{ON}, I_{OFF}, and I_{EFF}

Parameters	Technologies			
	65 nm	45 nm	32 nm	Proposed 14 nm
V_{TH}	0.330	0.290	0.250	0.200
I_{ON} (mA)	0.012	0.001	0.002	0.099
I_{OFF} (nA)	0.002	0.0004	0.051	2.207
I_{EFF} (mA)	0.006	0.001	0.001	0.051

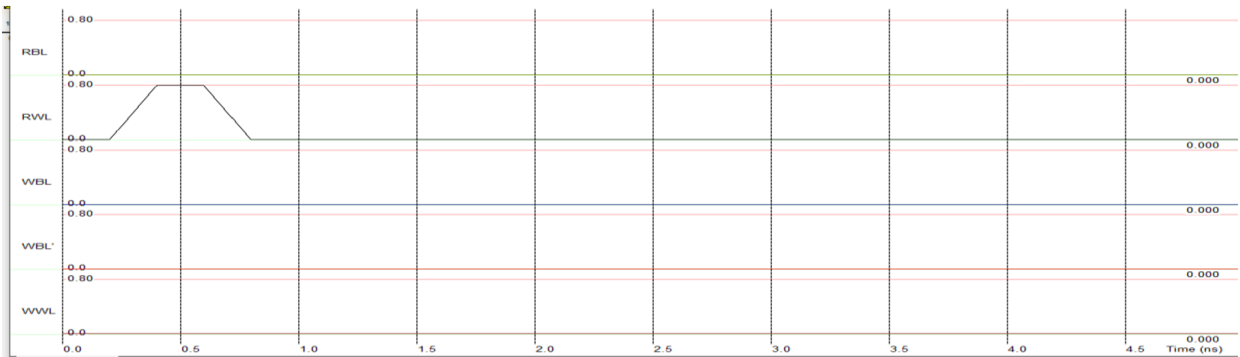

Fig. 4 – Analog simulation schematic of the proposed 14 nm FinFET 12T SRAM for the read operation

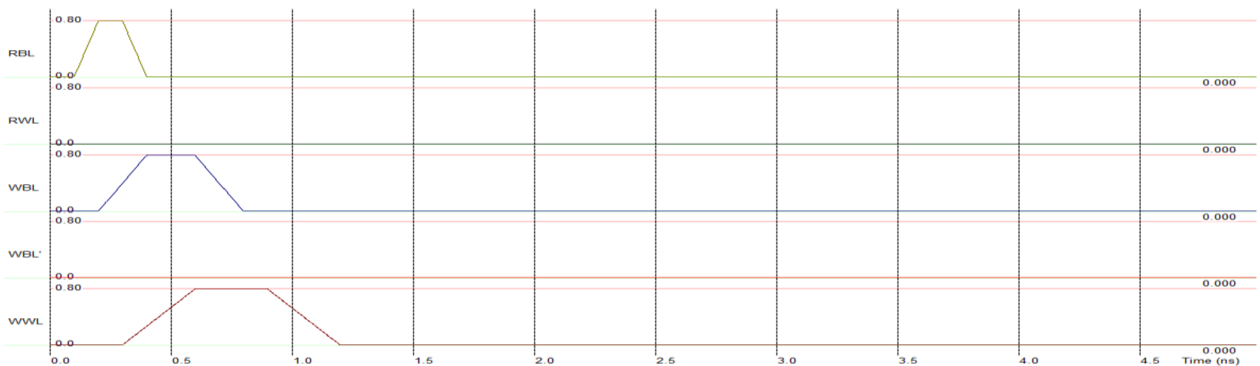

Fig. 5 – Analog simulation schematic of the proposed 14 nm FinFET 12T SRAM for the write operation

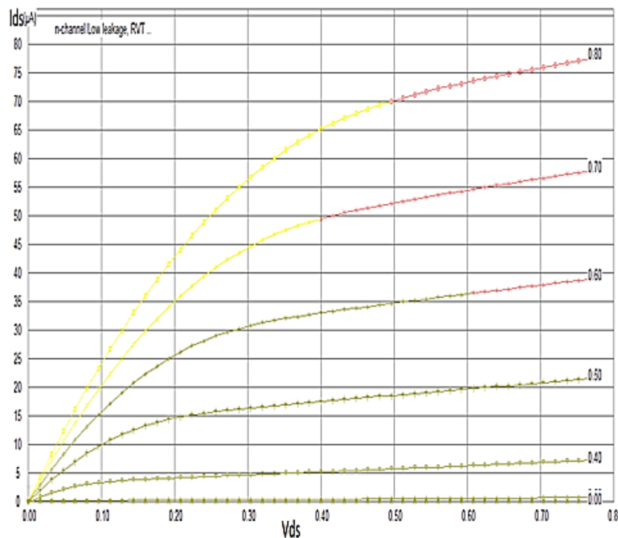

Fig. 6 – *Vds* vs *Ids* for *n*-channel

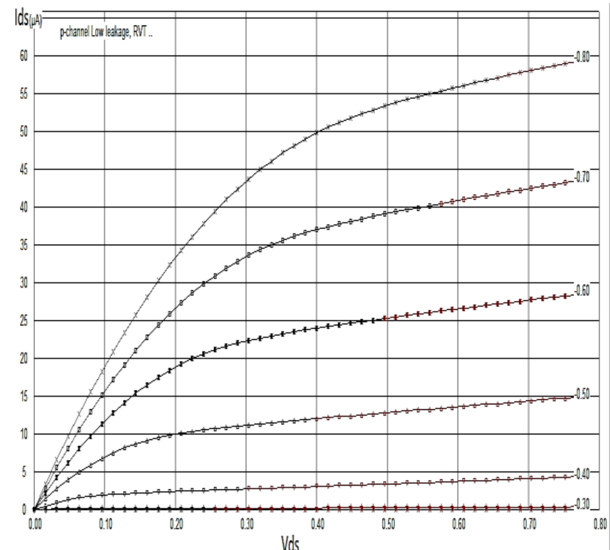

Fig. 7 – *Vds* vs *Ids* for *p*-channel

5. CONCLUSIONS

In the design of CMOS VLSI, low power consumption is crucial. The proposed low-power 14 nm FinFET 12T SRAM dissipates less dynamic power than existing technologies. Compared to standard 6T and 11T SRAM cells, the suggested cell (12T) is more stable. According to the simulation, the proposed cell dissipates less power at different temperatures and has higher stability than other existing SRAM cells. Despite the higher transistor count and size than other SRAM cells, the lower power dissipation and enhanced stability easily exceed this deficit. Although the FinFET transistor is scaled down from 65 to 14 nm, the threshold voltage gradually decreases. This proposed 14 nm FinFET 12T SRAM cell can be employed in high-speed devices like laptops, smartphones, and programmable logic devices to provide a low-power solution.

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Аналіз потужності та порогової напруги 12T SRAM комірки 14 нм FinFET для додатків із низьким енергоспоживанням

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Вбудовані модулі SRAM є обов'язковими компонентами сучасних SoCs. У зв'язку зі збільшенням популярності портативних пристроїв із живленням від акумуляторів останнім часом багато уваги приділяється конструкціям мікросхем із низьким енергоспоживанням. Традиційні конструкції комірок SRAM є водночас енергоємними та неефективними в цю нову еру швидкісних мобільних обчислень. Дане дослідження зосереджено на розсіюванні потужності операцій читання та запису 12T SRAM комірки 14 нм FinFET при різних температурах. Розсіювання потужності запропонованої SRAM комірки було розраховано та порівняно з розсіюванням різних існуючих технологій. Модель BSIM4 із коротким каналом пропонується як 12T SRAM комірка 14 нм FinFET. Розсіювана потужність запропонованої 12T SRAM комірки становила 7,430 мкВт для читання та 12,278 мкВт для запису при температурі 45 °C. Рекомендована SRAM комірка мала нижчу розсіювану потужність. Однак порогова напруга поступово знижувалася, оскільки розмір FinFET було зменшено з 65 до 14 нм. Для моделювання 14 нм FinFET використовувалися інструменти DSCH 3.8 і Microwind 3.8.

Ключові слова: SRAM, FinFET, Розсіювання потужності, BSIM4, Microwind.