JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. **14** No 3, 03006(5pp) (2022)

ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том **14** № 3, 03006(5cc) (2022)

Low Noise Amplifier Design with Current Reuse Architecture and Pre-distortion Technique for Nanoelectronic Sensors Operating at 2.4 GHz

K. Suganthi[1], B. Venila[2], M.S. Abirami[3], Ritam Dutta[4,*]

[1] *Department of ECE, SRMIST, Chennai 603203 Tamil Nadu, India*
[2] *Department of Mathematics, SRMIST, Chennai 603203 Tamil Nadu, India*
[3] *Department of Computational Intelligence, SRMIST, Chennai 603203 Tamil Nadu, India*
[4] *CISR – ITER, Siksha 'O' Anusandhan University, Bhubaneswar 751030 Odisha, India*

(Received 24 May 2022; revised manuscript received 22 June 2022; published online 30 June 2022)

This paper describes the development of different CMOS Low Noise Amplifier (LNA) topologies for achieving high linearity and low noise for nanosensor designs. The frequency of operation is 2.4 GHz, the ISM band is suitable for nanosensor applications. The novelty is introduced with a reconfigurable structure with the current reuse architecture for low power consumption, and pre-distortion technique is utilized to achieve good linearity without distortions, which is a preferrable metric for amplifier design. Nanoscale designs are achieved with an increase in robustness. The proposed CMOS based LNA design has moderate gain with a low noise figure of 2.6 dB at 2.4 GHz and less than 2 dB at 5 GHz. Good reverse isolation is achieved by the Voltage Standing Wave Ratio (VSWR), and the optimized *S* parameter input and output reflection coefficients are less than – 10 dB. The stability of the designed amplifier and the power gain results are compatible with the nanosensor design. The novelty achieved in the design is the wide bandwidth, good Figure of Merit (FOM), small size, moderate gain without distortions, low noise and good linearity due to complex design. Also, the power gain is moderate, and the layout of the design occupies a small chip area of 0.5×0.2 mm².

Keywords: CMOS design, LNA, Nanoamplifier, Circuit design, Nanosensing nanomaterials.

DOI: 10.21272/jnep.14(3).03006 PACS numbers: 85.35. – p

1. INTRODUCTION

The high performance of highly integrated Low Noise Amplifier (LNA) with inductor less design [1] results in solution of low cost with reduced area. It is suitable for Wireless LAN applications at fixed higher frequency of operation. The integrated transceivers design of LNA operating at particular frequency of 5-GHz with higher speed of transmission in Wireless Local Area Network (WLAN) [2] standards to address the receiver section with low components of noise and low power with good quality in communication.

A transceiver design of LNA includes LNA with receiver stage. In RF circuits, Amplifiers play a vital role with low noise, which result in high performance of overall design. The several performance parameters of LNA are specified and measured as follows: good matching at input and output, high gain, low power and Noise Factor (NF), high linearity. In transceiver system, LNA is the main block of the overall design, and it is figured in Fig. 1, and this is employed after the antenna so that this LNA amplifies those RF input signals from the antenna and so that the distortions are minimized by this amplifier.

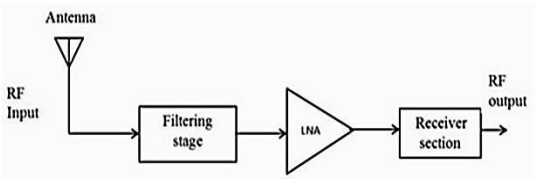

Fig. 1 – Low noise amplifier with receiver section

LNA is solution of front end in receiver section that reduces the presence of noise that is unwanted in the circuit with improved performance. In this LNA is placed following the stage of antenna is used in which the Signal to Noise Ratio (SNR) is adjusted [3]. The various performance parameters of the overall integrated design results in high performance with high operating range of frequency. The band of 5 GHz is less crowded with continued connection and faster speed in transmission of data. IEEE802.11a standard use high frequency of 5-GHz prevent the interference of signals from different applications. Thus, 5 GHz band of frequency is used for WLAN application with excellent performance of device. Power dissipation is typically higher for silicon based MOSFET devices compared to gallium arsenide FET based devices, [4] which will be operating in the tera- and millihertz regime.

By adopting the technique of current reuse, the high gain is obtained with efficient power consumption in the overall design. The amplification stage with Shunt Feed Back (SFB) feedback principle is mainly used to achieve good input matching and low power is obtained with lower supply voltage in the design of inductor-less LNA. But once the amplification stage of current re-use with feedback stage introduces the non-linear distortion in the design with increased noise. The linearization circuit is employed at the front end of the LNA to avoid the degradation of linearity in the design of LNA and cancel the inter-modulation distortion in circuit input matching with high linearity [5]. The linearity is improved so that overall efficiency of power can be obtained by employing this pre-distortion technique.

* ritamdutta1986@gmail.com
The results were presented at the 2nd International Conference on Innovative Research in Renewable Energy Technologies (IRRET-2022)

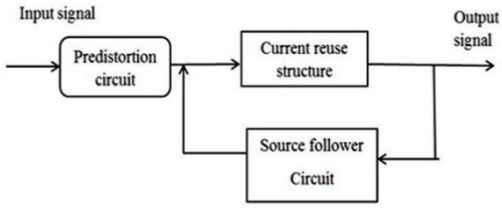

Fig. 2 – Two stage configuration with pre-distortion

Souza presents an inductor-less design is a two stage of current reuse structure followed by active feedback. First stage of current reuse is used to obtain high gain and it consumes low power. The second stage of active feedback is employed in the design, so that good matching is obtained at the input of LNA. The principle that is adopted is superposition of complementary derivative at 2.4 GHz frequency. Low area is obtained across wide frequency bands and that support applications of wireless communications. It occupies less area by designing the circuit in 130 nm CMOS [6].

Mahdi proposes a design includes complementary structure of current reuse and this characteristic feature reduce the distortions with improved efficiency of power. The good input matching is obtained by the shunt feedback with low power at reduced supply voltage by this inductor-less design, uses 130 nm CMOS technology [7].

The other work includes a design of common source gate with feedback topology of shunt. The structure of push pull cross coupled LNA is used, so that low power is consumed with enhancement in G_m and noise is cancelled partially. By following these techniques, overall performance of LNA design is improved. The technique of G_m boosting is applied to reduce the overall power consumption with high performance of the LNA design and technology of CMOS is employed in all these works [5, 6].

A linearization process, pre-distortion technique with LNA design at a particular frequency of 5 GHz for WLAN applications with linearity improvement and low consumption. This proposed design reduces the noise and allow high quality information at the output stage of the design [8]. This design adopts a CMOS technology of 90 nm with reduced area and most beneficial solution of low cost with inductor less design.

The LNA operation at 2.4 GHz and 5.2 GHz reveals WLAN application. The LNA operation at 28 GHz and 35 GHz reveals millimeter wave application. The designed LNA is simulated using EDA Cadence tool using 90 nm CMOS Technology.

2. EXPERIMENTAL METHODS EMPLOYED FOR NANOELECTRONIC DESIGN

Distortion in the design is mainly due to the nonlinear characteristics of trans-conductance and it leads to degraded linearity in the LNA design. It operates at the frequency of 2.4 GHz and 5.2 GHz band with high power consumption due to nonlinearity of the design with high NF which reduces the gain of the LNA design. These 2.4 GHz, 5 GHz and 5.2 GHz bands are suited for wireless communications. The feedback with derivative superposition principle provides higher trans conductance with high gain. The multi-stage design of LNA results in area efficiency with high gain and extended bandwidth.

The pre-distortion linearization employed in the LNA design to achieve high linearity and power efficiency simultaneously. The insertion of this linearization circuit in this design will not occupy more space for this type of amplifiers that are integrated. The two types of distortion are pre-distortion and post distortion at the input as well as output. The linearization requirements of this pre-distortion are so modest and result in efficient gain in the design of this LNA with high linearity [9].

In LNA, there is compensation in the non-linearity that is acquired by this pre-distortion technique. The signal distortions in the design of LNA and frequency interference is minimized by this pre-distorter circuit and this pre-distorter at the input also allows the transmission capacity rate that is higher so that it play a main role in the application of WLAN standards with high speed [10]. Linearization of LNA is most demanding technique compared to signaling of base-band devices. The various techniques of linearizing the LNA are compared with their efficiency band of operation and other parameters of linearization and are tabulated in Table 1.

Table 1 – Linearization technique summary

Linearization technique	Distortion cancellation	Wide band	Efficiency	Size
Feed Forward	High	Yes	Low	Large
Complementary	Low	Yes	Medium	Medium
Modified	Medium	Yes	Medium	Moderate
Predistortion	**High**	**Yes**	**High**	**Small**

Pre-distortion linearizer shows good performance and efficient to employ in LNA linearization to achieve high linearity with avoidance of interference. Pre-distortion linearizer satisfy all the LNA design parameters, and it operate at high frequency band with speed in trans-mission of signals.

The first stage of LNA, has stacked transistors of NMOS and PMOS with bias resistor R_{bias} as shown in Fig. 4.

The cancellation of distortion is completely achieved by the pre-distortion circuit design with the significance of high linearity and good power efficiency. The designed pre-distortion circuit is operated at a particular frequency of 5 GHz, and it is beneficial for WLAN applications [11].

An amplifier design includes many trades-offs between the performance parameters of gain, NF, linearity etc. Electrical properties are very well enhanced with respect to the Rogers and duroid material properties which are used in this design with a good aspect ratio of the device emphasized. Thermal properties are very well understood with the conductivity property of silicon-based CMOS devices. Also, the layout of the design is shown in subsection 4.2 in the following Fig. 8 with the discussion and illustration of the material properties of the design employed, for the novelty of reconfigurability.

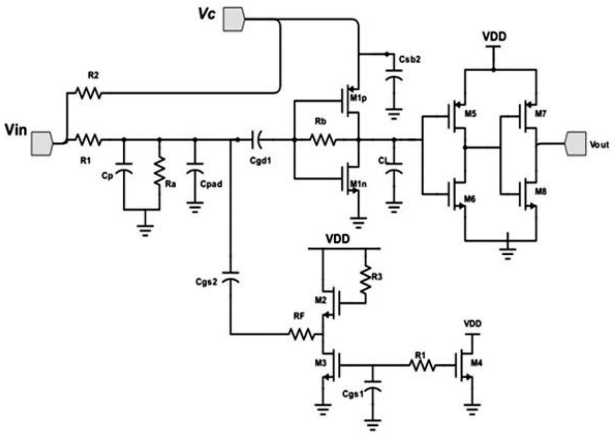

Fig. 3 – Design of LNA with pre-distortion stage

Table 2 – Material characteristics

Dielectric material	Frequency, GHz	Return loss and impedance	Gain and efficiency
Rogers	2-10 GHz	– 22 dB, 55 Ω	> 10 dB, 87 %
RT-duroid	5-10 GHz	– 12 dB, 50 Ω	> 10 dB, 84 %

3. DEISGN ANALYSIS AND IMPLEMENTATION

3.1 Voltage gain

The overall voltage gain of pre-distortion Low Noise Amplifier is expressed in equation (3). From the equivalent structure of pre-distortion includes R_1, R_a, R_2 and C_{gs3}. So that the from circuit it is described as Ra is parallel with capacitor Cgs_3 and this is series with R_1 and R_2. The voltage gain of the pre-distortion structure is given as:

$$Av = \left[\mathrm{Ra}||\frac{1}{SC_{gs3}}\right] + (R1||R2), \tag{1}$$

$$Av = Ax.Ay, \tag{2}$$

$$v = |-(Gm - Rf)R0(gm1 + SCgd1)(Gs + SCs)/(s2[(Cs + Cgd1)(C0 + Cgd1)] + S[(Cs + Cgs1)(G0 + gm1)) + G0Cgd1 + (C0 + Cgd1)Gs + Gs(G0 + gm1) + |(\mathrm{Ra}||1/SC_{gs3}) + (R1||R2))| \tag{3}$$

3.2 Input Matching

Noise is cancelled and controlled by the pre-distortion circuit, whereas noise is introduced by the feedback resistor. Input impedance of the designed circuit is expressed by equation (9):

$$Z_{in3} = Z_{in1} \,||\, Z_{in2}\,, \tag{4}$$

$$Z_{in3} = (Rf(gm1 + S(Cgs2 + CL) + G0)) / (Rf[S2(Cgs2Cgd1) + (Cgd1CL) + Cgs2CL] + S[(G0 + Cgd1gm1 + Cgs2G0)(G0 + gm1)]) + (1 + Av[gm1 + s(Cgs2 + CL) + G0] \tag{5}$$

3.3 Noise Figure

The noise figure of circuit includes source resistor with feedback resistor is expressed in equation (6):

$$\mathrm{NF} = 1 + \frac{Ra}{Rs.Av2} + \frac{Rs}{R1}\left[1 - \frac{Ra}{Rs.Av}\right]^2 + \frac{Rs}{R2}\left[1 - \frac{Ra}{Rs.Av}\right]^2. \tag{6}$$

3.4 Figure of Merit

The overall performance parameter of the LNA design is evaluated with Figure of Merit (FOM) parameter. The parameter with excellent efficiency is expressed by equations (7) and (8):

$$FOM_1 = \frac{Gain(dB)}{Power(mW)}, \tag{7}$$

$$FOM_2 = 20\log\left(\frac{Gain.Freq.IIP3(dB)}{(NFmin-1).PDC}\right). \tag{8}$$

4. PERFORMANCE ANALYSIS OF THE PROPOSED DESIGN

4.1 Amplifier Operating at 2.4 GHz (LNA1)

The schematic design includes two stage of current reuse structure and feedback integrated with inductor less design [5, 9]. The existing design of LNA allow medium bandwidth and the integrated solution of two stage develop distortions in design and result in degraded linearity. This degrades the performance of LNA with high noise and power consumed is also high in the circuit design.

Power gain. From Fig. 5, it is observed as power gain at 2.4 GHz is 9.49 dB with less matching of impedance in existing design and 13.09 dB at 5 GHZ and it has low forward gain. The reflection coefficient at output of design is observed as – 4.47 dB with high loss in LNA at 2.4 GHz and 0.41 dB loss at 5 GHz.

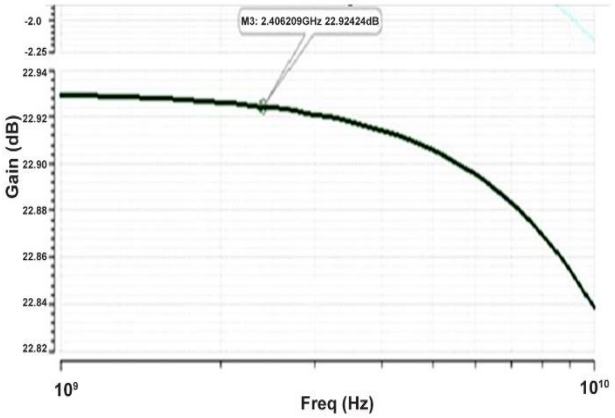

Fig. 4 – Gain of LNA1

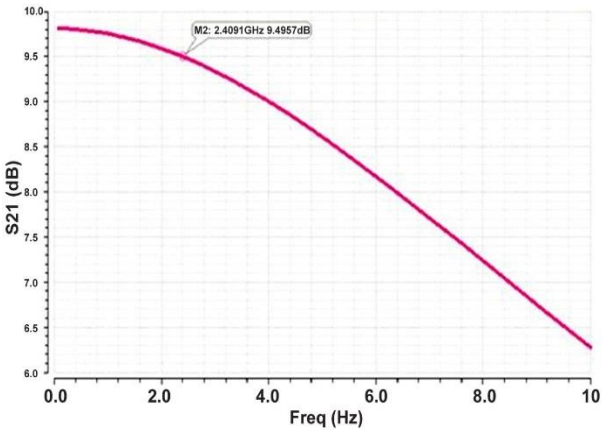

Fig. 5 – Power gain 2.5 GHz with pre-distorter

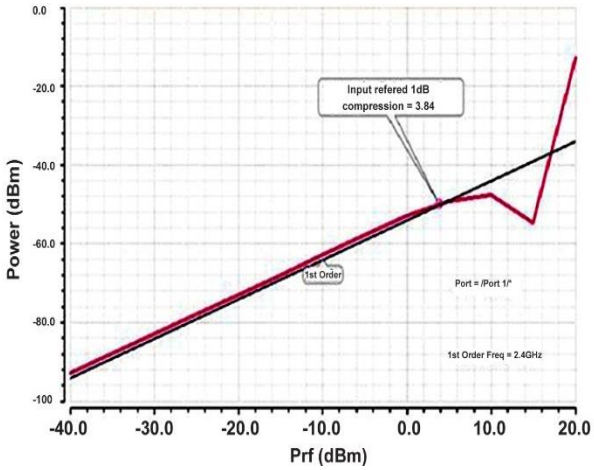

Fig. 6 – Compression points for 2.4 GHz

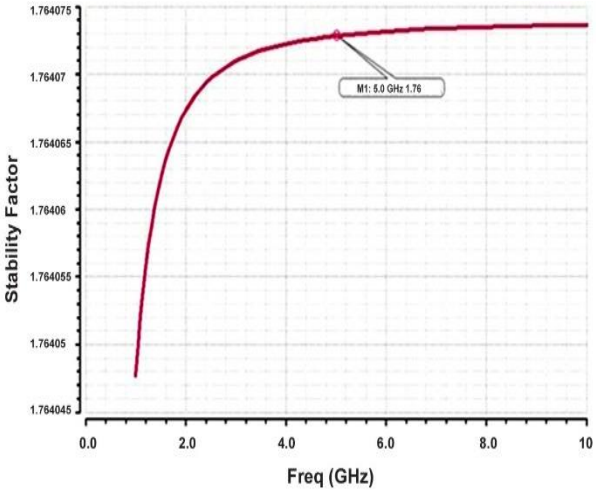

Fig. 7 – Stability factor

Table 3 – Material characteristics

Parameters	Ref. [10]	Ref. [11]	Ref. [12]	Proposed design (this work)
Technology (nm)	90	90	180	**90**
Frequency (GHz)	2.4	5	2.4	**2.4**
Gain (dB)	25	23	9.30	**22**
NF (dB)	< 2	1.31	1.90	**2.67**
S_{11} (dB)	< – 10	< – 10	< – 10	**< – 10**
S_{21} (dB)	27.64	13	11	**9.49**
P_{1dB} (dBm)	21	15	10	**3**
IIP3 (dBm)	20	14	16	**– 1**
Power (mW)	1.2	1.4	12	**7.01**
Supply (VDD)	3.3	3.3	1.5	**3.3**

Linearity and Compression Point (P_{1dB}). Linearity is the important parameter to determine the power efficiency as well as the presence of distortion in the LNA and these are represented by two analyses. One is the 1 dB compression and other is Input Intercept Point (IIP3). The compression point is represented at 2.45 GHz as 3.844 dBm and 15.8 dBm.

5. RESULTS AND DISCUSSION

Nanosensor applications demand compact chip size, which is provided by the optimized layout achieved by the VLSI design flow of pre-layout and post layout with the floorplan process with the placement of components and routing with respect design rules of DRC and LVS check. Cadence virtuoso for layout design and momentum RF for board layout are carried out with the design rule specifications already laid with the circuit schematic.

Various performance design factors and parameters are compared with the previous design of LNA at various technologies. The design of CMOS with supply voltage and operating at different range of frequency and these results are tabulated in Table 3.

The RF board layout, substrate model effect till layout generation with the successive stages involved in the design aspects of the proposed design are shown in Fig. 8a and Fig. 8b, respectively.

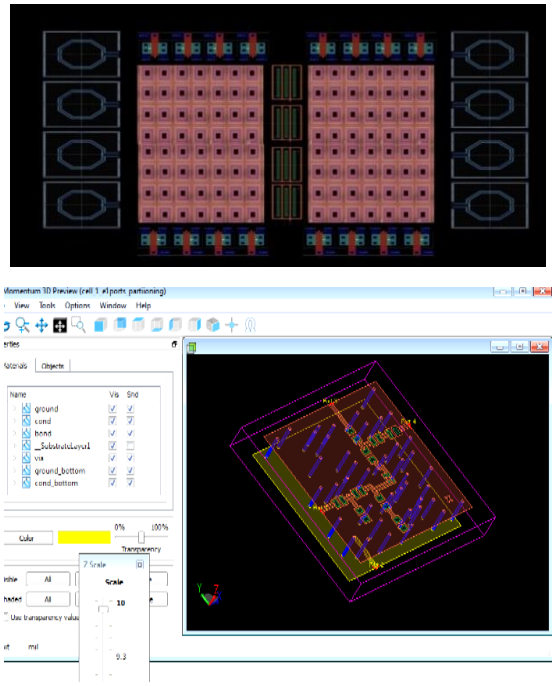

Fig. 8 – Layout of LNA (a) and momentum 3D preview and RF board layout (b)

6. CONCLUSIONS

This work presents the design of the pre-distortion circuit with the LNA to achieve improved linearity, and this employed proposed technique removes non-linear distortions in the LNA and support 5 GHz frequency without any interference in the signal transmission with high speed and result in high IIP3. The simulated results reveal gain greater than 20 dB and noise factor of 1 dB. The results are simulated in 90 nm CMOS tech and measured at 5 GHz frequency. The 1 dB compression of this design is achieved at + 21.6 dBm with IIP3 + 20.95 dBm and good impedance matching at the input as well as output. At 3.3 V the designed novel circuit consumes power of 1.2 mW.

Multi standard low-cost receiver front ends and provides reliability with micro- and nanoelectronic packaging industry-based technology. Validation of the result is carried out with S parameter simulation. The results indicate that the designed LNA1 is suitable for nanoelectronic sensor application.

REFERENCES

1. C.H. Doan, S. Emami, A.M. Niknejad, R.W. Broderson, *IEEE J. Solid State Circuits* **40**(1), 144 (2005).
2. Y.-S. Lin, J.-H. Lee, *Analog Integrated Circuit Signal Processing* **83**, 119 (2015).
3. Y.-S. Lin, J-H. Lee, *Analog Integrated Circuit Signal Processing*, **11**, 4 (2014).
4. J. Luo, L. Zhang, *IEEE Trans. Circ. Syst. –II*, **61**, 3 (2015).
5. S.K. Reynolds et.al., *IEEE J. Solid State Circ.* **39**, 11 (2014).
6. T. Dinc, A. Chakrabarti, H. Krishnaswamy, *IEEE J. Solid State Circ.* **51**(5), 1125 (2016).
7. Y.-S. Lin, C.-C. Chen, C-Y Lee, *Analog Integrated Circuits and Signal Processing*, **87**, 1 (2016).
8. H.V. Le, H.T. Duong, C.M. Ta, A.T. Huynh, R.J. Evans, E. Skafidas, *IEEE Radio-Frequency integration Technol.* **08** (2012).
9. D. Zito, D. Pepe, B. Neri, D. De Rossi, A. Lanata, A. Tognetti, E.P. Scilingo, *IEEE Trans. Circuit. Syst.* 2651 (2007).
10. R.T. Yazicigil, T. Haque, J. Zhu, Y. Xu, P.R. Kinget, *IEEE Trans. Circuit System.* (2016).
11. J. Elkind, E. Socher, *IEEE Trans. Circuit. Systems II*, **63**(10), 914 (2016).
12. H. Ali, *Hindawi Int. J. Aerospace Engineering* (2017).

Проект малошумного підсилювача з поточною архітектурою повторного використання та методом попереднього спотворення для наноелектронних датчиків, які працюють на частоті 2,4 ГГц

K. Suganthi[1], B. Venila[2], M.S. Abirami[3], Ritam Dutta[4]

[1] *Department of ECE, SRMIST, Chennai 603203 Tamil Nadu, India*
[2] *Department of Mathematics, SRMIST, Chennai 603203 Tamil Nadu, India*
[3] *Department of Computational Intelligence, SRMIST, Chennai 603203 Tamil Nadu, India*
[4] *CISR – ITER, Siksha 'O' Anusandhan University, Bhubaneswar 751030 Odisha, India*

У статті описується розробка різних конструкцій CMOS підсилювача з низьким рівнем шуму (LNA) для досягнення високої лінійності та низького рівня шуму в конструкціях нанодатчиків. Робоча частота становить 2,4 ГГц, а діапазон ISM підходить для додатків нанодатчиків. Новинка представлена структурою, що реконфігурується, з поточною архітектурою повторного використання для низького енергоспоживання, а метод попереднього спотворення використовується для досягнення хорошої лінійності без спотворень, що є кращим показником для конструкції підсилювача. Нанорозмірні конструкції отримано із збільшенням надійності. Пропонована конструкція LNA на основі CMOS має помірне підсилення з низьким коефіцієнтом шуму 2,6 дБ на частоті 2,4 ГГц та менше 2 дБ на частоті 5 ГГц. Хороша зворотна ізоляція досягається за рахунок коефіцієнту стоячої хвилі за напругою (VSWR), а оптимізований параметр S вхідних і вихідних коефіцієнтів відбиття становить менше – 10 дБ. Стабільність розробленого підсилювача та результати підсилення потужності сумісні з конструкцією наносенсора. Новизна, досягнута в конструкції, полягає у широкій смузі пропускання, хорошому показнику якості (FOM), малому розмірі, помірному підсиленні без спотворень, низькому рівні шуму та хорошій лінійності завдяки складній конструкції. Кім того, коефіцієнт підсилення потужності помірний, а сама конструкція займає невелику площу 0,5×0,2 мм^2.

Ключові слова: CMOS-дизайн, LNA, Нанопідсилювач, Конструкція схеми, Наночутливі матеріали.