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Improvement Analysis of Leakage Currents with Stacked High-*k*/Metal Gate in 10 nm Strained Channel HOI FinFET

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In the current semiconductor scenario, multiple gate FETs like tri-gate (TG) FinFETs have been a boon to continue the scaling of devices below 32 nm technology. The application of strained silicon has further enhanced drive currents. Leakage currents have been reduced by employing high-*k* materials, which has led to enhanced device switching characteristics. The development and characterization of a 10 nm channel TG *n*-FinFET device incorporating a tri-layered strained silicon channel and stacked high-*k* dielectric materials as the gate oxide are the motivation of this paper. The electrical characteristics and short channel effects (SCEs) of all the devices have been determined by replacing the SiO_2 gate oxide with a stacked gate oxide of 0.5 nm of SiO_2 and 0.5 nm EOT of various high-*k* dielectric materials like ZrO_2, Al_2O_3, Si_3N_4, and HfO_2. It is observed that SCEs and leakage characteristics are significantly improved by the use of stacked high-*k* dielectric materials like HfO_2, and the strain in the channel region significantly improves the drive current without hampering SCEs. Thus, the combination of strained silicon and HfO_2 dielectrics showed improved performance of the developed device with a reduced chip area.

Keywords: Tri-gate FinFET, Strained silicon, HOI structure, High-*k* dielectrics, Silvaco TCAD, Short channel effects.

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1. INTRODUCTION

With the incessant scaling of the geometry of conventional MOSFETS below 100 nm, there rose a huge physical problem in conventional MOSFETs [1] in the form of short channel effects (SCEs) and abrupt rise in sub threshold leakage currents [2]. In order to overcome these SCEs, the thickness of the oxide decreases, thus increasing the leakage due to gate induced drain leakage (GIDL) [3]. Thus, to overcome all such barriers, multiple gate field effect transistors (MUGFETs) are used, types of which are double gate (DG) and tri-gate (TG) FETs [4]. FinFETs are used as an alternative to bulk MOSFETs because of their improved stability, lower leakage current, improved short channel performance and enhanced subthreshold slope [5].

Erstwhile research has suggested that the materials used as gate oxide also signifies a crucial role in the performance of TG FinFETs. However, as the thickness of SiO_2 is reduced below 2 nm, this thin gate oxide layer leads to enhanced leakage current [6]. Recent research addressed this issue by substituting SiO_2 with several high-*k* dielectric materials such as Al_2O_3, Si_3N_4, HfO_2, and ZrO_2 keeping in line with effective oxide thickness (EOT) calculations and low dielectric leakage current. The EOT is calculated as [7]

$$\mathrm{EOT} = 3.9 \cdot T/K, \quad (1)$$

where T is the silicon dioxide thickness, K is the dielectric constant of the high-*k* material.

TG FinFET, along with the use of high-*k* dielectric materials, has been successful in reducing leakage currents of devices and improving the device performance. However, as device dimensions are reduced to 10 nm range, the physical thickness of the gate oxide layers becomes comparable to these dimensions. In order to reduce the physical thickness of the gate oxide layers, while maintaining the same EOT of 1 nm, stacked high-*k* materials are the need of the hour. This involves the deposition of 0.5 nm of SiO_2 as the gate oxide above the channel region of the device. Then a layer of high-*k* dielectric material is developed above this SiO_2 layer with an EOT of 0.5 nm, which attributes to a total gate oxide thickness of 1 nm.

Although the use of high-*k* dielectric materials reduces the leakage currents of the device, the drive currents are also severely degraded. Hence strained silicon technology [8] is used to enhance the drain current. When the strained silicon channel is introduced in FinFET, using a tri-layered silicon channel, it changes the physical parameters of the silicon channel by stretching atoms beyond their normal inter-atomic distance. The strained silicon region is achieved in the channel by incorporating a $Si_{0.6}Ge_{0.4}$ layer between two silicon layers, leading to three different layers in the channel. Therefore, while the induced strain in the channel improves drive currents of the 10 nm channel length FinFET making it faster, the use of various high-*k* gate oxide materials such as SiO_2 (k = 3.9), ZrO_2 (k = 22), Al_2O_3 (k = 9.3), HfO_2 (k = 25), Si_3N_4 (k = 7.8) leads to better control of the leakage currents and SCEs, which is the motivation of this paper.

2. DEVICE STRUCTURE

TG FinFETs are initially developed involving different channel materials. The geometrical details of the structure are listed in Table 1, where the device is

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developed, incorporating three different layers of the channel [9]. This consists of two layers of strained silicon and a $Si_{0.6}Ge_{0.4}$ layer between them, which creates strain in the silicon layers due to lattice mismatch. The strained silicon layers of the channel are developed to be 1.5 nm in thickness and the thickness of SiGe is developed to be 3 nm for the 10 nm HOI TG FinFET. The modelling and characterization of the devices are performed using Silvaco Atlas TCAD tools [10]. With the gate length of the structure kept at 10 nm, length, width and height of the source and drain are fixed at 6 nm only. The equivalent gate oxide layer is considered to be 1 nm thick. The 3D view of the HOI FinFET with stacked high-*k* material and the internal structure of the tri-layered strained silicon channel is shown in Fig. 1.

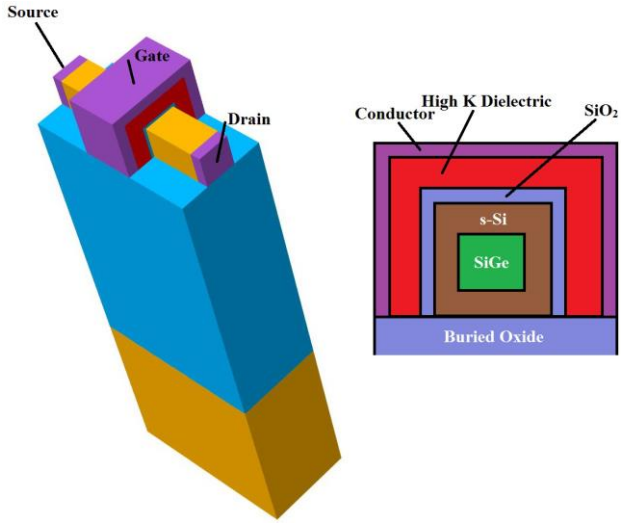

Fig. 1 – 3D representation and cross-section of the channel region of high-*k* gate stacked HOI FinFET

Table 1 – Parameters of the FinFET device

Parameters	Dimensions
Drain/source length	10 nm
Channel length	10 nm
Oxide thickness (SiO_2)	0.5 nm
Oxide thickness (high-*k*) (EOT)	0.5 nm
Height/width of FinFET	6 nm
Channel doping (*p*-type)	1×10^{15} cm^{-3}
Drain/source doping (*n*-type)	1×10^{18} cm^{-3}
Height of TBOX	50 nm
Height of substrate	30 nm

The different gate oxide materials considered are an inner layer of SiO_2 of 0.5 nm thickness along with high-*k* dielectrics like ZrO_2, HfO_2, Al_2O_3 and Si_3N_4 with an EOT of 0.5 nm for the analysis determining the best material among them for the practical scenario. For the numerical analysis of these devices, the Gummel and Newton methods are used because in HOI devices, due to the floating body effect observed in these devices, there is no direct contact of any electrode with it. Electrical parameters which are important for the analysis of devices are threshold voltage, subthreshold slope and leakage current.

3. RESULTS AND DISCUSSION

The linear and logarithmic (inset) transfer plots of the HOI TG *n*-FinFET are represented in Fig. 2. The I_D-V_{GS} characteristics of HOI *n*-FinFET take into account five different stacked gate oxides used for the study. The logarithmic plot of I_D-V_{GS} provides valuable information about the leakage current, which is also called off current (I_{off}), and the subthreshold slope.

The threshold voltage (V_{th}) of the 10 nm TG FinFET with only SiO_2 dielectric gate is 0.254 V. Taking into consideration other four stacked high-*k* dielectric oxide materials, like Si_3N_4, Al_2O_3, ZrO_2 and HfO_2, the respective threshold voltages, as shown in Fig. 3, are 0.251, 0.216, 0.216 and 0.317 V, respectively. Comparing these dielectric materials, we find that HfO_2 has the highest threshold voltage, so instead of using SiO_2, we can use a stack combination of silicon dioxide and hafnium oxide to get the best performance of the FinFET. It provides better voltage control of the device.

The maximum on current (I_{on}) is 183 μA/μm, which corresponds to SiO_2, but ZrO_2 outperforms other dielectrics in this aspect with 188.59 μA/μm. Other materials like Si_3N_4, Al_2O_3, and HfO_2 have maximum on currents of 159.75, 181.68 and 150.17 μA/μm, respectively. This discrepancy is due to the use of metal gates in the device, which have variable work functions.

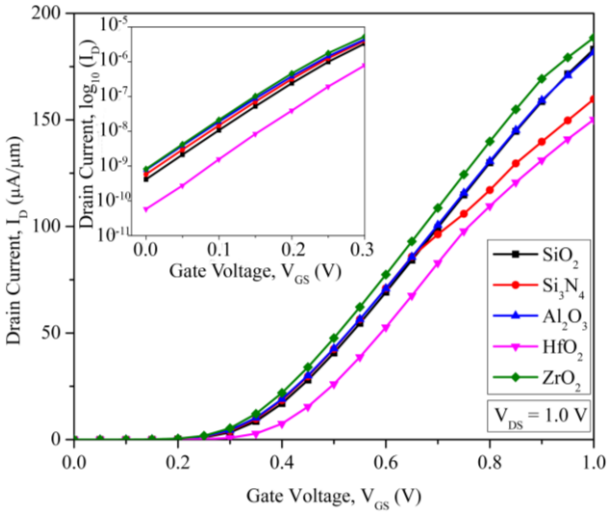

Fig. 2 – I_D-V_{GS} characteristics in linear scale (inset: logarithmic scale) at V_{DS} = 1 V

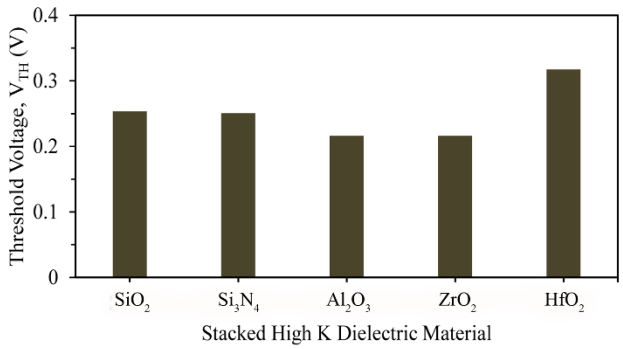

Fig. 3 – Transformation of the threshold voltage (V_{th}) of HOI design with different stacked dielectrics

Next, the dielectric gate performance is compared on other aspects like SS, leakage current (I_{off}) and DIBL to determine which material is best suited for high performance of device.

The off current can be computed using the formula below [11]:

$$I_{off}\ (\text{nA}) = 100 \cdot (W/L) \cdot (10\text{^}(-\ V_{th}/\text{SS})), \qquad (2)$$

where W and L are the channel width and length, respectively, V_{th} and SS denote the threshold voltage and subthreshold swing, respectively.

The change in leakage current (I_{off}) for five selected stacked dielectric materials is 58.12 pA/μm for HfO_2 and 0.584, 0.415, 0.825 and 0.779 nA/μm for Si_3N_4, SiO_2, ZrO_2 and Al_2O_3, respectively, as shown in Fig. 4. For the improved performance of the device, the material should have I_{off} as low as possible, which is observed for the stack combination of SiO_2 and HfO_2 gate oxides.

While comparing on the factor of I_{on}/I_{off} represented in Fig. 5, the value of I_{on} must be as large as possible and I_{off} should be as low as possible, so that the overall ratio must be high. For SiO_2, Si_3N_4, Al_2O_3, ZrO_2 and HfO_2, the respective values we get are 4.41, 2.74, 2.33, 2.29 and 25.83 (× 10^5), respectively. Thus, it is observed that the HfO_2 material as the gate oxide also performs best in this case as well.

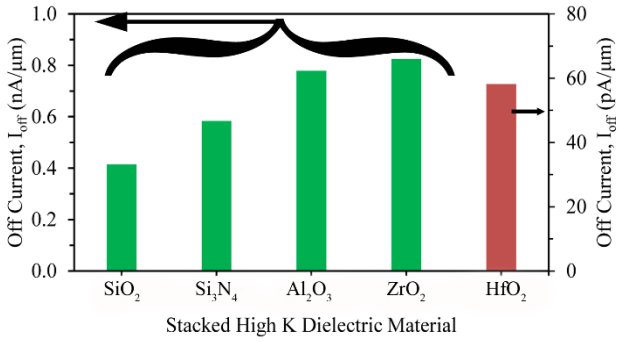

Fig. 4 – Transformation of I_{off} of HOI design with different stacked dielectrics

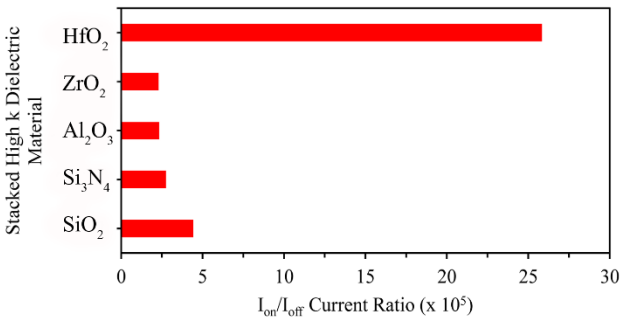

Fig. 5 – Reflection of changes in I_{on}/I_{off} ratio of HOI n-FinFET with different stacked dielectrics

Moving on to the next factor, subthreshold swing (SS) is obtained by a logarithmic plot of the transfer characteristics. We come to the following conclusion by comparing the SS of SiO_2 and HfO_2, whose respective SS values are 70.04 and 68.18 mV/decade, that in this aspect the stacked combination of SiO_2 and HfO_2 gates performs on par with the only SiO_2 gate from the given set of materials.

To calculate SS, we use the formula in [12]:

$$\text{SS (mV/decade)} = dV_{GS}/d(\log_{10}(I_{DS})), \qquad (3)$$

where dV_{GS} is the shift in the gate voltage and $d(\log_{10}(I_{DS}))$ is used to denote the shift in the logarithmic drain current.

As for the DIBL factor, the observations shown in Fig. 6 are 55.83, 65.73, 66.82, 58.25 and 50.43 mV/V for the set of gate oxide materials SiO_2 as well as a combination of SiO_2 with Si_3N_4, AL_2O_3, ZrO_2 and HfO_2, respectively. For the best material, the DIBL value must be the lowest to provide best performance and it is observed that HfO_2 performs best in this case providing lowest DIBL values.

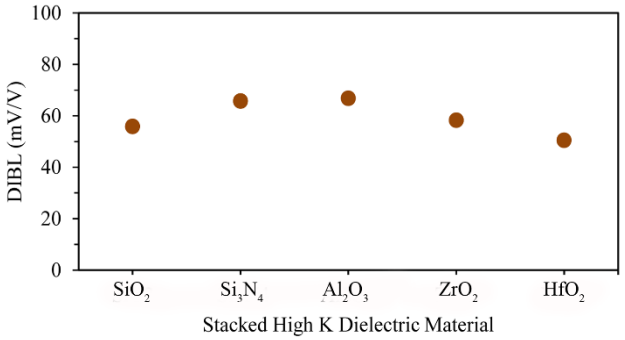

Fig. 6 – Variation of DIBL of HOI n-FinFET with different stacked dielectrics

Thus, it has been established that the stack combination of 0.5 nm of SiO_2 and 0.5 nm EOT of HfO_2 high-k dielectric material is best suitable to replace SiO_2 for controlling SCEs at sub-10 nm channel lengths. The use of strained silicon enhances the maximum drive currents of the devices, and the use of high-k materials keeps the leakage currents well under the limit defined by IRDS™ 2017 [13] standards. SCEs are also well controlled in the HOI structure with higher I_{on}/I_{off} current ratios, and smaller variations in SS and DIBL values are observed.

4. CONCLUSIONS

A basic TG FinFET was developed using three different channel layers to incorporate strain in the 10 nm channel length device. The gate oxide of the device was then developed by considering 0.5 nm of SiO_2, on top of which another oxide layer was grown, considering high-k dielectrics like Si_3N_4, Al_2O_3, ZrO_2 and HfO_2 with an EOT of 0.5 nm. The geometrical dimensions of the device were fixed at 06 nm. Drive currents, leakage currents, on-to-off current ratios of the device were compared for different dielectrics. It was observed that the inclusion of strain in the channel significantly improved the drive currents of the devices. The leakage currents also diminished with the use of high-k materials, especially for the device employing HfO_2 high-k dielectrics. Drive currents for 10 nm devices are around 183 μA/μm for only SiO_2 device and decrease slightly to 150 μA/μm for the stacked SiO_2 and HfO_2 device due to the use of metal gates in the HfO_2 device. Similarly, the leakage current I_{off} of HfO_2 is determined to be

58.13 pA/μm, whereas I_{off} of SiO_2 is 0.415 nA/μm. This leads to very high on-to-off current ratio for the stacked HfO_2 device, which is $25.83 \cdot 10^5$ as compared to $4.41 \cdot 10^5$ for only SiO_2 device. The subthreshold swing (SS) of all the devices varies between 68 and 70 mV/decade, but the DIBL of the device using stacked SiO_2 and HfO_2 as the gate oxide is minimum at 50 mV/V, while it is 56 mV/V for only SiO_2 device. This clearly shows that the device with HfO_2 provides the greatest control over SCEs with least leakage and better switching characteristics and has the possibility of becoming the device of choice in sub-10 nm technology nodes.

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Аналіз покращень струмів витоку з багатошаровим затвором high-*k*/метал у 10 нм напруженому каналі HOI FinFET

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У поточному розвитку напівпровідникової галузі багатозатворні FETs, як-от тризатворні tri-gate (TG) FinFETs, були стимулом для продовження масштабування пристроїв із технологією нижче 32 нм. Застосування напруженого кремнію ще більше посилило струми приводу. Струми витоку були зменшені за рахунок використання high-*k* матеріалів, що призвело до поліпшення комутаційних характеристик пристрою. Мотивом статті є розробка та характеристика пристрою TG *n*-FinFET з 10 нм каналом, що включає тришаровий канал із напруженим кремнієм та багатошарові high-*k* діелектричні матеріали як оксид затвора. Електричні характеристики та короткоканальні ефекти (SCEs) усіх пристроїв визначалися шляхом заміни оксиду затвора SiO_2 на багатошаровий оксид затвора із 0,5 нм SiO_2 та 0,5 нм EOT з різних high-*k* діелектричних матеріалів, таких як ZrO_2, Al_2O_3, Si_3N_4, та HfO_2. Помічено, що SCEs та характеристики витоку значно покращуються завдяки використанню багатошарових high-*k* діелектричних матеріалів, таких як HfO_2, а деформація в області каналу значно поліпшує струм приводу, не заважаючи SCEs. Таким чином, комбінація діелектриків з напруженого кремнію та HfO_2 показала покращення характеристик розробленого пристрою при зменшеній площі інтегральної схеми.

Ключові слова: Tri-gate FinFET, Напружений кремній, Структура HOI, High-*k* діелектрики, Silvaco TCAD, Короткоканальні ефекти.