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Effect of Channel Material on the Performance Parameters of GAA MOSFET

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The paper proposes an analysis of the characteristics of a cylindrical nanowire field effect transistor for two channel materials, namely Si and GaAs. The performance curves of Si and GaAs nanowire MOSFETs (GAA-NW-MOSFETs) in the 20 nm region are investigated via structure simulator called ATLAS. The simulation results show that the Si device has a much better threshold voltage and subthreshold swing, but the GaAs device has the best I_{ON}/I_{OFF} current ratio and less drain-induced barrier-lowering (DIBL). Furthermore, performance characteristics of analog devices such as drain current, transconductance, as well as output conductance, subthreshold slope (SS) and threshold voltage of the device are compared for two different materials (Si and GaAs). It is found that the GaAs material provides reduced drive current and lower leakage current, giving a high I_{ON}/I_{OFF}. In terms of SS, the Si material in the device ensures the perfect and stable device performance.

Keywords: Gate all around (GAA), Subthreshold slope (SS), Nanowire material, Metal oxide semiconductor (MOS), Analog frequency.

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1. INTRODUCTION

Nanotechnologies have been known for almost a century, and today they are exponentially widespread compared to past decades. Using Moore's law, the traditional metal-oxide-semiconductor field-effect transistor (MOSFET) architecture is scaled down to the nanoscale. Structure scaling is performed to improve device parameters, namely, to increase performance, reduce series power losses and IC compatibility [1]. The reduction in dimensions of short channel effects (SCEs) can raise many issues such as reduced threshold voltage and raised substrate bias, whereas narrowing of the transistor width leads to an increase in the electric field, leading to reduction in performance degradation and current reliability.

The semiconductor industry has spread widely and solved the traditional silicon issues concerning CMOS scaling, usage of efficiency boosters such as innovative materials, as well as creative device structures for CMOS devices of the future [2]. The GaAs MOSFET technique is utilized for higher RF-power at low voltage for providing high efficiency related to wireless products. This methodology offers a great advantage in terms of integrating RF power, then switching, and further controlling the power functions [3, 4]. It reduces the device cost and boosts new functionality for device integration. GaAs-GAA has been found to have an advantage over Si-GAA due to very high electron mobility and resistivity, as well as very low thermal conductance and transit time. In addition to the channel material (using GaAs or Si), scaling limitations can be overcome by employing different innovations n device geometry proposals [5-8]. For example, a cylindrical nanowire MOSFET device has a higher channel potential, which reduces SCEs and leads to an improvement in the subthreshold slope value. Additionally, it provides an opportunity to use undoped channel that can lower down the threshold voltage changes because of decreased random dopant fluctuations [9-11]. Thus, the use of nanowires is the optimized option to downscale devices. Moreover, the GAA structure provides better gate control capability over planar transistors [12].

Silicon nanowire FETs can be fabricated using different techniques such as the top-down approach: lithography, then etching and oxidation [13, 14], chemical vapor deposition, molecular beam epitaxy (MBE), and the bottom-up approach: with better wire size control. In the present work, an extensive analysis of GAA-MOSFET is done using two transport models. In our paper, GAA-MOSFET is designed with 20 nm channel length and investigated for two different channel materials: Si and GaAs. The loss parameter, namely SCE, is studied to evaluate device parameters which show optimized and better performance. The proposed device is evaluated and, according to its performance, can be attributed to the semiconductor industry.

2. PROPOSED DEVICE STRUCTURE

The device shown in Fig. 1 depicts silicon and gallium arsenide gate all around MOSFET (GAA-MOSFET) and the experimented ON current characteristic.

The GAA-MOSFET channel has a cylindrical shape, therefore the nanowire gate as well as source and drain, as shown in Fig. 1, are designed two different devices, one is silicon as a device material and the other is the gallium arsenide gate. The simulations of the proposed structure were performed with the ATLAS simulation tool [15] to calculate the performance of both GAA-MOSFET materials (Si and GaAs), as shown in Fig. 1. The gate length is $L = 20$ nm, the Si film thickness is 2.5 nm, the oxide thickness $t_{ox1} = 0.4$ nm (SiO_2) and $t_{ox2} = 2.1$ nm (HfO_2), with elevated dielectric gate is obtained by setting operation of metal work function with the same I_{OFF} and drain bias of 1.0 V.

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Maximum drain/source doping in the channel area with n-type doping is $N^{+} = 1 \times 10^{19}$ cm^{-3}.

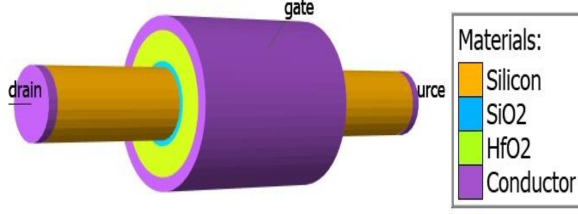


Fig. 1 – Cross-sectional view of Si-GAA-MOSFET

The geometric limits used for the proposed device simulation (GAA-MOSFET) are set out in Table 1. Simulation of a cylindrical nanoscale outboard close to the MOSFET gate with fixed charges is accomplished with an ATLAS-3D device simulation using the scattering method of flooding. Other models include Shockley-Read-Hall (SRH) models for handling field/concentration based mobility, plus SRH models induce minority charge recombination.

Table 1 – Parameters of GAA-NW-MOSFET

Parameters	Values
Channel length L, nm	20 nm
Source and drain length L_S, nm	10 nm
Gate oxide t_{ox}, nm	HfO_2 (2.1 nm) + SiO_2 (0.4 nm)
Substrate doping N^{+}, cm^{-3}	1×10^{19}
Gate/metal work function, eV	3.9 eV

It is very renowned that SCEs and leakage current exist in case when the channel length appears similar to the depletion layer width. The effects can cause numerous issues related to reliability. Furthermore, the included effects are threshold voltage roll-off, drain voltage, DIBL, and I_{ON}/I_{OFF} ratio.

For MOSFET, a minimum V_{gs} necessary to make device in ON state is known as threshold voltage (V_{th}). Fundamentally, it varies according to device geometry as well as opted material characteristics. For reliability of device performance, no variation in the V_{th} is acceptable as the device operability with the same efficiency is mandatory at the manufacture and consumer point. The present paper employed a constant-current method, so that the cut-off current is 1×10^{-7}.

For the weaker inversion region, a potential barrier exists over drain-source regimes. It causes rise in the drain-source current which in addition needs a high applied voltage to lower down the barrier height. This shows that drain is a very influential node for DIBL. This effect is more pronounced in case when the size of features reduces:

$$\mathrm{DIBL} = \Delta V_{th}/\Delta V_{ds}. \quad (1)$$

On lowering the potential barrier, free electrons initialize the flow of current in between source and drain, irrespective of the $V_{gs} < V_{th}$ condition. For present paper, the V_{th} value variation on the applied voltage has a value of 0.05 V and 1 V, respectively. The SS is actually a deviation in the V_{gs} value in order to achieve a significant change in drain current per decade. Generally, it reveals how effectively the value of drain current can be lowered down for a given value of V_{th}. The lower SS values can help us in achieving a better control over the channel, thus imposing lower leakage current and reduced on-off switching delay:

$$\mathrm{SS} = dV_{gs}/d(\log_{10} \cdot I_{ds}). \quad (2)$$

As per Boltzmann approximations, the MOSFET SS value is > 60 mV/dec.

I_{ON}/I_{OFF} ratio is the ratio of device currents while working in the accumulation to depletion mode. The device current in the OFF state refers to leakage current, which is generally triggered via carrier thermal emissions over potential barriers. The leakage current is the direct part of using the stationary power and the opposite part of the channel length. Therefore, the scaling down of MOSFET is of major concern while designing devices. The ON current reveals switching delay alleviations [16]. The I_{ON}/I_{OFF} raised values reveal an improvement in device performance. Fundamentally, V_t is the ratio of the maximum possible drain current ($V_{gs} = V_{dd}$, $V_{ds} = V_{dd}$) to device OFF current with a range of 10^6-10^{10}.

3. RESULTS AND DISCUSSION

Based on this detailed analysis, parameters and device characteristics have been studied to understand and figure out the performance of the devices, and comparative results in this session and two existing devices are also found. The stimulated outcome of conventional GAA-MOSFET with the marked work in [16] is depicted in Fig. 2. Tue reported data have been found via plot digitizer tool.

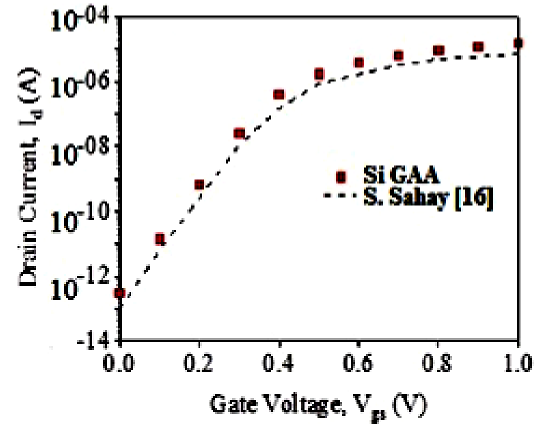


Fig. 2 – Experimental characteristics of the simulated output current of the GAA-MOSFET structure with a conventional structure [16]

Fig. 3 shows the I_d-V_{gs} transfer features of silicon and gallium arsenide nanowire GAA-MOSFETs at two different $V_{ds} = 50$ mV and 1 V values when V_{gs} varies from 0 to 1 V. For Si and GaAs, the I_d-V_{gs} characteristics are represented in Fig. 3. The GaAs material shows lower leakage current in comparison to the Si device. Its cause was the current direction, as well as the very low effective mass value of GaAs [13]. The low level of subthreshold leakage current improves the I_{ON}/I_{OFF} ratio of the GaAs device (Table 2 for parameter values).

The graph in Fig. 3 displays current variables that are different from the logarithmic scale, as a consequence offering I_{ON} and I_{OFF} values. The proposed structure with the GaAs material exhibits higher drain current (I_{ON}) than the Si material.

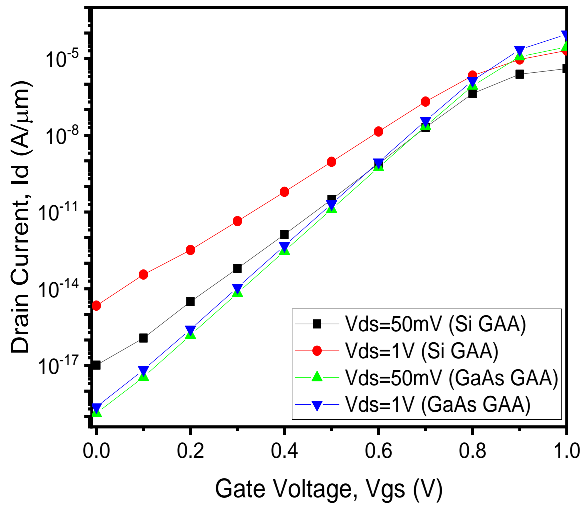


Fig. 3 – Drain current I_d vs. V_{gs} at different drain voltage V_{ds}: 50 mV and 1 V for silicon and GaAs materials, respectively

Table 2 reveals the impact of channel material differences in the proposed device performance. The threshold voltage and I_{ON}/I_{OFF} ratio increase; the width of depletion barrier region achieves larger proportion of the channel length with higher gate voltage requirement to collect carriers as well as to form the inversion layer. Therefore, increased threshold voltage and ON state current raise I_{ON}/I_{OFF}. A short length channel seeks more leakage current, thus increasing SS value. It is found that SS has an approximately fixed value of 10 nm or greater as channel length. And this reduces the sensitivity of the surface potential to the gate voltage, finally reducing it and increasing SS values. DIBL is obtained by direct measurement of the current leak, thus lowering the channel length. The lowering length of the channel results in a gradual boom in the drain-source voltage. A better drain voltage compared to the source voltage leads to a deeper field penetration, leading to a decrease in the channel barrier height, which creates the impact of DIBL.

Table 2 – Performance sheet

Figure of Merit	Silicon	GaAs
Threshold voltage	0.58	0.66
DIBL	63 mV/V	14 mV/V
SS	62 mV/decade	69 mV/decade
I_{ON}/I_{OFF} ratio	9.3×10^9	1.3×10^{15}

Analysis of the desired device parameters such as I_d vs V_{gs}, I_{ds} vs V_{ds}, transconductance and output conductance are examined in the current paper.

In Fig. 4, the transconductance (G_m) vs. V_{gs} curves at $V_{ds} = 1$ V are presented for GaAs and Si materials. Transconductance of the MOSFET determined the amplifier gain, as proven in (1). The development of G_m provides the transport efficiency of the provided gateway structure which is vital for analog performance:

$$G_m = \partial I_d / \partial V_{gs}. \quad (3)$$

The transconductance provides the device gain, and the transconductance curve peak provides the optimum point for device biasing as an amplifier. The curves in Fig. 4 and Fig. 5 show the effect of fixed charges interface upon G_m and output conductance, respectively. As it can be seen, the drain voltage increases the output transconductance of the device. The shift of G_m peak values shifts V_{gs} towards lower or higher values. All the parameters affect the reliability and performance of the device, since the device biasing point changes. The GaAs (Si) material has a high (low) G_m value with high (low) gain value over two channel materials.

In Fig. 5, G_{ds}, V_s and V_{gs} with different values of V_{ds} of 0.8, 0.9 and 1 V are introduced. To find the output conductance G_{ds}, the following formula is used:

$$G_{ds} = \partial I_d / \partial V_{ds}. \quad (4)$$

Fig. 5a and Fig. 5b reveal differences in G_{ds} for the proposed structure relative to the given drain bias. The value of G_{ds} is found lower in GaAs as compared to silicon-based device. A crucial metric to find device analog functioning in terms of efficiency is G_m/I_{ds}. A high value of I_{ds}/G_m demonstrates the device's ability for a certain bias value of drain to convert dc power to ac gain.

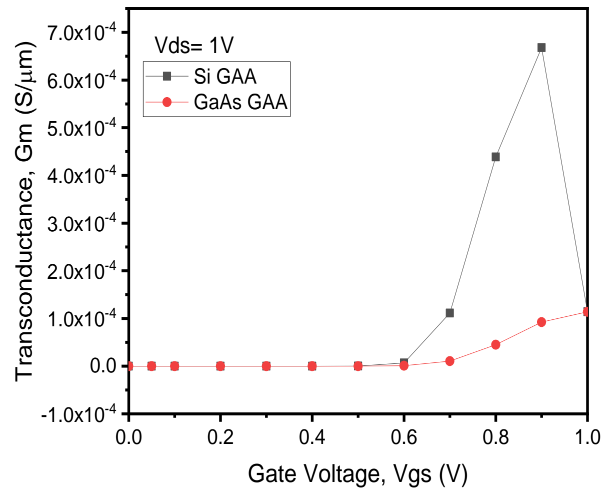
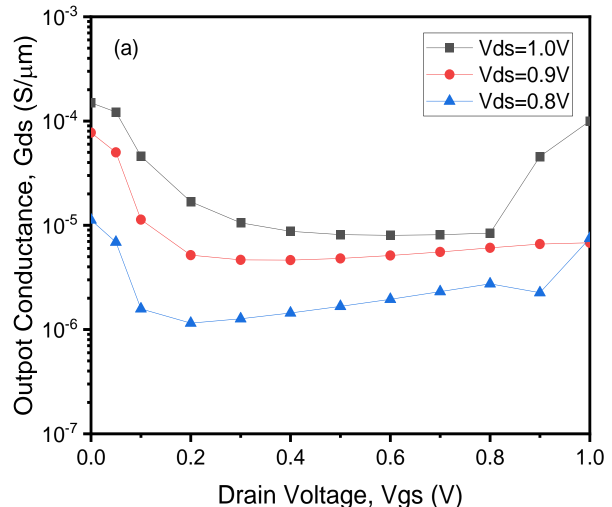


Fig. 4 – Transconductance G_m vs. V_{gs} at $V_{ds} = 1$ V



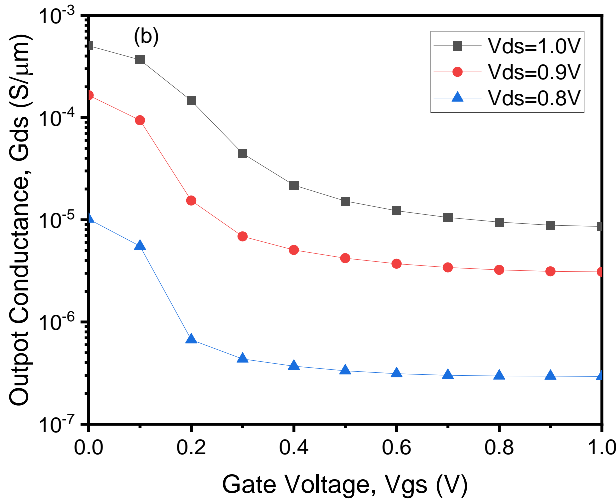


Fig. 5 – Output conductance G_{ds} vs. V_{gs} with different drain voltage V_{ds} of 0.8, 0.9 and 1 V for a) silicon GAA, b) GaAs GAA

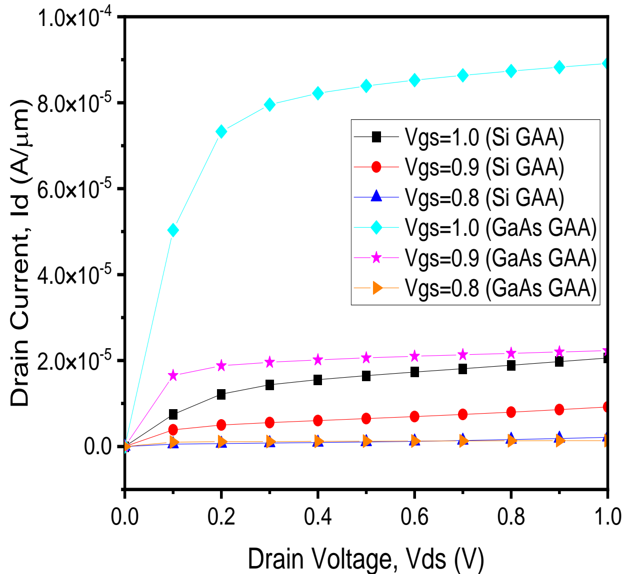


Fig. 6 – Drain current I_d vs V_{ds} at V_{gs} = 0.8, 0.9 and 1 V for silicon and GaAs materials

Fig. 6 reveals the direct drain current variation with V_{ds} for V_{gs} = 0.8, 0.9 and 1.0 V for GAA-MOSFET with Si and GaAs materials. The figure sincerely suggests that with rise in the value of gate voltage, GAA-MOSFET device leads to amplification in I_d which is related with gate material that leads to efficient operation of the device channel system, resulting in redistribution of the field on drain side. Increased drain bias decreases close to the lower gate metal work function and the drain end maintains a consistent concentration on inversion layer.

4. CONCLUSIONS

A cylindrical-gate nanowire-based FET has shown its capability in reducing scaling limitations and improving device performance. It has been found that GaAs based GAA MOSFET provides reduced drive current, lower leakage current, giving high I_{ON}/I_{OFF}. In terms of SS, Si material in the device gives an ideal as well as stable device performance. The GaAs material in the device has shown drastic degradation when performed for gate lengths less than 20 nm. Although a higher threshold voltage is available, the GaAs material is found to be less affected by the DIBL effect. However, the GaAs based GAA device gives the DIBL value of 14 mV/V (max), whereas it is 63 mV/V for silicon. Next, the channel length modulation effect is observed to a lesser extent in the case of the Si device compared to the GaAs material. The proposed device can be improved via high-k dielectric content utilization for gate insulation. An effect of gate and dielectric material on the Schottky-barrier MOSFET in analog analysis at L = 40 nm is analyzed in the present paper, suggesting that a less doped structure needs to be preferred in designing analog circuits that can lower SCEs and thermal budget. In sum, a comparison of Si GAA and GaAs GAA MOSFETs shows that the current-driving capability and gain are found efficient in the case of GaAs material, so the channel material can be chosen according to the application field.

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Вплив матеріалу каналу на експлуатаційні параметри GAA MOSFET

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У роботі пропонується аналіз характеристик польового транзистора з каналом із циліндричного нанодроту для двох матеріалів каналу, а саме Si та GaAs. Характеристики транзистора GAA-NW-MOSFET з нанодротами Si та GaAs в діапазоні 20 нм досліджуються за допомогою симулятора структури ATLAS. Результати моделювання показують, що пристрій з Si має набагато кращу порогову напругу та підпорогове коливання, а пристрій з GaAs має найкраще співвідношення струмів I_{ON}/I_{OFF} та менше значення DIBL. Крім того, порівнюються експлуатаційні характеристики аналогових пристроїв для двох різних матеріалів (Si та GaAs), такі як струм стоку, крутизна, а також вихідна провідність, підпороговий нахил (SS) і порогова напруга пристрою. Встановлено, що матеріал GaAs забезпечує знижений струм приводу та менший струм витоку, даючи високе I_{ON}/I_{OFF}. З точки зору SS, матеріал Si забезпечує ідеальну та стабільну роботу пристрою.

Ключові слова: GAA, Підпороговий нахил (SS), Матеріал нанодроту, Метал-оксид-напівпровідник (MOS), Аналогова частота.