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Si- and Ge-FinFET Inverter Circuits Optimization Based on Driver to Load Transistor Fin Ratio

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This paper proposes a novel method to adaptively select the best driver to load transistor fin ratio of six transistor (6T) FinFET-SRAMs according to the best values of noise margins and inflection voltages with a comparison between using Si and Ge as a semiconductor channel in a FinFET-SRAM cell. A 6T memory cell is considered as a primary memory cell that is widely used to design Static Random Access Memory (SRAM) and it has many applications in modern electronics. The 6T-SRAM cell is considered the first applicable unit to be implemented in an on-chip system using nanoscale FinFETs because of critical scaling issues of a SRAM cell of planar MOSFETs. The methodology for optimizing the driver to load transistor fin ratio will strongly depend on improving the noise margin and inflection voltage of the butterfly characteristics of the SRAM cell. The first step in this study of the 6T-FinFET-SRAM cell is to obtain the output characteristics (I_D-V_D) of FinFET. This research used simulation to generate the FinFET output characteristics and then used its data in a designed model by MATLAB to create the butterfly characteristics of the SRAM cell. The butterfly characteristics of 6T-Si- and Ge-FinFET-SRAM cell were investigated with fin ratios N_p/N_n of 0.5, 1, 2, 3, 4, and 5. Noise margin and inflection voltage were used as critical factors to obtain the optimal fin ratio N_p/N_n. Results indicate that the optimization strongly depends on the fin ratio for both Si and Ge semiconductors. Because of the channel fin shape with more channel current controlled, the results are completely different from a planar 6T-MOSFET-SRAM cell. For the 6T-Si-FinFET-SRAM cell, the optimized fin ratio was 2/1 and for the 6T-Ge-FinFET-SRAM cell, the optimized fin ratio was 1/4.

Keywords: FinFET, CMOS, Transistor, SRAM, Butterfly characteristics.

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1. INTRODUCTION

Since the traditional structure of silicon Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) is very close to the minimization limits, many new structures are being extensively investigated, and FinFET is the one of these new structures in nanodimensions. FinFET is of great interest from both researchers and semiconductor industry [1].

Transistors in nano-dimension such as Silicon Nanowire Transistors (SiNWTs), Carbon Nanotube Transistors (CNTs) and FinFETs are generating significant interest in the industry of electronics devices as they are the leaders among small, reliable and fast electronic devices. The functionality of the new generation of nanoscale circuits and a broadband range of extra applications will depend on the investigation of the characteristics of these FinFETs [2]. These new versions of MOSFETs and high-speed Integrated Circuits (ICs), which use new semiconductor nanoscale structures with fin-like channel, will find many applications in the near future after intensive investigation of their characteristics by researchers. Manufacturing technologies of ICs based on FinFETs are still in the growth phase, requiring new inventions along with confronting modern MOSFETs.

To grasp the characteristics of FinFET in-depth and also to evaluate its performances, simulation has become an important and leader in this new technology. Moreover, the simulation work could be supported by the experimental work to accelerate improvements to FinFETs by reducing their cost, recognizing their strengths and weaknesses, and minimizing their size to the nanometer zone [3-5].

According to the ITRS 2.0 roadmap (2016), FinFET will be the dominant transistor of the future in CMOS technology due to its ability to continue scaling down to 5 nm node technology and beyond [6], because its fin-shaped channel, which tends to have superior gate control, then allows to significantly improve short channel effects in planar MOSFETs, such as subthreshold slope and higher I_{ON}/I_{OFF} ratio [7, 8]. The perfect gate design with low OFF-state leakage current promotes the adoption of FinFETs for high-volume IC production with 22 nm node technology generation [9].

Neha et al. [10] explored Ge-FinFET under scaling a germanium fin with a standard cell architecture at a node of less than 5 nm. The authors explained that the germanium device has an almost 70 % improvement in drive current and is 3.4 times less in resistance.

A six transistor (6T) memory cell is considered as a primary memory cell that is widely used to design Static Random Access Memory (SRAM) and has many applications in modern electronics. The main goal of nowadays semiconductor technology is to design IC chips (including SRAM), which contain nanoscale transistors with high speed and performance, resulting in higher levels of integration with more memory in the available area. To fulfill this target, the designers of ICs are developing a new MOSFET structure that makes SRAM cells minimal and higher in integration.

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A 6T SRAM is considered as the first applicable unit to be implemented in an on-chip system using FinFET because of critical scaling issues for a SRAM cell with planar MOSFET, such as the need for continuous scaling down cell size and stability issues [11]. Thus, in this paper, a computer-based model has been developed to investigate and optimize the fin ratio of the static characteristics of Si and Ge 6T FinFET-SRAM cells.

The device optimization technique was carried out in [12] for low-power FinFET-SRAM, where the gate sidewall offset spacer thickness is optimized to yield a minimum leakage current in FinFETs. The scalability of the FinFET SRAM supply voltage was investigated in [13] for low-power applications, and the noise margins affected by the line-edge roughness (LER) were also studied. Optimization of fin thickness and height of FinFET-SRAM was explored in [14] depending on leakage and stability by examining the design space along with surface orientation. The implementation of different FinFET devices and the performances of 6T SRAMs are compared for various pull-up, pull-down and pass-gate (PU:PD:PG) transistor ratios to identify the superior FinFET device for low-power consumption and high-speed SRAM applications [15].

This paper proposes a novel method to adaptively select the best driver-to-load transistor fin ratio N_p/N_n, where N_p is the number of fins of driver of *n*-channel transistor and N_n is the number of fins of load of *p*-channel transistor. The best value of fin ratio (N_p/N_n) of FinFET-SRAMs will be found according to the best values of noise margins and inflection voltages with a comparison between using Si and Ge as semiconductor channels in the FinFET-SRAM cell.

SRAM cell configuration consists of six MOSFETs. It has two logic inverters, and each inverter input is connected to the second inverter output, *p*-channel pull-up and *n*-channel pull-down transistors, and two *n*-channel transistors work as a pass-gate. When the horizontally running word-line is enabled, the two pass-gate transistors are turned on and linked to the bit storage nodes with vertically running bit-lines. In other words, they allow access to the cell for read and write operations, acting as bidirectional transmission gates.

2. METHODOLOGY

The structure of FinFET is shown in Fig. 1. The first step in this investigation of the 6T-FinFET-SRAM cell is to obtain the output characteristic I_D-V_D of FinFET. In this study, the output characteristic I_D-V_D of FinFET was modeled using a simulation tool MuGFET [16]. MuGFET simulation software tool was invented at Purdue University. Table 1 illustrates the parameters that were used at this stage of the simulation to determine the output characteristics of FinFET.

The second step in this investigation of the 6T-FinFET-SRAM cell is to use the new MATLAB model (proposed in [17]) to produce the butterfly characteristics of the 6T-FinFET-SRAM cell. This model was used to obtain the transfer characteristics of FinFET logic inverters of SRAM and then to calculate the butterfly characteristics of the 6T-FinFET-SRAM. The model is designed to find the intersection points of the curves that have the same gate voltages of the I_D-V_D characteristic of the load and driver FinFETs, which are configured as a CMOS inverter in the SRAM cell circuit. Mainly, the MATLAB model is constructed to produce V_{out}-V_{in} characteristics and I_{out}-V_{in} characteristics of the FinFET-CMOS inverter circuit based on the output characteristics of FinFETs [17]. This new model will calculate the Noise Margin Low (NML) and Noise Margin High (NMH). The fin-ratio optimization in principle will be based on improving the inflection voltage (V_{inf}) and noise margins. The NML, NMH and inflection voltage were used as limiting factors in this study. So, the best SRAM cell has equal and higher values of the NMH and NML as much as possible. Both NMH and NML should be higher and equal as possible, and also the V_{inf} value should be close to half the V_{DD} (the source voltage of inverters).

Table 1 – Parameters of the FinFET used in this research

Parameter name	*n*-channel	*p*-channel
Fin width (*t*)	30 nm	30 nm
Source length	50 nm	50 nm
Drain length	50 nm	50 nm
Channel length (L_g)	45 nm	45 nm
Oxide thickness (SiO_2) (T_{ox})	2.5 nm	2.5 nm
Gate overlap	2 nm	2 nm
Channel concentration	$1\cdot10^{16}$/cm^3 (*p*-type)	$1\cdot10^{16}$/cm^3 (*n*-type)
Source and drain concentration	$1\cdot10^{19}$/cm^3 (*n*-type)	$1\cdot10^{19}$/cm^3 (*p*-type)

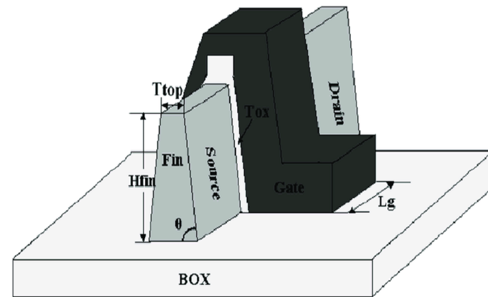

Fig. 1 – FinFET structure [1]

3. RESULTS AND DISCUSSION

The fin ratio of *p*- and *n*-channel FinFETs has been chosen to make the 6T-SRAM cell perform better. The fin ratio (N_p/N_n) of both *p*- and *n*-channel FinFETs is the dimensional ratio in normal Si-CMOS, where dimensional ratio in a Si-CMOS logic inverter is 3/1 due to an increase in the *p*-channel transistor width or a decrease in the *n*-channel transistor length to restore the low hole mobility in the *p*-channel. In this research paper, the same dimensions and concentrations given in Table 1 were used to study the effect of fin ratio for both Si and Ge-6T-SRAM cells on the characteristics of the SRAM.

Fig. 2 illustrates the butterfly characteristics of the 6T-Si-FinFET-SRAM cell, from which it can be seen that the inflection point (V_{inf}) shifts to the right with increasing fin ratio (N_p/N_n) due to an increase in *p*-channel fins or a decrease in *n*-channel fins, where $N_p/N_n = 0.5$, 1, 2,

3, 4 and 5 at voltage $V_{DD} = 1$. In planar CMOS, an increase in I_d in the load transistor (*p*-channel), by increasing this transistor width with a ratio of 3 to 1, leads to the overlap of the *p*-channel with a lower hole mobility. According to the results of this paper, it is clear that the ratio of the number of fins in *p*- and *n*-channel FinFETs does not follow this rule. The fin-ratio optimization in principle will depend on the improvement in the inflection voltage (V_{inf}) and noise margins.

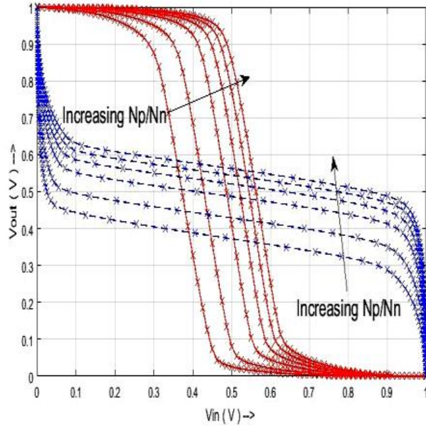

Fig. 2 – Butterfly characteristics of the 6T-Si-FinFET-SRAM cell with N_p/N_n ratio of 0.5, 1, 2, 3, 4, and 5

The NMH, NML and inflection voltage were used as limiting factors in this study, so the best SRAM cell has equal values of NMH and NML. Both NMH and NML values should be higher and as equal as possible, and V_{inf} should be closer to half the V_{DD} value. According to Fig. 2, for the Si-FinFET-SRAM, an increase in N_p/N_n leads to an increase in NML and a decrease in NMH and intersection at an optimized fin ratio $N_p/N_n = 2.2 \approx 2 = 2/1$. In the current characteristics (Fig. 3), the current increases to the inflection point with increasing fin ratio. It is seen from Fig. 4 that the intersection of the noise margin (NML and NMH) curves occurs at a ratio $N_p/N_n = 2.2 \approx 2 = 2/1$, which is considered the best and optimized fin ratio. At this best ratio, NMH = 0.35 V, NML = 0.34 V and $V_{inf} = 0.5$ V, which is equal to $V_{DD}/2$ (0.5 V).

For the 6T-Ge-FinFET-SRAM cell, Fig. 5 shows the butterfly characteristics, from which it is seen that the inflection point (V_{inf}) shifts to the right with increasing fin ratio N_p/N_n due to an increase in the number of fins of the *p*-channel transistor or a decrease in the number of fins of the *n*-channel transistor, where $N_p/N_n = 0.25$, 0.5, 0.75, 1, and 2 at voltage $V_{DD} = 1$.

An increase in I_d in the *n*-channel transistor by increasing the number of fins in driver (*n*-channel) FinFET leads to recovery of a lower current in *n*-channel FinFETs. This procedure provides better noise margins of the SRAM circuit. The fin ratio optimization in principle aims to improve noise margins and of course the inflection voltage (V_{inf}). Improvements in noise margins and inflection voltage are considered as limiting factors. The best SRAM cell has equal values of NMH and NML. Both NMH and NML should be as high as possible, provided that they are nearly equal, and V_{inf} must be close to half the V_{DD} value.

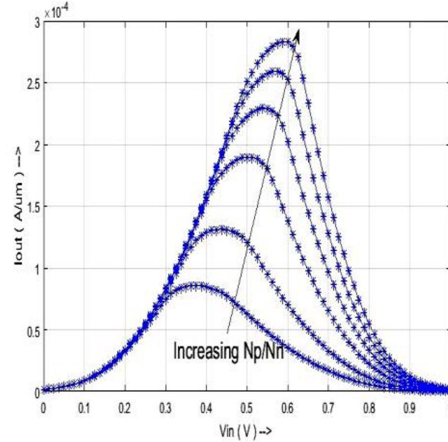

Fig. 3 – Current characteristics of the 6T-Si-FinFET-SRAM cell with N_p/N_n ratio of 0.5, 1, 2, 3, 4, and 5

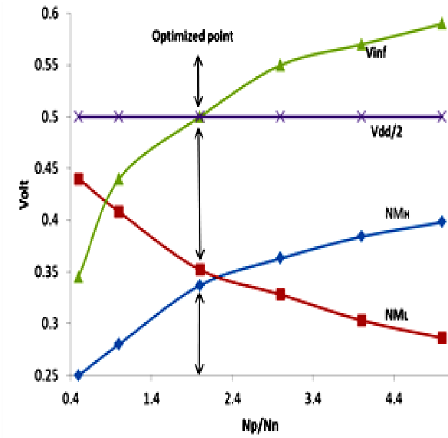

Fig. 4 – Noise margin and inflection voltage optimization with fin ratio in the 6T-Si-FinFET-SRAM cell

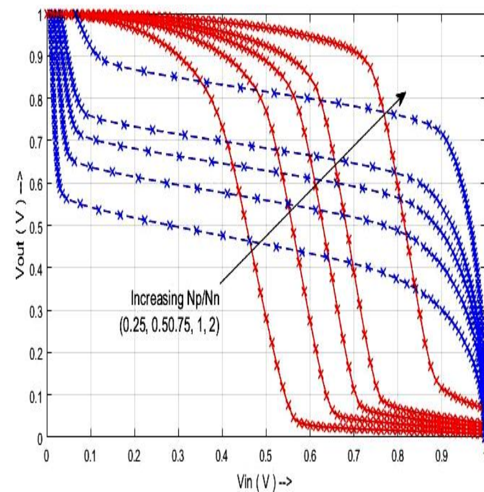

Fig. 5 – Butterfly characteristics of the 6T-Ge-FinFET-SRAM cell with N_p/N_n ratio of 0.25, 0.5, 0.75, 1, and 2

From the current characteristics (Fig. 6) it is obvious that the current increases to the inflection voltage with increasing fin ratio from 0.25 to 2. According to Fig. 7, an increase in the fin ratio leads to a decrease in NMH and an increase in NML when crossing curves at the optimized fin ratio (= 0.28 ≈ 0.25 = 1/4).

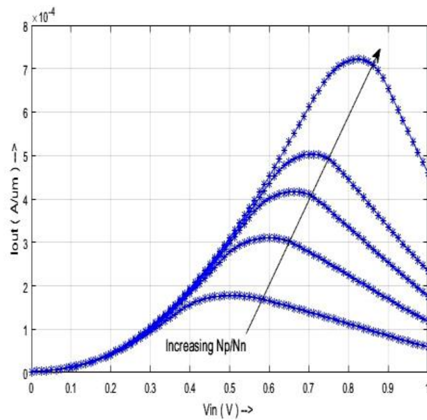

Fig. 6 – Current characteristics of the 6T-Si-FinFET-SRAM cell with N_p/N_n ratio of 0.25, 0.5, 0.75, 1, and 2

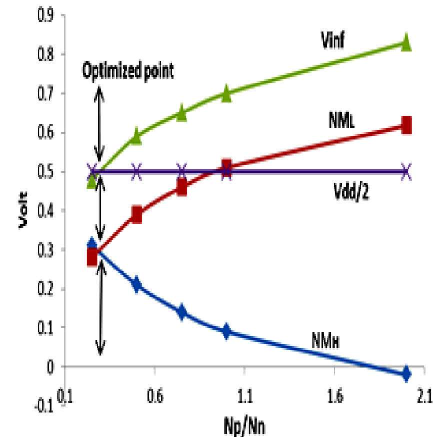

Fig. 7 – Noise margin and inflection voltage optimization with fin ratio in the 6T-Ge-FinFET-SRAM cell

Fig. 7 shows that the intersection of NMH and NML curves occurs at a fin ratio of $N_p/N_n = 0.28 \approx 2.5 = 1/4$, which is the best value for fin ratio. At this optimized point, NMH = 0.31 V, NML = 0.28 V, $V_{inf} = 0.5$ V, which equals to $V_{DD}/2$ (0.5 V).

4. CONCLUSIONS

The influence of load to driver fin ratio of FinFET in a 6T-SRAM cell with Si and Ge as a semiconductor channel on the SRAM characteristics was investigated in this research paper. The limiting parameters in this optimization were butterfly characteristics, best noise margins and inflection voltage. The results indicate that the optimization strongly depends on the fin ratio for both Si and Ge semiconductors. Due to the channel fin shape with more amount of channel current controlled, the results are completely different from a planar 6T-MOSFET-SRAM cell. For the 6T-Si-FinFET-SRAM cell, the optimized fin ratio was 2/1, and for the 6T-Ge-FinFET-SRAM cell, it was 1/4.

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