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Modeling and Simulation of MOSFET (High-*k* Dielectric) Using Genetic Algorithms

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A Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a type of field effect transistor; the operation is based on the effect of an electric field applied to the metal-oxide-semiconductor structure, i.e., to the gate electrode. It is an essential electronic component, especially in the microelectronics industry. Since the invention of the integrated circuit, the principal growth vector of the silicon microelectronics industry has been the miniaturization of MOSFETs. To minimize the undesirable effects (for example leakage current) due to the miniaturization of MOSFETs, several solutions have been used to improve the performance of MOSFETs. Among these solutions is the use of new high permittivity gate oxides (for example, HfO_2 oxide). A nanoscale MOSFET is a complex electronic device, and the simulation of nanoscale devices therefore needs new theories and modeling techniques (for example, artificial intelligence). The Genetic Algorithms (GAs) are adaptive metaheuristic algorithms based on the evolutionary ideas (Evolutionary Algorithms (EAs)) of natural selection and genetics. GAs are used to generate high-quality solutions to optimization and search problems by relying on genetic operators such as selection, crossover and mutation. This paper describes advanced modeling (optimization), simulation and parameter extraction of nanoscale MOSFETs (HfO_2 oxide) using a GA approach. The electrical characteristics of MOSFETs are predicted according to different parameters (drain current, drain voltage, gate voltage, channel length, oxide thickness).

Keywords: MOSFET, HfO_2, SiO_2, CMOS technology, High-*k* dielectric, Artificial intelligence, Genetic algorithms.

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1. INTRODUCTION

During the past decades, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have continually been scaled down in size; different scaling limits for MOSFETs have been discussed. These components, which now reach nanometer size, must comply with the rules established by the ITRS (International Technology Roadmap for Semiconductors). In this context, the oxide thicknesses reach limitations that make them permeable to leakage currents. The solution is to replace SiO_2 by a high-*k* dielectric, many candidates are potentially suitable to meet the specifications imposed by the ITRS, one of them, hafnium oxide (HfO_2). This material has been widely studied in recent years because of its promising physical and electrical properties and compatibility with silicon technology. HfO_2 found application in [1, 2].

This paper describes the electrical characterization and modeling of MOSFETs (HfO_2 oxide) using Genetic Algorithms (GAs) to identify different parameters.

2. EKV TRANSISTOR MODEL

There are three modes (regions) of operation in a MOSFET.

When $V_{GS} < V_T$ (cutoff region), V_T is the threshold voltage, the transistor is turned off, and there is no conduction between drain and source ($I_D \approx 0$).

When $V_{GS} > V_T$ and $V_{DS} \le V_{GS} - V_T$ (linear region), the transistor is turned on; the current equation of the MOSFET is modeled by:

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[\left(V_{GS}-V_T\right)V_{DS}-\frac{V_{DS}^2}{2}\right], \quad (1)$$

$$I_D = k_n\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right], \quad (2)$$

$$k_n = \frac{\mu_n \varepsilon\varepsilon_{ox}}{2t_{ox}}\frac{W}{L} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right). \quad (3)$$

When $V_{GS} > V_T$ and $V_{DS} \ge V_{GS} - V_T$ (saturation region), the switch is turned on, the device is in saturation mode of operation, and the drain current is given by:

$$I_D = k_n\left(V_{GS}-V_T\right)^2. \quad (4)$$

When $V_{DS} = V_{GS} - V_T$, from equations (2) and (4) we get $I_D = k_n V_{DS}^2$.

In some cases, such as to simulate an analog circuit, it is necessary to have a model which is continuous in all regimes of operation (weak or strong inversion). The EKV model developed in section 7.8 [3] solves the problem, the EKV MOSFET model is a mathematical model of a MOSFET which is intended for circuit simulation and analog circuit design.

Fig. 1 presents the $\log I_D(V_{GS})$ characteristic of a standard MOSFET.

EKV defines the drain current as a combination of a forward current controlled by the source and a reverse current controlled by the drain. Following the work of Enz, Krummenacher and Vittoz (the so-called "EKV model"), one can rewrite Eq. (7.8.2) (see section 7.8 [3]) as follows [4-6]:

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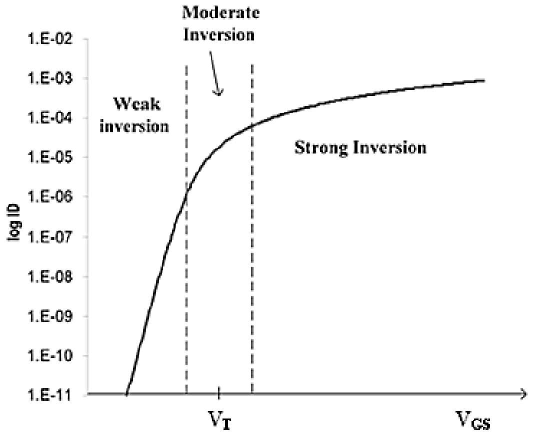

Fig. 1 – Discontinuity of $I_{DS}(V_{GS})$ characteristic at $V_{GS} \cong V_T$

$$I_D = I_F - I_R\,, \tag{5}$$

$$I_D = 2n\mu_n C_{ox}\frac{W}{L}\left(\frac{KT}{q}\right)^2\left[\begin{array}{l}\left\{\ln\left[1+\exp\left(\dfrac{V_P-V_S}{2KT/q}\right)\right]\right\}^2\\ -\left\{\ln\left[1+\exp\left(\dfrac{V_P-V_{DS}}{2KT/q}\right)\right]\right\}^2\end{array}\right], \tag{6}$$

$$V_P = \frac{(V_{GS}-V_T)}{n}\,. \tag{7}$$

On the other hand, $V_S = 0$, $V_{DS} < V_P$ and $V_{GS} > V_T$ (i.e., the transistor operates in a non-saturated regime). In this case, the exponential terms are much larger than unity, and one can write:

$$I_D = 2n\mu_n C_{ox}\frac{W}{L}\left(\frac{KT}{q}\right)^2\left[\left(\frac{V_P}{2KT/q}\right)^2-\left(\frac{V_P-V_{DS}}{2KT/q}\right)^2\right], \tag{8}$$

$$I_D = \frac{1}{2}n\mu_n C_{ox}\frac{W}{L}\left[2V_{DS}V_P - V_{DS}^2\right], \tag{9}$$

$$I_D = \frac{1}{2}n\mu_n C_{ox}\frac{W}{L}\left[2\frac{(V_{GS}-V_T)V_{DS}}{n} - V_{DS}^2\right], \tag{10}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{GS}-V_T)V_{DS} - nV_{DS}^2\right], \tag{11}$$

$$I_D = k_n[2(V_{GS}-V_T)V_{DS} - nV_{DS}^2]\,. \tag{12}$$

3. EQUIVALENT OXIDE THICKNESS

The miniaturization of a MOSFET (SiO_2 oxide) in the nanoscale range produces dramatic gate leakage issues detrimental for the performance. The capacitive coupling C_{ox} between the gate and the substrate must increase or remain constant. Therefore, to maintain these properties, the gate oxide thickness t_{ox} is reduced [7], but when the thickness decreases below a certain value, several problems arise [8-10]. To solve these problems, it is necessary to replace the gate dielectric (currently SiO_2) with a high-*k* dielectric (for example, HfO_2), then we can increase the oxide thickness and reduce the gate current, while keeping a high C_{ox}. The concept of an equivalent oxide thickness (EOT) is introduced. Fig. 2 shows a comparison of the leakage current density as a function of the equivalent oxide thickness (EOT) between HfO_2 and SiO_2. The equivalent oxide thickness is given by:

$$C_{\mathrm{SiO_2}} = C_{High-k} \Leftrightarrow \frac{\varepsilon_{\mathrm{SiO_2}}}{t_{\mathrm{SiO_2}}} = \frac{\varepsilon_{High-k}}{t_{High-k}} \tag{13}$$

$$\Rightarrow t_{\mathrm{SiO_2}} = EOT = \frac{\varepsilon_{\mathrm{SiO_2}}}{\varepsilon_{High-k}}t_{High-k}\,. \tag{14}$$

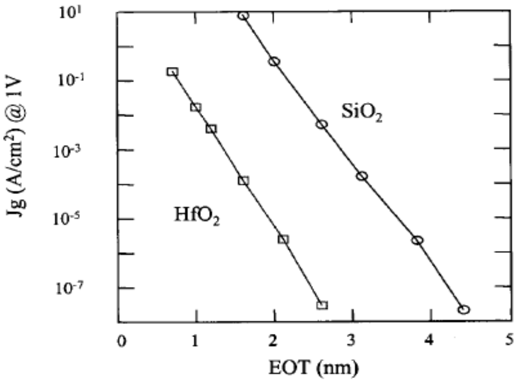

Fig. 2 – Comparison of the leakage current density between HfO_2 and SiO_2 [11]

4. GENETIC ALGORITHMS (GAs)

Genetic algorithms (GAs) were first developed and introduced by Holland in 1975. GAs are adaptive metaheuristic search algorithms based on evolutionary ideas (Evolutionary Algorithms (EAs)) of natural selection and genetics, which generate approximate solutions to optimization problems. GAs found application in [12, 13], etc. The fitness function *f* is defined as:

$$f = \frac{1}{M}\sum_{V_{GS}}\sum_{V_{DS}}\left[\frac{I_{DS,NUM}-I_{DS,GA}}{I_{DS,NUM}}\right]^2 + \frac{1}{M}\sum_{V_{GS}}\sum_{V_{DS}}\left[\frac{\log(I_{DS,NUM})-\log(I_{DS,GA})}{\log(I_{DS,NUM})}\right]^2 \tag{15}$$

The expression of the normalized error is given by:

$$\varepsilon = \frac{1}{M}\sum_{i=1}^{m}\sum_{j=1}^{n}\left|\frac{I_{DS,NUM}-I_{DS,GA}}{I_{DS,NUM}}\right|. \tag{16}$$

5. SIMULATION AND DETERMINATION OF PARAMETERS WITH GA PROCESS

Fig. 3, Fig. 4, Fig. 5 and Fig. 6 show a comparison between the results predicted by the GA model with those calculated by the compact model for lightly doped short channel, with $t_{ox} = 14$ nm (monoclinic-HfO_2, EOT = 3 nm) and $t_{ox} = 22$ nm (tetragonal-HfO_2, EOT = 3 nm).

Fig. 7 and Fig. 8 show the convergence behavior to the optimal solution (evolution of the fitness function). The final optimized parameters are given in Table 1, Table 2 and Table 3.

Table 1 – Optimized MOSFET parameters ($I_D(V_D)$)

	Parameters	Compact Model	GA Model
MOSFET $L = 0.1$ µm, monoclinic	V_T	0.01	0.01017
	k_n	0.2844e-3	0.28459e-3
MOSFET $L = 0.1$ µm, tetragonal	V_T	0.01	0.00995
	k_n	0.2799e-3	0.27960e-3

Table 2 – Optimized MOSFET parameters ($I_G(V_G)$)

	Parameters	Compact Model	GA Model
MOSFET $L = 0.1$ µm, monoclinic	V_T	0.01	0.01050
	k_n	0.2844e-3	0.28520e-3
MOSFET $L = 0.1$ µm, tetragonal	V_T	0.01	0.01016
	k_n	0.2799e-3	0.28016e-3

Table 3 – GA parameters used in this application

GA parameters	Values
Population size	5-20-50
The Maximum number of generations	5000
Fitness function	Proportional
Selection	Tournament
Crossover	Dispersed
Mutation	Uniform
Mutation rate	0.01-0.05-0.1
Reproduction rate	0.8

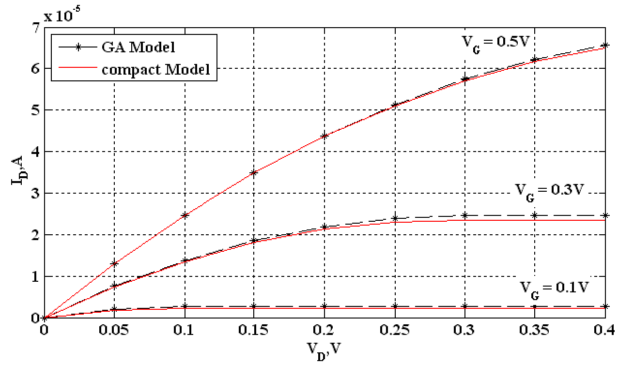

Fig. 3 – $I_D(V_D)$ characteristics of the MOSFET (m-HfO$_2$ oxide)

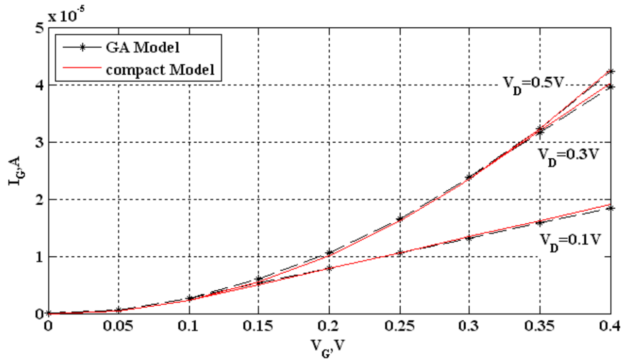

Fig. 4 – $I_G(V_G)$ characteristics of the MOSFET (m-HfO$_2$ oxide)

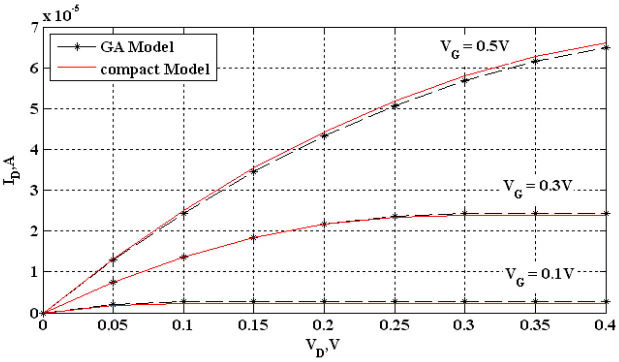

Fig. 5 – $I_D(V_D)$ characteristics of the MOSFET (t-HfO$_2$ oxide)

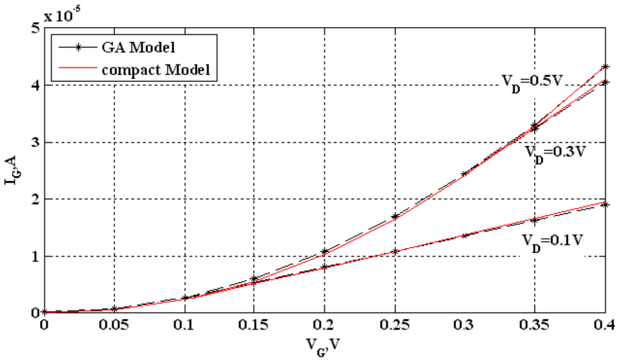

Fig. 6 – $I_G(V_G)$ characteristics of the MOSFET (t-HfO$_2$ oxide)

The electrical characteristics of a high-*k* MOSFET (monoclinic-HfO$_2$ oxide) (Fig. 3, Fig. 4) and electrical characteristics of a high-*k* MOSFET (tetragonal-HfO$_2$ oxide) (Fig. 5, Fig. 6) have the same results but with different thickness ($t_{\text{m-HfO2}} = 14$ nm, $t_{\text{t-HfO2}} = 22$ nm).

The electrical characteristics simulated by the compact model are compared with the GA model. It can be observed that good agreement between the compact and GA data was obtained by both models.

From the results obtained (Fig. 3, Fig. 4, Fig. 5 and Fig. 6), HfO$_2$ [20] is a good candidate to replace SiO$_2$.

The results in this work are in good agreement with previous results on extraction parameters and electrical characteristics for MOSFETs using various techniques of artificial intelligence (genetic algorithm [14-17] and neural networks [18, 19]) applied to different MOSFET models.

Mutation rate. As illustrated in Fig. 7, GA was improved by increasing the mutation rate from 0.01 to 0.1. A high mutation rate introduces high diversity in the population and makes the search process similar to a random search (Fig. 7c). On the other hand, it is very difficult for GA to find a global solution with such a low mutation rate (Fig. 7a), and thus the performance will be degraded.

Population size. As illustrated in Fig. 8, GA was improved by increasing the population size from 5 to 50. Too small or too large a population size degrades the performance of GA (Fig. 8a, c).

It should be noted that the GA execution depends mainly on the selection and recombination processes. After analyzing the results, we noticed that the evolution of the fitness function gives good performance with a mutation rate of 0.05 and a population size of 20 for the optimization process (Fig. 7b and Fig. 8b).

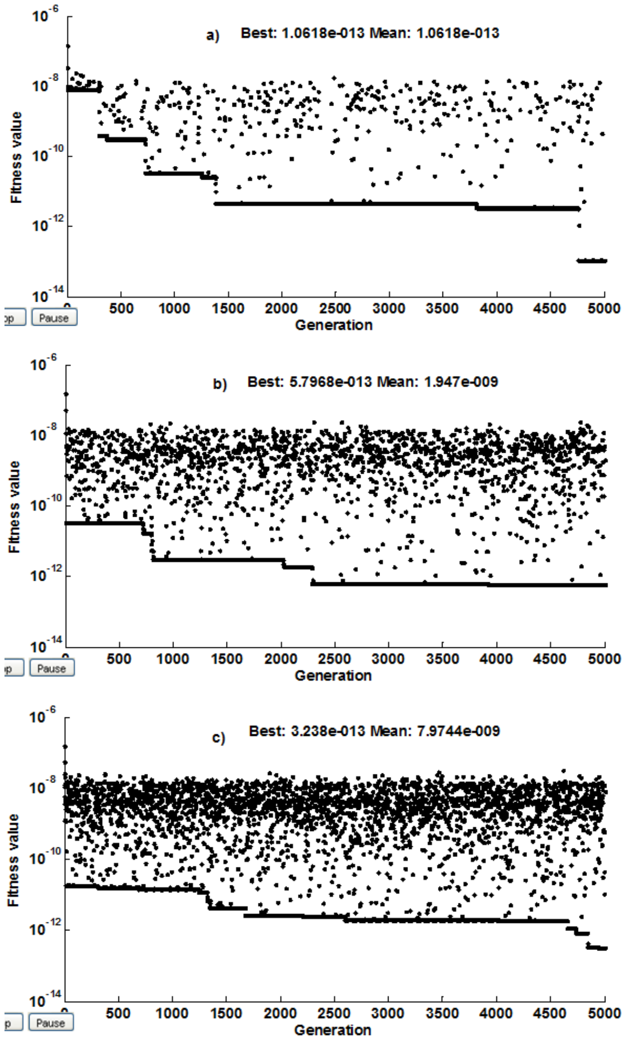

Fig. 7 – Evolution of the fitness function for different mutation rates (population size = 20): a) 0.01, b) 0.05, c) 0.1 (monoclinic-HfO_2 oxide)

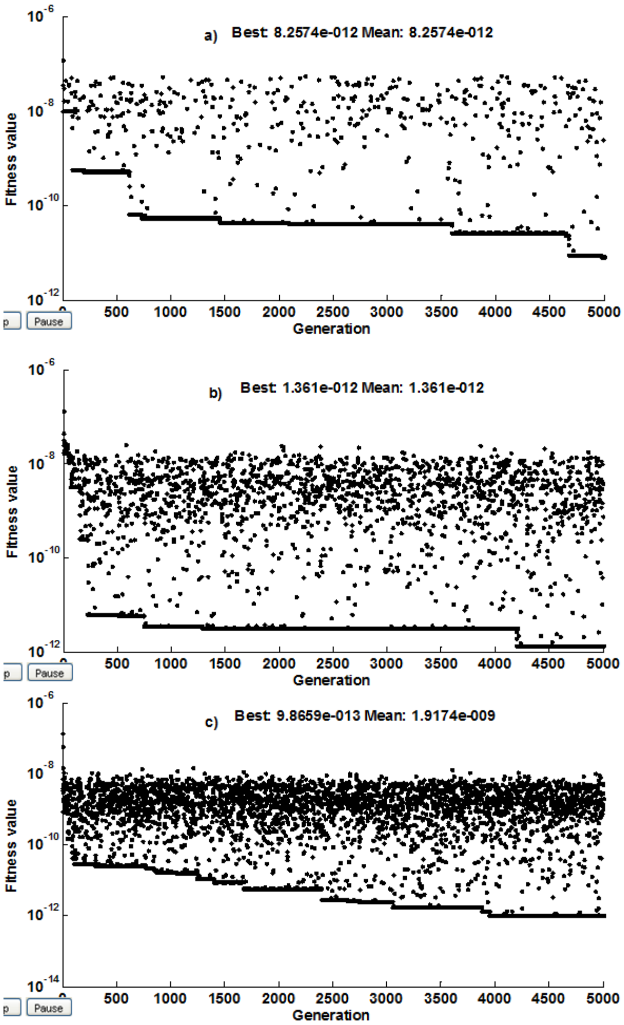

Fig. 8 – Evolution of the fitness function for different population sizes (mutation rate = 0.05): a) 5, b) 20, c) 50, (tetragonal-HfO_2 oxide)

6. CONCLUSIONS

In this paper, the electrical characteristics of a high-*k* MOSFET (HfO_2 oxide) have been optimized and extracted with artificial intelligence (Genetic Algorithm (GA) approach). This optimization method for nano-scale MOSFET devices has been successfully developed. Optimization in electronics solves problems that were previously unsolvable and often leads to original solutions. In this paper, we have demonstrated the optimization by GAs to study nanometer CMOS circuits.

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Моделювання та імітація польового транзистора MOSFET (з high-*k* діелектриком) з використанням генетичних алгоритмів

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Польовий транзистор на основі металу, оксиду та напівпровідника (MOSFET) – це тип польового транзистора; його робота заснована на впливі електричного поля, прикладеного до структури метал-оксид-напівпровідник, тобто до електроду затвора. Це важливий електронний компонент, особливо в мікроелектронній промисловості. З моменту винаходу інтегральної схеми основним напрямом розвитку індустрії кремнієвої мікроелектроніки була мініатюризація MOSFET. Щоб звести до мінімуму небажані ефекти (наприклад, струм витоку) через мініатюризацію MOSFET, було використано кілька рішень для покращення продуктивності MOSFET. Серед цих рішень – використання нових оксидів затвора з високою діелектричною проникністю (наприклад, HfO_2). Нанорозмірний MOSFET є складним електронним пристроєм, тому для його моделювання потрібні нові теорії та методи моделювання (наприклад, штучний інтелект). Генетичні алгоритми (ГА) – це адаптивні метаевристичні алгоритми, засновані на еволюційних ідеях (еволюційних алгоритмах) природного відбору та генетики. ГА використовуються для генерування високоякісних рішень проблем оптимізації та пошуку, покладаючись на такі генетичні оператори, як відбір, кросовер та мутація. У статті описано розширене моделювання (оптимізація), імітація та вилучення параметрів нанорозмірних MOSFET (оксид HfO_2) з використанням підходу ГА. Електричні характеристики MOSFET прогнозуються відповідно до різних параметрів (струм стоку, напруга стоку, напруга затвора, довжина каналу, товщина оксиду).

Ключові слова: MOSFET, HfO_2, SiO_2, Технологія CMOS, High-*k* діелектрик, Штучний інтелект, Генетичні алгоритми.