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Performance Analysis of Gate All Around (GAA) MOSFET at Cryogenic Temperature for the Sub-Nanometer Regime

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In this work, an *n*-type gate all around (GAA) MOSFET with various gate lengths from 90 to 12 nm is considered for simulation. The temperature dependent simulation is carried out in order to investigate the electrical characteristics extensively. The temperature range used in this work varies from 6 to 700 K, including cryogenic temperature, and the behavior of the GAA MOSFET as a next generation semiconductor device for quantum computing systems is investigated. The implementation of a hardware-based quantum processor needs the integration of a CMOS controller and read-out interface circuit that will operate at cryogenic temperature (6 K). In this work, we investigate the critical behavior of the drain current at cryogenic temperature and normal room temperature. A comparative analysis is carried out to study the effect of temperature on the device performance. The proposed device at cryogenic temperature can work properly and become a promising device for future quantum computing systems.

Keywords: MOSFET, Cryogenic, CMOS, Quantum processor.

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1. INTRODUCTION

With the continuous downscaling of device dimensions to mitigate the current problems in the semiconductor industry, various device architectures are being implemented [1-5]. Among all those structures, GAA MOSFET has proved itself as the best candidate to overcome the problems raised by device miniaturization [6-9]. Advanced CMOS processes today perform very well not only at room temperature and above, but also at low or cryogenic temperatures. Large-scale integration of spin bits and Cryo-CMOS control circuits plans to take quantum computing to the next level. A low-temperature circuit designed for space applications, ultra-low noise detectors and scientific equipment are the main application to investigate transistors in cryogenic analysis [10-12]. This technique is laborious and expensive as it requires analysis at very low temperatures with more pre-caution. Here, the MOSFET gate length varies from 12 to 90 nm with a temperature change from 6 to 700 K [13-15].

2. DEVICE DESIGN AND SIMULATION

The simulation is carried out using Sentaurus TCAD simulator from Synopsys [16]. This simulator is the industry standard semiconductor simulator that includes quantum corrections. The device under simulation is scaled down from 90 to 12 nm in order to study the behavior more accurately. As the device size is scaled down to 12 nm, apart from the drift diffusion model, the quantum potential model is also included. Since we introduced a high-*k* dielectric material as a ferroelectric (FE) material, Si_3N_4 is used as an interfacing layer for bonding silicon and HfO_2. The simulation is carried out by including field-dependent mobility in addition to velocity saturation and concentration dependent models available in Sentaurus TCAD from Synopsys. As the temperature variation is carried out in order to perform cryogenic temperature analysis, the temperature dependent SRH model is also included.

Fig. 1 shows a bird eye view of the proposed structure and doping concentration in the source, drain and channel region. The doping concentration in the source and drain was kept at 1e+20, and in the channel – 1e+16.

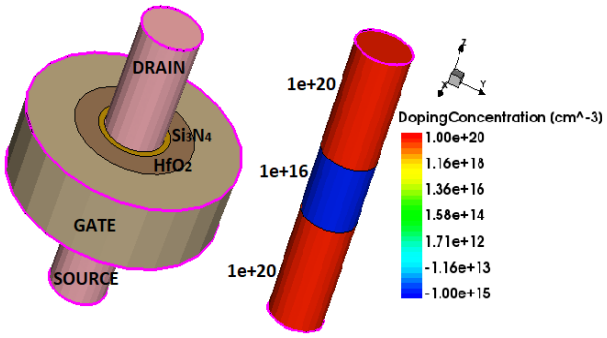

Fig. 1 – Bird eye view of the proposed structure: (a) 12 nm gate length, (b) doping concentration in the source, drain and channel region

3. RESULTS AND DISCUSSION

Fig. 2 shows the electron mobility (eMobility) of the proposed structure for a gate length of 1 nm with a temperature of 30 K. From the figure the variation of electron mobility is clearly observed. This variation is observed for two different gate voltages (V_{GS} = 0.2 V and 1.0 V) for temperatures of 30 K and 300 K, respectively. With increasing gate voltage, the distribution of electron mobility can be observed from the legend attached to the figure. However, with increasing temperature (room temperature and above), the electron mobility decreases, as shown in Fig. 2b.

Similarly, the electron mobility for the 90 nm GAA MOSFET is also observed, and it also provides the same trend as the 12 nm GAA MOSFET. With increasing temperature, the mobility decreases, as shown in Fig. 3.

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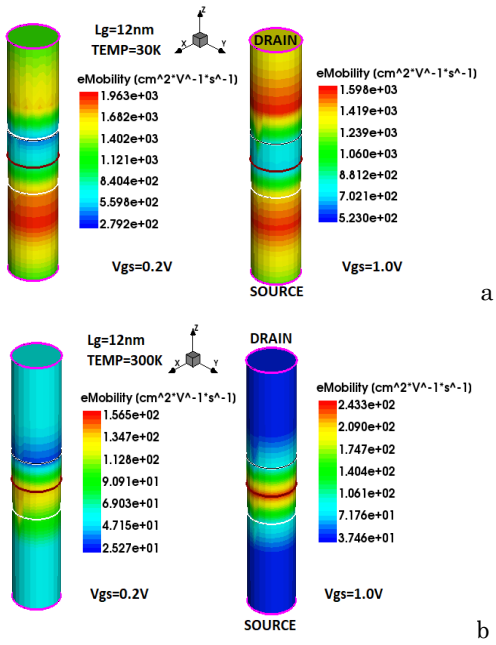


Fig. 2 – Electron mobility (eMobility) for the 12 nm MOSFET at temperatures of 30 K (a) and 300 K (b)

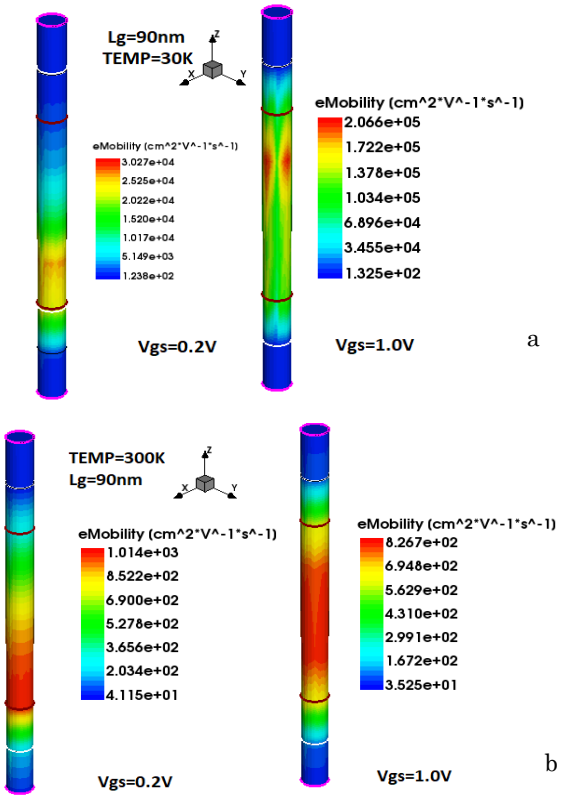


Fig. 3 – Electron mobility (eMobility) for the 90 nm MOSFET at temperatures of 30 K (a) and 300 K (b)

The electrostatic potential distributions of the proposed structure at 12 nm and 90 nm are shown in Fig. 4 and Fig. 5, respectively. The potential distribution on the channel surface can be observed from the cut section of the channel with the legend. The developed potential through the channel can be observed as V_{bi} (built in potential) on the source side and $V_{bi} + V_{ds}$ on the drain side. At low temperatures, still a potential

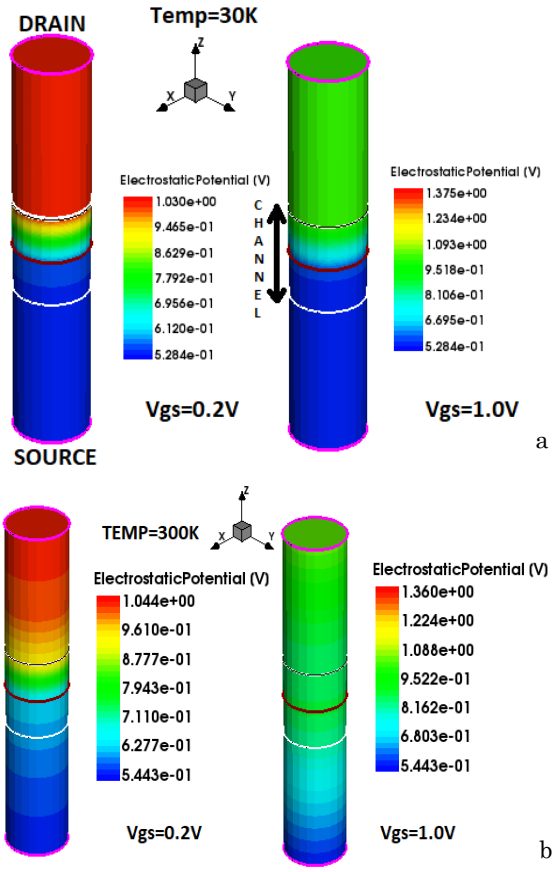
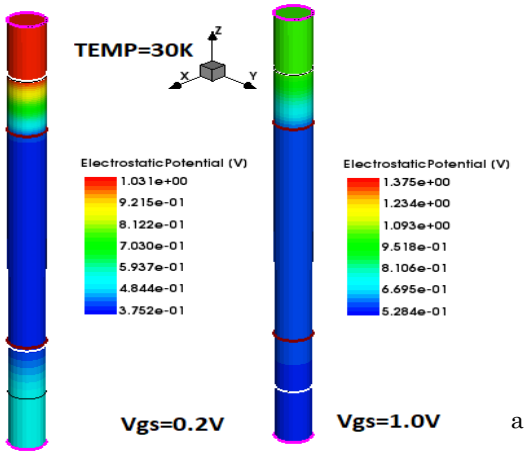


Fig. 4 – Electrostatic potential distribution for the 12 nm MOSFET at temperatures of 30 K (a) at 300 K (b)

difference exists at the source-channel or drain-channel interface, but at high temperatures, the potential through the channel is almost equal, as shown in Fig. 4b.

The trend can be more clearly visible for the 90 nm device, as shown in Fig. 5. At higher temperatures and a gate voltage of 1 V, the potential through the channel is almost equal, as shown in green (Fig. 5b).

The analysis then extends to cryogenic temperature based investigation for quantum computing systems, so the temperature varies up to 6 K and the corresponding drain current is shown in Fig. 6. From the figure, it can be observed that the drain current decreases with decreasing temperature for a lower value of temperature, which is indicated by the arrow in Fig. 6.



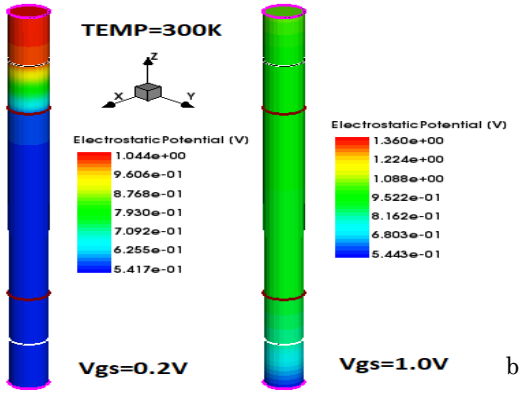


Fig. 5 – Electrostatic potential distribution for the 90 nm MOSFET at temperatures of 30 K (a) and 300 K (b)

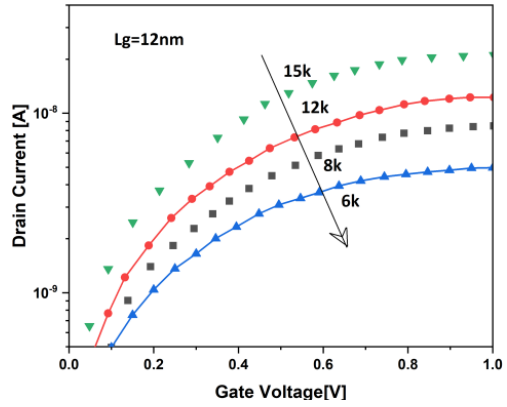
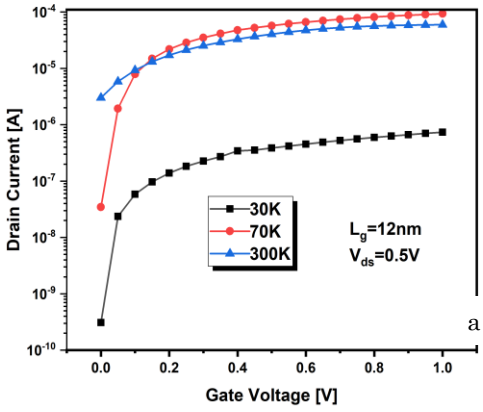


Fig. 6 – Drain current analysis at different cryogenic temperatures for quantum computing

The transfer characteristic of the proposed structure in logarithmic scale is shown in Fig. 7. From the figure, it can be observed that for a lower temperature value (30 K), the drain current is small compared to the other two (70 K and 300 K). This clearly indicates that at low temperatures, the current decreases with decreasing temperature.

However, it is totally different if the temperature increases from lower to room temperature and above. In this case, with increasing temperature, the drain current decreases, as shown in Fig. 7 for 12 nm and 90 nm, respectively. For a device with a long channel at low temperatures, the off-state current becomes better compared to higher temperatures, which is a good sign for switching and other applications.



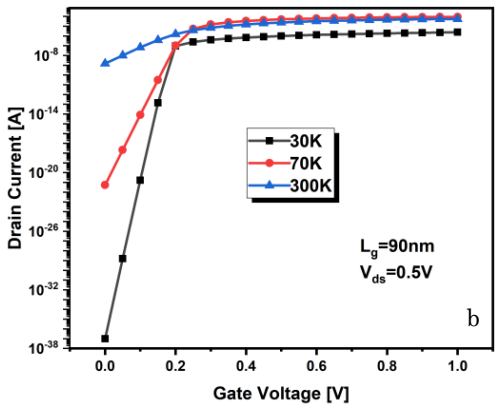


Fig. 7 – Drain current analysis at different temperatures for (a) lower gate length (12 nm), (b) higher gate length (90 nm)

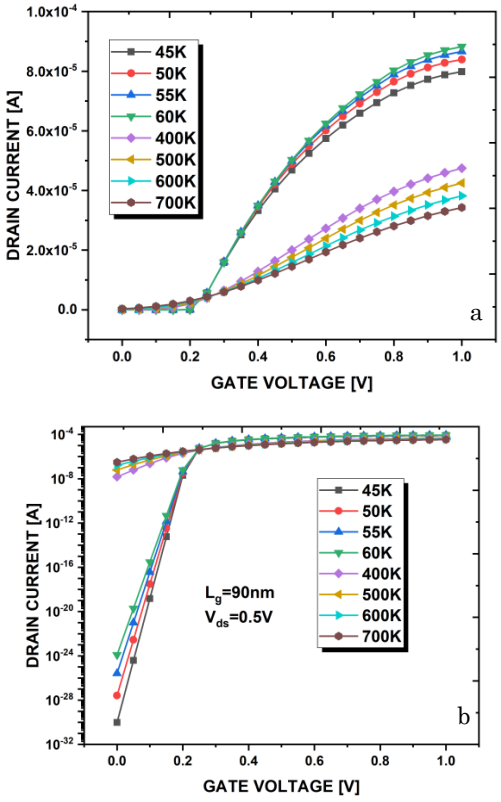


Fig. 8 – Drain current analysis for different temperatures in (a) linear scale, (b) logarithmic scale

In order to show the same thing in a single graph, the transfer characteristic of the proposed structure is depicted from a temperature of 45 to 700 K, and the result thus obtained is shown in Fig. 8 in linear and logarithmic scale, respectively. From Fig. 8a, it can be seen that at a lower temperature, the drain current decreases (45 K) compared to 60 K. However, with an increase in temperature (> 300 K), the drain current decreases gradually. From Fig. 8b, it can be observed that at a lower temperature, the off-state leakage current is better that leads to high I_{on}/I_{off} ratio.

4. CONCLUSIONS

In this work, a comparative study was carried out to investigate the effect of temperature on device perfor-

mance. In addition, the study included cryogenic temperature to examine the device performance as a potential candidate for quantum computing systems. With improved drain current and better off-state current, the proposed device at cryogenic temperatures can operate properly and emerge as a cutting-edge device for future quantum computing systems.

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Аналіз продуктивності GAA MOSFET при кріогенній температурі для субнанометрового режиму

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У роботі розглядається GAA MOSFET *n*-типу з різними довжинами затвора від 90 до 12 нм. Температурно-залежне моделювання проводиться з метою детального дослідження електричних характеристик. Діапазон температур, використаний у роботі, варіюється від 6 до 700 К, включаючи кріогенну температуру, і досліджується поведінка GAA MOSFET як напівпровідникового пристрою наступного покоління для квантових обчислювальних систем. Реалізація апаратного квантового процесора потребує інтеграції CMOS-контролера та схеми інтерфейсу зчитування, яка працюватиме при кріогенній температурі (6 К). У роботі досліджується критична поведінка струму стоку при кріогенній температурі та при нормальній кімнатній температурі. Проводиться порівняльний аналіз для вивчення впливу температури на продуктивність приладу. Запропонований пристрій при кріогенній температурі може працювати належним чином і стати передовим пристроєм для майбутніх квантових обчислювальних систем.

Ключові слова: MOSFET, Кріогенний, CMOS, Квантовий процесор.