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Evaluation of Device Fabrication from FET to CFET: A Review

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Semiconductor industry is advancing day by day to meet the needs of society. As technology grows, the transistor density in an IC increases to augment the performance keeping down the size. Due to the miniaturization of transistors over the past decades, technological progress is in great demand. Vigorous scaling of a planar MOSFET has outaged its nanoscale era due to significant complications associated with increased parasitic capacitance, subthreshold leakage current, thinner gate oxides, which led the researchers to develop and innovate new devices with improved efficiency at low power parameters and reduced short channel effects (SCEs). In this review article, recent technological demand for FETs with multiple gates has been explored and reviewed with advancements. Devices with multiple gates show better performance than conventional FETs due to their steep subthreshold slope, lower leakage current and excellent electrostatic properties even in nanometer regime channel lengths. A triple gate FET and a gate all around FET further improve gate control over the channel. Using FinFET based multi-gate technology, gate control over the channel charge could be increased along with a reduction in parasitic capacitances. To explore the discontinuity of research, the challenges of FinFET technologies have also been addressed along with the introduction of emerging devices. Nanosheets and forksheets address these problems well, as gate structures are stacked on top of each other to form a multiple gate structure that supports enhanced gate control over the channel, whereas C-FET introduces 3D scaling by 'folding' the *n*FET on top of the *p*FET by exploiting the full edge possibilities of device scaling in 3D.

Keywords: Field effect transistor, CMOS, Fin-FET, CFET, Short channel effects, Fabrication.

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1. INTRODUCTION

The invention of vacuum tubes is what launched the electronics industry. Such systems will regulate the movement of electrons in vacuum. After World War II, however, it was found that the complexity and power consumption of these devices increased dramatically due to an overwhelming number of discrete components. As a result, the performance of devices would continue to decline. One example is the Boeing B-29 which consisted of 300-1000 vacuum tubes during the war. Each additional component would reduce the reliability and increase troubleshooting time.

A breakthrough came in 1947, when John Baden, William Shockley and Walter Brattain of Bell labs unveiled the first functioning point-contact germanium transistor. In 1950, Shockley developed the first Bipolar Junction Transistor (BJT). In comparison to a vacuum tube, transistors are more reliable, power efficient and smaller. A transistor is a 3-terminal device which can be viewed as an electrically controlled switch. One of the terminals acts as a control terminal. Ideally, if current is applied to the control terminal, the device will act as a closed switch between the two terminals, which otherwise behave as an open switch. In 1958, Jack Kilby of Texas Instruments built the first Integrated Circuit (IC) consisting of two bipolar transistors connected on a single piece of silicon, thereby initiating the "Silicon Age". Early ICs used BJTs. One of the drawbacks of BJTs is the problem of higher static power dissipation. This means that power is consumed even when the circuit is not switched. This limits the maximum number of transistors that can be integrated into a single silicon chip.

In 1963, Frank Wanlass and C.T. Sah of Fairchild unveiled the first logic gate, in which *n*-channel and *p*-channel transistors were used in a complementary symmetric circuit configuration. This is what is known as CMOS today. It draws almost zero static power dissipation. Early ICs used NMOS technology, because the NMOS process was simple, less expensive and more devices could be packed into a single chip compared to CMOS technology. The first microprocessor was announced by Intel in 1971.

As static power dissipation of an NMOS transistor is greater than that of a CMOS, power consumption of ICs became a serious issue in the 80s, when thousands of transistors were integrated into a single chip. Due to features like low power, reliable performance and high speed, CMOS technology would adopt and replace NMOS and bipolar technology in almost all digital applications. Throughout the next few years, CMOS scaling and improvement in processing technologies have led to continuous enhancement in circuit speeds, along with further improvement in packaging densities of chips and performance-to-cost ratios of microelectronics-based products.

Since the semiconductor technology is advancing,

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the electronic device structures are downscaling day by day. The consequences of the device scaling reduce the controllability of the gate over the channel charge, and the disrupted charge flow through the channel causes the short channel effects (SCEs) [1]. The impact of SCEs deteriorates the device performance and makes it unsuitable for scaling down below 20 nm. To increase gate controllability over the channel charge, semiconductor technology moves towards multi-gate MOSFETs.

Semiconductor industry has shown the vigorous advancements with the introduction of MOSFETs into the industry. To cope up with the requirements of semiconductor industry, MOSFETs have been subjected to rigorous scaling. In the early era of scaling, it focused on reducing the physical channel length, encouraging the shrinking of dimensions. But this geometric scaling only saved the industry for 3 decades (IRTS) in the mid-90s with the drawbacks of SCEs [1]. Beyond the progress of technology roadmap, as CMOS scaling has reached the limit of achieving high performance in trade off with cost, some versions of emerging devices have led the in-dustry to continue to rapidly improve performance, cost per function, reduce power dissipation, and increase functional density. Technological advances such as DG MOSFET (double-gate MOSFET, also known as FinFET) and CNFET (Carbon Nanotube Field Effect Transistor) are promising technologies of choice to replace classical CMOS at the nanoscale level and enable vertical stacking and 3D technology to meet everyday's needs.

This paper briefly discusses different technologies that are evolving because of MOSFET scaling.

2. SILICON ON INSULATOR

Silicon on insulator (SOI) has been in this race for nearly two decades [2]. But due to uncertainty and poor performance, along with the continued scalability of conventional MOSFETs in the early stages of development, SOI was of little interest in the semiconductor industry. When SOI transistors started to emerge, they could perform better than classical transistors [3].

With the inception of Unibond and smart cut technology [4, 5], the possibility of manufacturing 300 mm SOI wafers became a reality [4]. Extensive research on ultra-thin body (UTB) SOI MOSFETs [5] has increased the development of SOI-based devices replacing classical MOSFETs. The conventional SOI structure is similar to the classical MOSFET structure, except for the difference that the buried oxide is incorporated into the silicon substrate. To minimize capacitance at junction, the oxide is placed beyond the diffusion depth to improve the switching speed of CMOS circuit devices.

Different types of SOI transistors are partially and fully depleted (PD and FD), as illustrated in Fig. 1a and Fig. 1b, respectively. In a PD SOI transistor, the gate depletion width is thinner than that of the silicon body, and hence the depletion layer covers the region under the gate only partially, whereas in the FD structure, the silicon layer thickness is comparably smaller than the depletion width or sometimes equivalent; and hence it was named as FD SOI.

PD SOI shows a reduction of about 50 % in power dissipation and an increase of about 20 % in performance compared to a conventional MOSFET [6]. On a silicon layer 45 nm thick, a 33 nm FET is fabricated with performance improvement of about 25 %, as reported in [7]. SOI structures are less prone to soft errors in storing digital data.

SOI also reported elimination of reverse body effects in stacked digital circuit applications [8], which gives an additional advantage when choosing SOI over classical MOSFETs.

The floating body effect is the major drawback of PD SOI, which is reported as the main source of major unwanted properties of SOI such as unstable threshold voltage (variation of dynamic VT) because of the fact that it has variation in the substrate-source voltage [3]. In the saturation region, a sudden increase in drain current, often termed as a "kink effect" [9], and delay variations in circuits, caused by the switching memory effect, are some of the drawbacks of SOI. The floating body effect can be reduced by creating a body contact [10], whereas creating a body contact is critical for manufacturing. As an alternative approach, the thickness of silicon is reduced, resulting in the development of a structure called FD SOI [11].

FD SOI uses an ultra-thin layer of silicon over the buried oxide to reduce leakage currents. FD SOI also boasts a back-bias feature. As FD SOI has a thinner silicon layer than that of the gate depletion width, which is the cause for the absence of a non-depleted substrate, the floating body effect is also reduced to a major extent in FD SOI. The electrical characteristics of bulk MOSFET and FD SOI are investigated to analyze the performance of both structures in [12]. As shown in Fig. 2, fully depleted SOI devices can improve the electrical characteristics like lower threshold voltage, steeper subthreshold swing, lower leakage current, better DIBL, good I_{on}/I_{off} than bulk MOSFETs.

The results acquired in [12] reported that FD SOI has a lower threshold voltage compared to bulk-Si MOSFET. As SOI is fully depleted, the drain to substrate capacitance is negligible, as a result no latch up condition exists. At the same time, SOI also shows the performance improvement in switching speed because of the low threshold voltage due to positive body bias. The leakage current of a FD SOI MOSFET is also reported smaller than that of bulk-Si MOSFET.

At deeper scaling levels, a single-gate (SG) device has SCEs which can be addressed by different multi-gate structures like double-gate (DG), gate all around (GAA) and tri-gate (TG) structures. DG MOSFETs are electrostatically superior to SG MOSFETs and can have additional gate length scaling [13].

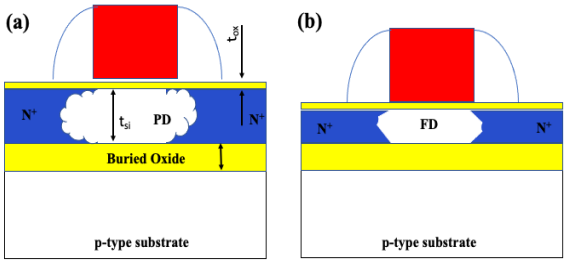

Fig. 1 – Schematic of (a) PD SOI and (b) FD SOI structures. Reproduced from [5]

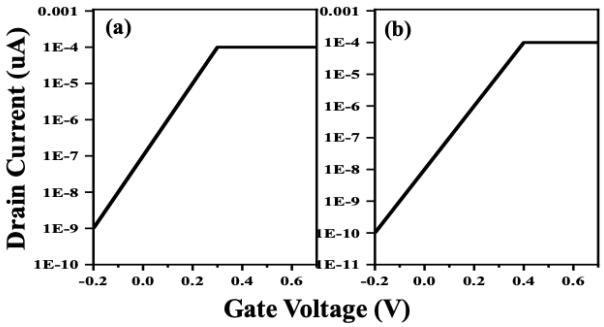

Fig. 2 – (a) I_d-V_g characteristics of bulk n-MOSFET; (b) I_d-V_g characteristics of SOI n-MOSFET. Reproduced from [12]

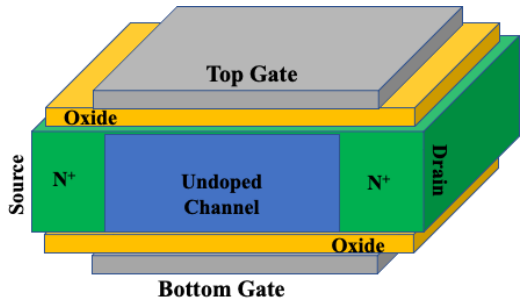

Fig. 3 – General DG MOSFET (DGFET) structure. Reproduced from [14]

The DG transistor is one of the most prominent devices for extremely scaled CMOS technology generations [14]. Indeed, due to good electrostatic control over the channel by the two gates, it is expected to have decreased SCEs, higher drive currents and near-ideal subthreshold slopes when compared to SG transistors [15]. The basic structure of a DG MOSFET is shown in Fig. 3. Among all DG architectures, planar devices are promising: their process is closest to the bulk one, it is easy to combine several architectures, and both gates can be independently biased, which provides greater functional flexibility [16].

A DG MOSFET has two gates located at the bottom and top of the channel in an ultra-thin body, the presence of two gates allows to achieve well-defined gate control over the channel and improve the drain-to-source ON-state current. It also reduces the leakage current occurring in the OFF state, decreases SCEs and reports a comparably good on-off ratio than classical MOSFETs [18].

The DG MOSFET is better than a Single Gate MOSFET (SG MOSFET) electrostatically because of the existence of two gates which controls the channel from both sides. The two gates together can control roughly twice as much current as a single gate, resulting in stronger switching signals. One half of the device is controlled by each gate and the operation is independent of the other. The current flow through the channel is determined by controlling the electric field through the voltage applied to the gate. This gives the ideal subthreshold slope for suitable sub-threshold operation. Hence, DGFETs can be operated at much lower voltages [26, 27].

As a DG MOSFET has twice the current driving capability of a classical CMOS, it can be operated with less threshold voltages and lower inputs [18]. The relative scaling advantage of the DG MOSFET is about double. As two gates allow better control of the channel as compared to a single gate, the threshold voltage will be low at low dimensions, and they can be operated in a low-voltage range. This voltage range can be ineffective in switching MOSFET ON or OFF, a DG MOSFET allows better control of this. SCEs in a DG MOSFET decrease, allowing the gate length to be scaled down to 10 nm.

The main idea of a DG MOSFET (DGFET) is to have Si channel of very small width and to control the Si channel by applying gate contacts to both sides of the channel. The DG concept is borrowed from FD SOI structures [19]. If the buried oxide thickness decreases to that of the gate dielectrics and if the ground plane is electrically connected to the transistor gate, then the ground plane acts as the second gate. The DG structure consists of a conducting channel, usually undoped, surrounded by gate electrodes on either side. Various structures of DGFETs are possible: a) planar (gates and channel are horizontal), b) vertical (conduction direction is vertical), and c) FinFET (channel is vertical; conduction is parallel to the wafer surface) depicted in Fig. 4.

In DG MOSFETs, two different modes of operation are possible depending on their work function due to the two-gate structure.

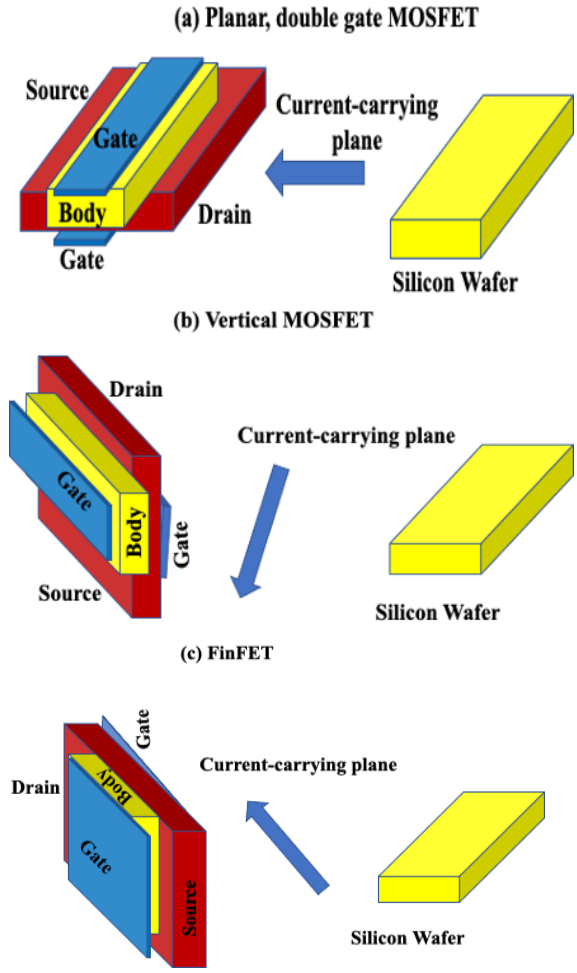

Fig. 4 – (a) Planar DG MOSFET; (b) vertical MOSFET; (c) FinFET (MOSFETs with vertical and horizontal channels – potential advantages for RF Enrico Gili). Reproduced from [20]

Symmetric DG (SDG) MOSFET. When both gates have identical material or work function, then the structure is known as symmetric DG MOSFET. Both gates are connected exactly with same bias. In the on-state, two conducting channels (inversion layers) are framed on two sides of the silicon body in the SDG device [20]. In the meantime, both channels are on. Also, the SDG device shows higher carrier mobility because of its lower transverse electric field compared to the ADG gadget.

Asymmetric DG (ADG) MOSFET. In asymmetric DG MOSFETs, both gates have completely different materials or work functions. These have two different work functions of both gates. DG MOSFET switching can be obtained by applying different voltages to both gates [20]. Just a single channel is made for the ADG device unless the operation voltage is high to form another reverse layer near the P^+ gate. The threshold voltage of an ADG MOSFET can be balanced by changing the body thickness (T_{si}) along with the gate oxide thickness (T_{ox}), without the requirement for extrinsic gate materials.

Major compact modelling work is focused on symmetric and undoped DG MOSFET devices [21]. But the real devices are lightly doped, about $1015\ cm^{-3}$, and asymmetric in nature. In numerical simulation [21], it becomes clear that even a low doping density of $1015\ cm^{-3}$ could cause a large surface potential shift. From the point of view of compact modelling, even millivolt range error is not acceptable for the surface potential. There are a limited number of asymmetric DG MOSFET models [21]. Although the real device asymmetry is due to different oxide thicknesses, flat band voltages and applied gate voltages at the two input gate terminals, most compact models usually consider the asymmetry arising only from different flat band voltages and oxide thicknesses at the two gates.

A projection of the I_D-V_{GS} characteristics of SG and DG FETs is shown in Fig. 6a. The DG FET provides a sharper slope resulting from the advantage of gate coupling, which also gives a lower threshold voltage for a given off-current. This, in turn, gives higher drive currents at lower power-supply voltages. It is clearly evident from Fig. 6b for shorter channel length that the DIBL and subthreshold swing for the DG device are significantly improved relative to those of bulk silicon (Nowak et al., 2004) [22].

3. VERTICAL DG MOSFET

The vertical MOSFET is an attractive alternative to the planar DG MOSFET. The name 'vertical' comes from its current direction, which flows vertically from drain to source, in contrast to the planar structure, whose current flows horizontally, parallel to the surface plane. This structure offers several advantages, ultimately as it relies on a lithography-independent process for channel determination while keeping compatibility with conventional processing [23]. The minimum channel length is controlled by non-lithographic methods (ion implantation or epitaxial growth) in a vertical DG MOSFET, but whereas in a planar DG MOSFET, the minimum channel length (L) depends on the minimum feature length achievable with photolithography. It also makes the implementation of a DG easier, which can lead to higher drive current and higher packing density.

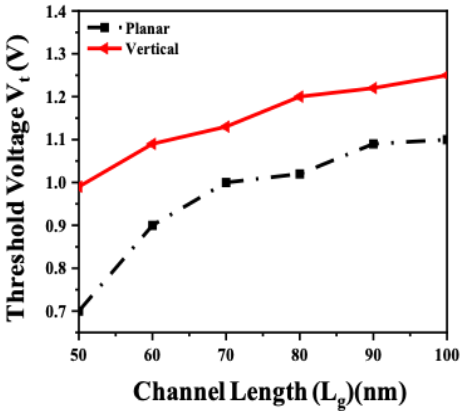

Fig. 5 – (a) V_t roll-off characteristics and threshold voltages, (b) drain leakage current I_{off} for planar and vertical MOSFETs. Reproduced from [23]

A comparative analysis of vertical and planar MOSFETs is reported in [23]. The results show that sharp V_t roll off occurs in a planar device compared to a vertical device as shown in Fig. 5a. This is because the DG has two gate structures on either side of the vertical channel that gives good electrostatic control over the channel even at scaling levels down to 50 nm. It is also reported that I_{off} is reduced in a vertical MOSFET compared to a planar MOSFET, as represented in [23].

The vertical structure offers several advantages as well as challenges over the conventional/planar structure, according to published results. The main advantage is the possibility to further downscale the device with relaxed lithography for channel length definition. The channel length definition of vertical MOSFETs is achieved using careful layer deposition or other thin film definitions, in which lithography is not very critical [38, 39]. Another advantage of a vertical MOSFET is that it can decrease the required space, depending on the application, and the channel width is doubled per the transistor area. In vertical MOSFETs, the gate length is controlled by non-lithographic methods; this allows the fabrication of sub-100 nm channel length devices with relaxed photolithography rules, reducing the cost. Better control of the substrate depletion region in thin FD pillars reduces SCEs and parasitic capacitances [23].

The output characteristics, threshold voltage, DIBL and subthreshold swing (S) of vertical DG MOSFETs with different channel lengths are reported in [24].

The major drawback of vertical DG MOSFETs is that an ultrathin Si channel is extremely difficult to produce on a bulk substrate [23].

4. FinFET TECHNOLOGY

Headers FinFET devices were proposed as the most likely candidates to substitute bulk MOSFETs for ultimate scaling [25]. FinFET devices can be employed with either two gates tied together (three-terminal (3T) structure) or two independently biased gates (four-terminal (4T) structure) [25]. ITRS proposed multi-gate

FETs such as planar DG FETs and FinFETs as a possible scaling path to improve performance and low power CMOS technology [26]. A distinctive feature of a FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The effective channel length of the device depends on the fin thickness (measured in the direction from source to drain). It is the predominant successor to a SG MOSFET because of its better electrostatic properties and ease of manufacture as compared to classical MOSFETs. Although early DG FETs presented manufacturing challenges associated with vertical structures, DG devices called FinFETs or wraparound FETs that are compatible with conventional CMOS in most processing steps have been demonstrated [27].

Normally, the DG structure is used to decrease SCEs, OFF drive current and threshold voltage. Three different DG architectures were used and compared to increase the performance of device. Overall, DG FinFET structures are preferred as they are more area efficient and less complicated than planar and vertical DG MOSFETs [28].

Source/drain series resistance and mobility are found to be higher whereas saturation velocity is less in FinFETs [28]. Voltage gain is also higher in FinFETs as compared to bulk MOSFETs. The fin width is an important parameter to reduce SCEs and it also helps in scaling down the gate length even further. Parasitic capacitance in FinFETs is again an important factor which is responsible for decreasing device performance.

The dependence of parasitic capacitance on geometry is also considered to be a factor which affects during scaling down [29]. The FinFET structure is used to reduce SCEs which occur due to scaling down the node. The fin thickness (corresponding to twice the body thickness) is found to be critical for suppressing SCEs [30]. The relation between the silicon fin thickness and the subthreshold swing is used to increase the performance of the device. The fin thickness can also adjust to improve subthreshold swing. FinFET used shows a very high drive current and good short-channel behavior down to a gate length of 18 nm [30].

The transfer characteristics of the InGaAs FinFET that are modeled with the BSIM-CMG model are shown in Fig. 9 in semi-log (left) and linear (right) scales, showing the subthreshold, as well as strong inversion region drain-current model, reported in [31].

FinFETs are easier to fabricate than lateral DG FETs. In the vertical and fin geometries, the body thickness is controlled by lithographic and etching processes, respectively. The gates should be precisely aligned (to within one quarter of the gate length), to avoid compromised performance [32].

The feature of self-alignment between the gates is easier to implement with FinFETs, but harder to make in lateral DG FETs. On the other hand, lateral DG FETs and FinFETs depend heavily on lithography in defining the channel length, so the critical problem in lithography has a greater impact on further device design.

4.1 FinFET Technology

TG MOSFETs are immune to SCEs, exhibit excellent stability, and have comparatively less DIBL [31]. They also provide higher drive current with lower leakage current [32]. Control over SCEs has always been one of the challenging issues [32]. TG transistors favor an increase in currents per chip area. Due to the maximum ON currents, TG FETs appeared to be attractive. The source and drain proximity and the reduction of the gate length result in a decrease in gate control over the channel.

By enclosing the gate geometrically close to the channel, improved control over the channel can be achieved, resulting in a tighter gate coupling. The ultra-thin body that resembles a fin structure supports closer enclosing of the gate towards the channel, and the increase in the number of gates from SG to multi-gate supports a tighter gate coupling [32].

TG provides flexible body dimension by relaxing the requirements for fin thickness and fin height, and also achieves good fin aspect ratio. The presence of TG increases effective gate control there by reducing the DIBL. It also reduces mobility degradation since the channel is undoped or very lightly doped, and hence increases the I_{on}/I_{off} ratio and performance, thereby making it suitable for low power applications [32].

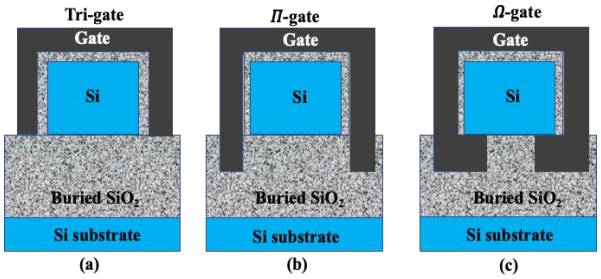

Fig. 6 – Different structures of FETs: (a) tri-gate (TG) FET, (b) π-gate FET, (c) Ω-gate FET. Reproduced from [27]

There are different structures of TG FETs reported in [27], as shown in Fig. 6. One of the most important multi-gate structures is the Pi-gate SOI MOSFET because it combines good subthreshold characteristics with high ON currents and is a very good alternative to planar devices.

The Pi-gate SOI MOSFET has great potential to replace current devices due to its geometry that is a partway between TG and DG devices [33]. The gate goes down into the buried oxide, allowing more effective control of the electrostatics in the channel region and shielding it from electric-field lines arising in the drain when the width of the devices is small enough [33].

The Pi-gate structure as shown in Fig. 7 is a TG MOSFET where the gate electrode extends to some depth in the buried oxide on both sides of the device. The gate is in the shape of the uppercase Greek letter Pi. The gate extension in the buried oxide shields the back of the channel region from electric field lines from the drain almost as well as an actual back gate. Unlike the DG or GAA structure, however, the Pi-gate SOI MOSFET can readily be manufactured, since it merely requires the addition of masking and the RIE buried oxide etch step to the conventional SOI CMOS fabrication process [33].

Ref [34] shows the DIBL and the threshold voltage roll-off in a FD SOI MOSFET with different gate struc-

tures and different effective gate lengths. DIBL is defined as the difference in threshold voltages when the drain voltage is either 0.1 or 1 V.

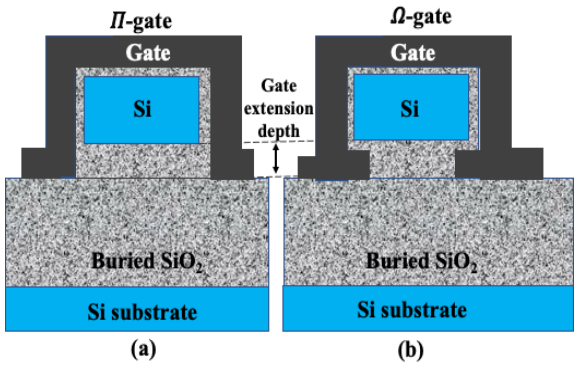

Fig. 7 – P-gate (Pi-gate) and X-gate (Omega-gate) MOSFET cross-sections. Reproduced from [33]

The silicon substrate under the buried oxide is always kept grounded. DIBL is most effectively suppressed by the four-gate structure, but the Pi-gate device is second. Similarly, it can be observed that the threshold voltage roll-off is minimized using the four-gate structure, but the Pi-gate device shows an excellent behavior as well. The DIBL and threshold voltage roll-off characteristics of the SG device are not shown in this graph because they are much larger than those of other devices. In Ref [34], the subthreshold swing in fully depleted SOI MOSFETs with different gate structures and gate lengths for a drain voltage of 100 mV. The silicon substrate under the buried oxide is kept grounded at all times. The degradation of the four-gate structure is the smallest and, once again, the Pi-gate device exhibits a degradation very close to that of the four-gate device. It has been reported [34] that the characteristics of a Pi-gate device with a zero-gate extension in the buried oxide are identical to those of a TG MOSFET.

4.2 GAA FETs

As we move towards nanoscale technology, the transistor density increases. So, downscaling of transistors is required, but reducing the transistor size leads to degradation of the device performance. This degradation is due to SCEs such as subthreshold current, DIBL, etc. Several structures such as DG and TG transistors have replaced MOSFETs. GAA structures have shown the advantage of strong gate control over the channel in contrast to multi-gate FETs. It has the highest conductivity and electrical properties.

Basically, in GAA MOSFETs, as shown in Fig. 8, the gate is wrapped all around the channel. With all-around covering of the gate over the channel, it is a promising structure for better gate control and better short channel performance. There are undoped and doped channels, both types of channels are used in GAA technology. The drain and source terminals are formed at the outer sides of the channel.

Normally, the gate length is defined by the length of the gate material, which is wrapped around the channel, whereas in nanowire technology, the gate length is slightly larger than the channel length, which is called the gate overlap thickness. The gate length also defines the gate controllability over the channel and the effective electric field of the channel. SCEs like subthreshold slope and DIBL are anti-proportional to the gate length as they increase with decreasing gate length. Another parameter like threshold voltage V_t is directly proportional to the gate length as it decreases with decreasing gate length.

Continuous scaling of GAA silicon nanowire FETs has comparably better control over SCEs [34]. A GAA FET with silicon nanowire has good gate controllability, better carrier transport property, high I_{on}/I_{off} ratio and also low leakage which makes it a better option for future electronic systems. Analytical models of GAA FETs for extracting different parameters for devices are described in [35]. The effectiveness of the GAA FET structure can be described by the above models and is reported in [37]. A nanowire FET with GAA structure is fabricated by bottom-up and top-down design [37]. This structure reports better electrostatic control of the gate over the channel that provides high transconductance [39]. GAA MOSFETs report better performance as compared with DG and TG FETs [38]. Simulation and analysis report that GAA configuration provides good performance with respect to SCEs when compared with other structures [39]. Better subthreshold slope and DIBL suppression are an added advantage of GAA structures. Scaling the channel length of MOSFETs to 45 nm restricts static power consumption due to increased leakage in the OFF state [37].

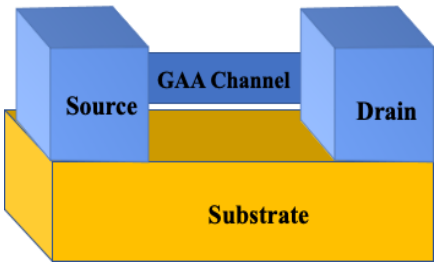

Fig. 8 – Gate-all-around (GAA) MOSFET. Reproduced from [34]

As scaling goes beyond 5 nm, the above discussed structures are expected to run out of steam. At reduced gate length, even FinFET structures fail to provide enough electrostatic control. On top of that, the evolution to standard cells with a lower track height requires a transition to single-fin devices, which cannot provide enough drive current even if the fin height further increases.

Vertically stacked nanosheet transistors can meet the needs of today, which can be seen as a natural evolution of the FinFET device. Just imagine placing a FinFET on its side and dividing it into separate horizontal sheets, which make up the channels. The gate now fully wraps around the channel. This GAA nature of a nanosheet provides superior channel control compared to the multi-gate FinFET. At the same time, the more optimal distribution of the channel cross-section in the 3D volume optimizes the effective drive per the footprint.

Research done at IMEC has proved that a nanosheet device shows a 10 % speed gain (at constant power) and a 24 % power reduction (at constant speed)

compared to a FinFET [40]. Contrary to the nanosheet device, the sheets are now controlled by a forked gate structure as shown in Fig. 9, realized by introducing a dielectric wall in between the *p*- and *n*-MOS devices before gate patterning. This wall physically isolates the *p*-gate trench from the *n*-gate trench, providing a much tighter *n*-to-*p* spacing. The process flow used for making the forksheet device requires only few additional steps apart from the steps required to design nanosheet devices. On top of this process window enhancement, the forksheet is expected to have superior area and performance scalability due to the large reduction in *n*-to-*p* separation.

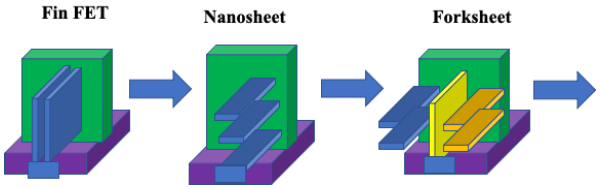

Fig. 9 – Natural evolution from FinFET to nanosheet and to forksheet. Reproduced from [40]

Optimizing routability brings us to the CFET or complementary FET device pushing the horizon for Moore's Law further out. The concept of CFET consists in 'folding' the nFET on top of the *p*FET (either fin-on-fin or sheet-on-sheet) – as such fully exploiting the possibilities of device scaling in 3D. By its stacked nature, the CFET exhibits 2 levels of local interconnects – providing more freedom for internal cell routing and for reducing cell area. Routing between cells can also be largely improved [40].

The forksheet can be considered as the next step in the natural evolution from planar to FinFET and to vertically stacked nanosheets. The above characteristics demonstrate its potential as an ultimate logic 'universal' CMOS device for the 2 nm technology node. In further research, the process challenges to fully bring these devices into production need to be resolved. Routing optimization brings us to the CFET or complementary FET device, expanding horizons for Moore's law.

The concept of CFET (Complementary-Field Effect Transistor) consists in 'folding' the nFET on top of the *p*FET (either fin-on-fin or sheet-on-sheet) – as such fully exploiting the possibilities of device scaling in 3D. By its stacked nature, the CFET exhibits 2 levels of local interconnects as shown in Fig. 9 providing more freedom for internal cell routing and for reducing cell area. Routing between cells can also be largely improved.

The Complementary-Field Effect Transistor (CFET) technology suggests that it is possible to directly fabricate *n*-MOS transistors on top of *p*-MOS transistors or vice-versa. This architecture will require new metal wiring designs and Buried Power Rails (BPR) within the substrate. The design will be disruptive and will require the development of specific new processing steps such as dielectric selective deposition on metal.

5. CONCLUSIONS

The semiconductor industry has been growing since the establishment of CMOS for more than decades. Given the effects of scaling, the industry has shown interest in developing new structures, and has also focused on developing methodologies such as insulating material put under the transistor structure to mitigate some SCEs and reduce parasitic capacitance to respond the scaling limitations. However, the willingness to adapt the new device structures has outraced interest in developing various device methodologies for scaling issues. New device structures like SOI, multi-gate structures, GAA FETs, etc. were discussed.

SOI devices also suffer from SCEs, these effects can be minimized by heavily doping the top of the substrate under the BOX to form a ground-plane electrode. Such an electrode, however, increases the source and drain capacitance to the substrate and may degrade the crosstalk characteristics. FinFETs overcome most SCEs, hence they are not prone to damage or ageing as seen in conventional MOSFETs, and therefore increase reliability and are suitable for producing fast digital logic circuits. They show that improved control over the channel was achieved by surrounding the channel (FinFETs) with a gate stack, getting added benefit of scaling down and no SCEs.

However, FinFET structures could not withstand scaling beyond 5 nm and led to nanosheet devices that opened the path for vertical structures. The technology nodes of 16, 14, and 10 nm are no longer named after the channel length or any other transistor dimension as they previously did, these names are given in ITRS. Nanowires and nanosheets are developed to get the maximum benefit from the MOSFET structure. It is around this development that the track height of standard cells is taken into focus for reduction in chip area, and forksheets track height was used as a scaling knob. Stacking devices allows further downscaling, as demonstrated by the forksheets and CFETs, where the track height of a standard cell is reduced for the first time to achieve scaling.

REFERENCES

1. G.A. Brown, P.M. Zeitzoff, G. Bersuker, H.R. Huff, *Mater. Today* **7** No 1, 26 (2004).
2. M. Bruel, *Electron. Lett.* **31** No 14, 1201 (1995).
3. M. Bruel, *Nucl. Instrum. Meth. Phys. Res. B* **108** No 3, 313 (1996).
4. M. Yoshimi, C. Mazuré, *2004 International Conference on Integrated Circuit Design and Technology (IEEE)* (2004).
5. Y.-K. Choi, D. Ha, T.-J. King, C. Hu, *IEEE Electron Dev. Lett.* **22** No 9, 447 (2001).
6. K. Mistry, G. Grula, J. Sleight, L. Bai, R. Stephany, R. Flatley, P. Skerry, *International Electron Devices Meeting. IEDM Technical Digest* (1997).
7. S. Narasimha, A. Ajmera, H. Park, et al., *International Electron Devices Meeting. Technical Digest* Cat. No. 01CH37224 (2001).
8. K.L. Shepard, D.-J. Kim, *IEEE Trans. Computer-Aided Des. Integrated Circuit. System.* **20** No 7, 888 (2001).
9. K. Kato, K. Taniguchi, *IEEE Trans. Electron Dev.* **33** No 1, 133 (1986).
10. Y. Omura, K. Izumi, *IEEE Trans. Electron Dev.* **35** No 8, 1391 (1988).

11. J.-P. Colinge, *Electron. Lett.* **22** No 4, 187 (1986).
12. D. Ranka, et al., *2011 International Conference on Devices and Communications (ICDeCom)* (2011).
13. S, Chopade, S. Mane, D. Padole, *2013 IEEE International Conference of IEEE Region 10 (TENCON 2013)* (2013).
14. V. Subramanian, *IETE Tech. Rev.* **27** No 6, 446 (2010).
15. F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, T. Elewa, *IEEE Electron Dev. Lett.* **8** No 9, 410 (1987).
16. S. Zhang, X. Lin, R. Huang, R. Han, M. Chan, *IEEE Trans. Electron Dev.* **50** No 11, 2297 (2003).
17. J. Widiez, J. Lolivier, M. Vinet, T. Poiroux, B. Previtali, F. Dauge, M. Mouis, S. Deleonibus, *IEEE Trans. Electron Dev.* **52** No 8, 1772 (2005).
18. T. Sekigawa, Y. Hayashi, *Solid-State Electron.* **27** No 8, 827 (1984).
19. J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors* (Springer: 2008).
20. E. Gili, V.D. Kunz, T. Uchino, M.M.A. Hakim, C.H. de Groot, P. Ashburn, S. Hall, *IEEE Trans. Electron Dev.* **53** No 5, 1080 (2006).
21. S.K. Gupta, *Int. J. Wisdom Based Comput.* **1** No 3, 60 (2011).
22. E.J. Nowak, I. Aller, T. Ludwig, K. Kim, R.V. Joshi, C.-T. Chuang, K. Bernstein, R. Puri, *IEEE Circuits Dev. Magaz.* **20** No 1, 20 (2004).
23. I. Saad, N. Bolong, P. Divya, K.T.T. Kin, *2011 UkSim 13th International Conference on Computer Modelling and Simulation* (2011).
24. T. Schulz, W. Rosner, L. Risch, A. Korbel, U. Langmann, *IEEE Trans. Electron Dev.* **48** No 8, 1783 (2001).
25. M.A. Riyadi, I. Saad, M.T. Ahmadi, R. Ismail, *AIP Conf. Proc.* **1136** No 1, 248 (2009).
26. S. Mukhopadhyay, C. Neau, R.T. Cakici, A. Agarwal, C.H. Kim, K. Roy, *IEEE Trans. Very Large Scale Integration (VLSI) System.* **11** No 4, 716 (2003).
27. G. Shahidi, *IEDM Short Course: Scaling Challenges: Device Architectures, New Materials, and Process Technologies* (Baltimore: 2009).
28. D. Hisamoto, W.-C.Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, C. Hu, *IEEE Trans. Electron Dev.* **47** No 12, 2320 (2000).
29. A.W. Dey, C. Thelander, E. Lind, et al., *IEEE Electron Dev. Lett.* **33** No 6, 791 (2012).
30. P. Verheyen, et al., *IEEE Int. Electron Dev. Meet. Technical Digest* (2005).
31. D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, H.-S. P. Wong, *Proc. IEEE* **89** No 3, 259 (2001).
32. D. Mitra, C. Maiti, *NateHCA*, 57 (2007).
33. J. Conde, A. Cerdeira, M. Pavanello, V. Kilchytska, D. Flandre, *Microelectron. Eng.* **88** No 7, 1633 (2011).
34. S. Bangsaruntip, G.M. Cohen, A. Majumdar, J.W. Sleight, *IEEE Electron Dev. Lett.* **31** No 9, 903 (2010).
35. B. Yu, Y. Yuan, J. Song, Y. Taur, *IEEE Trans. Electron Dev.* **56** No 10, 2357 (2009).
36. N. Singh, K.D. Buddharaju, S.K. Manhas, et al., *IEEE Trans. Electron Dev.* **55** No 11, 3107 (2008).
37. J. Guo, J. Wang, E. Polizzi, S. Datta, M. Lundstrom, *IEEE Trans. Nanotechnol.* **2** No 4, 329 (2003).
38. S.-H. Oh, D. Monroe, J. Hergenrother, *IEEE Electron Dev. Lett.* **21** No 9, 445 (2000).
39. B.S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, R. Chau, *IEEE Electron Dev. Lett.* **24** No 4, 263 (2003).
40. D. Nagy, G. Espiñeira, G. Indalecio, A.J. García-Loureiro, K. Kalna, N. Seoane, *IEEE Access* **8**, 53196 (2020).

Оцінка виготовлення пристроїв від FET до CFET: огляд

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Напівпровідникова промисловість розвивається з кожним днем, щоб задовольнити потреби суспільства. З розвитком технологій щільність транзисторів в мікросхемі зростає, щоб підвищити продуктивність, зберігаючи при цьому розмір. Завдяки мініатюризації транзисторів за останні десятиліття, технічний прогрес не стоїть на місці. Інтенсивне масштабування планарного MOSFET перервало еру нанорозмірних приладів через значні ускладнення, пов'язані зі збільшенням паразитної ємності, підпороговим струмом витоку, більш тонкими оксидами затвора, що спонукало дослідників розробити та впровадити нові пристрої з підвищеною ефективністю при низьких параметрах потужності та зменшеними короткоканальними ефектами (SCEs). У цій оглядовій статті було досліджено та проаналізовано нещодавній технологічний попит на польові транзистори (FETs) з декількома затворами. Пристрої з декількома затворами демонструють кращі характеристики, ніж звичайні FETs через їх крутий підпороговий схил, менший струм витоку та відмінні електростатичні властивості навіть при нанометровій довжині каналу. Польові транзистори з потрійним затвором (TG FETs) і польові транзистори з горизонтальним розташуванням каналів та круговим затвором (GAA FETs) додатково покращують керування затвором у каналі. Використовуючи технологію з декількома затворами на основі FinFET, контроль затвора над каналом може бути покращено разом із зменшенням паразитних ємностей. Щоб вивчити переривання у дослідженнях, проблеми технологій FinFET також були розглянуті разом із впровадженням нових пристроїв. Нанолисти та розгалужені листи добре вирішують ці проблеми, оскільки структури затворів накладаються одна на одну, щоб сформувати структуру з декількома затворами, яка підтримує покращений контроль затвора над каналом, тоді як CFET вводить 3D масштабування шляхом «складання» *n*FET поверх *p*FET, використовуючи всі можливості масштабування пристрою в 3D просторі.

Ключові слова: Польовий транзистор (FET), CMOS, FinFET, CFET, Короткоканальні ефекти, Виготовлення.