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Analysis of Junctionless Nanowire Transistor with Heterojunction, Metal Nitride and Dual Metal Gate

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This paper focuses on the performance of Silicon-on-Insulator (SOI) based junctionless (JL) nanowire multichannel transistor. It has been analyzed with various strains in order to improve the device performance. Instead of one channel, by using the Multi Bridge Channel (MBC) concept, two channels have been incorporated in the JL nanowire structure. Moreover, three methods have been used to improve the JL device. The first one is the Dual Metal Gate (DMG) concept, the second one is heterojunction (silicon carbide (SiC) is used as the source/drain material), and the third one is metal nitride. By using these three methods, mobility has been increased, as well as current drive. The current-voltage (*I-V*) characteristics comparison has been performed between DMG and Single Metal Gate, DMG and Single Metal Nitride gate using Sentaurus Technology Computer Aided Design (TCAD). The results were calibrated using physical models, such as the temperature-dependent carrier transport model (drift diffusion), density gradient model, mobility model, and Shockley-Read-Hall recombination model. By integrating heterojunction into DMG and single metal nitride gate, the performance of both devices has been improved, but single metal nitride gate has shown the 6 % better performance than DMG with heterojunction. In all the devices, the Subthreshold Swing (SS) is almost 60 mV dec^{-1} which is near the ideal value.

Keywords: Junctionless tri-gate, Double-channel, TiN, DMG, Silicon carbide (SiC).

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1. INTRODUCTION

Now a days, researchers are focusing on junctionless (JL) transistors to utilize the benefits because of easy fabrication. The JL principle was eventually used to a variety of devices, including GAA, FinFETs, TFETs, TFTs, double-gate and tri-gate devices. [1]. One of the best ways to improve the performance of JL devices is to induce strain in the channel, which increases the carrier velocity. Without modifying the structure, just changing the materials, it is possible to induce strain. Local strain caused by the gate electrode, substrate strain, and biaxial tensile strain were studied in [2].

SiC was experimentally proven and introduced as a source and drain material creating a heterojunction, which induced horizontal tensile strain and vertical compressive strain in the silicon channel, thus increasing the current drive by 50 % for a gate length of 50 nm [3]. An increase in the current drive was depicted in a 40 nm device using SiC as a source/drain material [4]. Z. Ren [5] in 2008 discussed SiC with phosphorus material doping to increase the current. The efficiency of Si and SiC in terms of radiation was discussed in [6]. Papers [7-9] talk about the functions of heterojunction and the creation of tensile strain in the strained silicon channel. In addition to heterojunction, the use of metal nitride (TiN) induced strain in the gate based on nitrogen level. The poly depletion problem is eliminated when a metal gate is used. By lowering the transverse electric field at a given gate overdrive, it improves carrier mobility. Moreover, based on the thickness of metal nitride, the gate work function can be tuned [10]. Another way to increase the carrier velocity is Dual Metal Gate (DMG) functionality. The gate is made up of two metals with different work functions. Due to the different work functions of metals, the potential step near the junction changes, increasing the carrier velocity, carrier transport efficiency, and drain current [11]. The peak electric field at the drain end is reduced in the DMG structure, resulting in an increase in the average electric field under the gate. This enables improved lifetime of the device [12, 13]. The superiority of HfO_2 dielectric over other oxide layers has been proven in [14, 15] by creating dual metal gates in cylindrical nanowires and analyzing with various gate oxides.

In this work, a SOI based JL nanowire transistor incorporated with different strains induced by different materials has been analyzed. This paper structure is divided into Device Structure, Results and Discussion, and Conclusions.

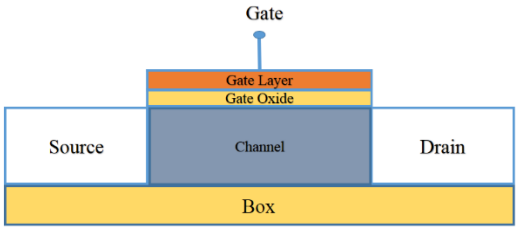

Fig. 1 – JL nanowire transistor [1]

2. DEVICE STRUCTURE

A JL nanowire was created in the TCAD Simulation, as illustrated in Fig. 1, by employing the values from [1]. The channel was surrounded by tri-gate

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electrodes since the device was built on SOI.

The channel thickness and width are 10 nm and 20 nm, respectively, with a gate length of 1000 nm. A uniform doping concentration of $2 \cdot 10^{17}$ is applied to the source, drain, and channel. Both the gate oxide and buried oxide layers were made of SiO_2. V_{GS} was kept at 1.3 V and V_{DS} was kept at 1.5 V to simulate the device. Fig. 2 illustrates that the simulated and experimental results are identical [1].

After validation, the same device was modified with double channel and HfO_2. The second channel was stacked vertically with the same channel thickness and width. Both channels were separated and surrounded by HfO_2 due to suggestion of [14, 15]. The inter-oxide layer thickness of 40 nm was determined after running different thickness values, which are shown in Fig. 3. HfO_2 reduces leakage current and increases current when compared to SiO_2. Polysilicon was used in Fig. 3. In this device structure, first, DMG was implemented as shown in Fig. 4. Single gate was divided into two different metals with different work functions at an equal distance. Metals 1 and 2 were equally divided by 500 nm each, as suggested in [16], and the work function of metal 1 equal to 4.8 eV (gold) and of metal 2 equal to 4.33 eV (titanium) are taken from [17]. Second, in the DMG structure, heterojunction was implemented. To create heterojunction in the device, SiC was used as a source and drain material and silicon as a channel material. In the third method, DMG was replaced with single metal nitride (TiN). So, in this last structure, a heterostructure (SiC in source/drain) with single metal nitride was implemented in a JL nanowire transistor. The fabrication steps were explained in [1, 7-10, 18, 19]. The calibration of results was performed by using physical models, such as temperature-dependent drift diffusion model, density gradient model, mobility and Shockley-Read-Hall recombination model for carrier lifetime [20].

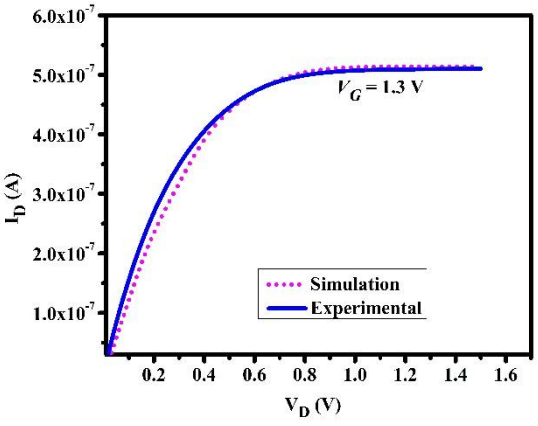

Fig. 2 – Simulation result is validated by [1]

3. RESULTS AND DISCUSSION

3.1 Dual Metal Gate

Fig. 5 depicts the electrostatic potential comparison between single channel with single metal gate (SCSMG), double channel with single metal gate (DCSMG) and double channel with dual metal gate (DCDMG). Among these three, there is a step potential increased near the junction due to the difference in work functions of metals 1 and 2 in DMG.

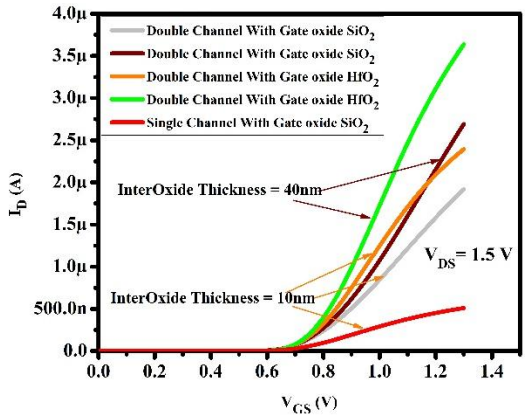

Fig. 3 – Transfer characteristics of DCSMG and SCSMG with different interface oxide thickness

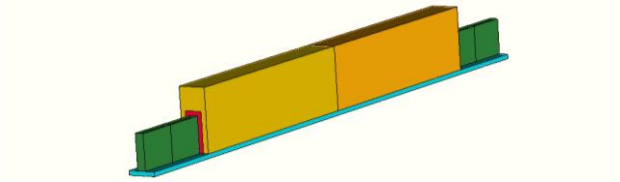

Fig. 4 – DMG formation in TCAD

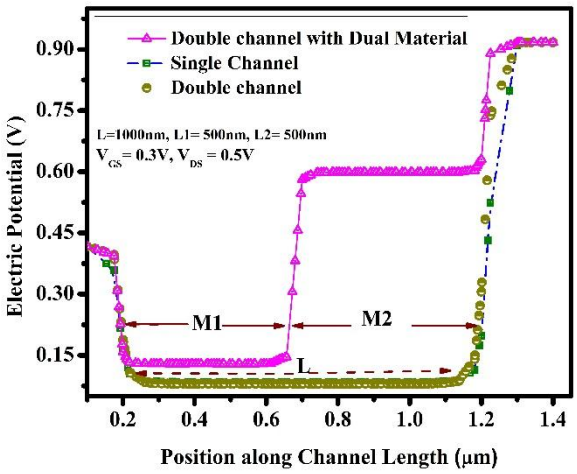

Fig. 5 – Electric potential variation in SMG and DMG

The work function of metal 1 is greater than that of metal 2, according to the relation $WF = -q\Phi - EF$, potential under the gate of metal 1 is lower compared to metal 2. Due to the sudden potential difference across the junction, there is an increase in the average carrier velocity and drain current. Moreover, due to an increase in the electric field peak in the middle of the junction, the electric field on the drain side decreases. So, the hot carrier effect is reduced in the device and the lifetime of the device is increased.

3.2 Heterojunction

The heterojunction was created by replacing Si with SiC at the source and drain in a double channel device with DMG. The bandgap of Si and SiC is 1.1 eV

and 3.26 eV, respectively. According to the heterojunction theory, the conduction band of the source region is higher than that of the channel region, and the band-offset ΔEC created by the heterojunction increases the velocity of electrons from the source. The current drive has been increased based on that functionality. The source and drain (SiC) regions act as stressors to generate lateral tension and vertical compression in the channel, thereby increasing the mobility of electrons which increases output current drive.

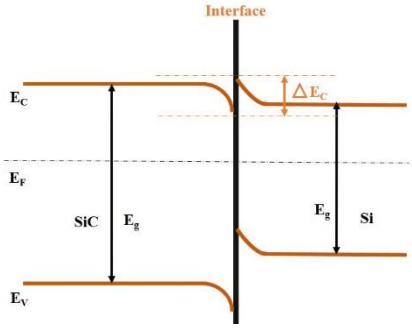

Fig. 6 –Heterojunction formation

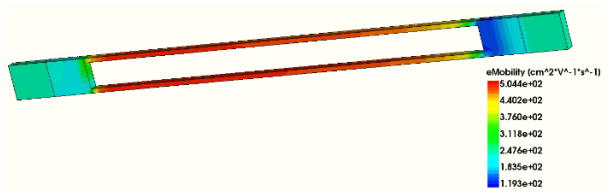

Fig. 7 – eMobility of heterojunction with single metal nitride and double channel

3.3 Metal Nitride

In heterojunction double channel device with DMG, DMG is replaced by TiN. Due to the nitrogen content in TiN, the mobility increases. Fig. 7 shows the eMobility of metal nitride in heterojunction device. Both channels have increased mobility due to the strain created by heterojunction and metal nitride. Fig. 8 and Fig. 9 depict the *I-V* characteristics of dual metal gate with double channel, dual metal gate with double channel and SiC, and single metal nitride gate with double channel and SiC. For all devices, the transfer characteristics were plotted with V_{DS} = 1.5 V and V_{GS} ranging from 0 to 1.3 V. When silicon is used as a source/drain material, the drain current saturates at 4.6 μA, but in the case of SiC as a source/drain material, the drain current increases linearly because of heterojunction. Moreover, when TiN is used as a gate metal, the drain current increases based on thickness. So, the work function of metal nitride can be tuned by increasing the nitrogen content in TiN and the thickness of the metal nitride gate. So, as per Fig. 8, when heterojunction and metal nitride are incorporated into a conventional SOI JL nanowire, the device produces 12 times better current than a conventional wire. When heterojunction and DMG are incorporated into a conventional SOI JL nanowire, the device produces 10 times better current than a conventional wire. In all devices, the SS is almost 60 mV·dec^{-1} which is near the ideal value.

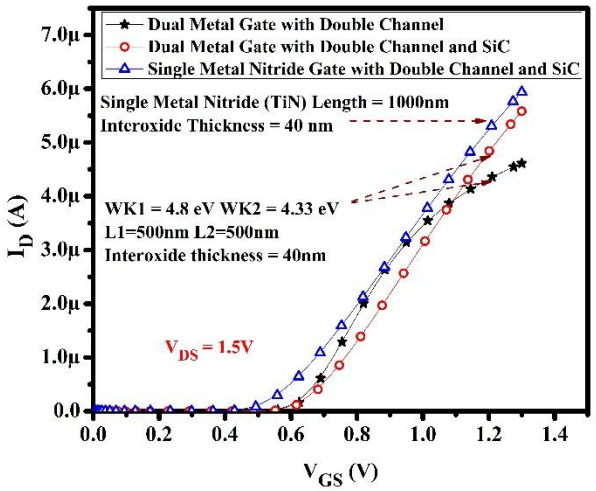

Fig. 8 – Comparison of the transfer characteristics between DMG with double channel, DMG with double channel and SiC, and single metal nitride gate with double channel and SiC

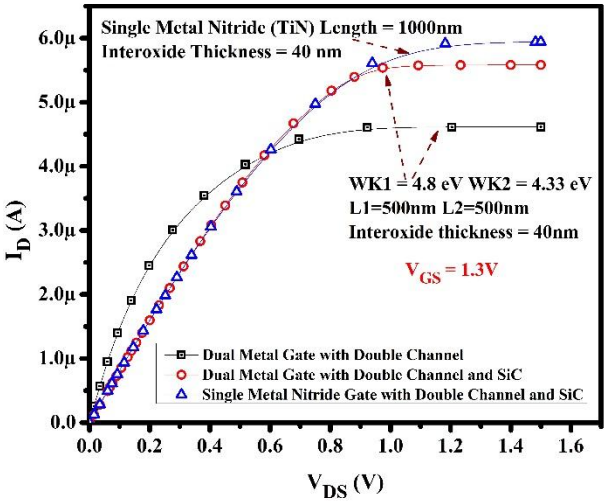

Fig. 9 – Comparison of the output characteristics between DMG with double channel, DMG with double channel and SiC, and single metal nitride gate with double channel and SiC

4. CONCLUSIONS

Without changing the device structure, using only materials, strain has been created and the carrier velocity has been increased. An increase in the carrier velocity of the device resulted in improved device performance over a conventional device [1]. The concept of heterostructure, dual-metal gate, and metal nitride has been implemented in this work, and the outcomes are compared with a conventional SOI JL nanowire transistor. Almost 12 times better current drive than a conventional JL nanowire is produced under different strain levels.

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Аналіз безперехідного транзистора на основі нанодротів з гетеропереходом, нітридом металу та подвійним металевим затвором

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У роботі зосереджено увагу на характеристиках безперехідного (JL) багатоканального SOI транзистора на основі нанодротів. Його було проаналізовано під впливом різних деформацій для покращення продуктивності. Замість одного каналу, за допомогою концепції Multi Bridge Channel (MBC), два канали були включені в JL структуру нанодротів. Крім того, для вдосконалення JL пристрою було використано три методи. Перший – концепція подвійного металевого затвору (DMG), другий – гетероперехід (карбід кремнію (SiC) використано як матеріал стоку/витоку), і третій – нітрид металу. За допомогою цих трьох методів було збільшено мобільність, а також керуючий струм. Порівняння вольт-амперних (*I-V*) характеристик було проведено між DMG та одинарним металевим затвором, DMG та одинарним метал-нітридним затвором за допомогою комп'ютерного симулятора Sentaurus Technology Computer Aided Design (TCAD). Результати було відкалібровано з використанням фізичних моделей, таких як залежна від температури модель транспорту носіїв (дрейфова дифузія), модель градієнта густини, модель мобільності та рекомбінаційна модель Шоклі-Ріда-Холла. Інтеграція гетеропереходу в DMG та одинарний метал-нітридний затвор покращила продуктивність обох пристроїв, але останній показав на 6 % кращу продуктивність, ніж DMG з гетеропереходом. У всіх пристроях коефіцієнт підпорогових коливань (SS) складає майже 60 мВ дек$^{-1}$, що є майже ідеальним значенням.

Ключові слова: Безперехідний тризатворний, Двоканальний, TiN, DMG, Карбід кремнію (SiC).