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Impact of High-*k* Dielectric Materials on Short Channel Effects in Tri-gate SOI FinFETs

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The CMOS technology has been dominated long enough by the silicon material world and it has been approaching to its limitations. With contracting magnitudes of thicknesses of the gate oxide layer, leakage current worsens which drastically reduces the device reliability. In the nano regime device, the introduction of high-*k* materials has brought down the Short Channel Effects (SCEs) significantly. They also provide electrical stability and have proven to be scalable. Different devices are evolved for different gate oxides such as SiO_2 and high-*k* materials like Si_3N_4, Al_2O_3, ZrO_2 and HfO_2. These high-*k* dielectric materials are compared with the performance of SiO_2 in a Tri-Gate (TG) SOI FinFET device. TG SOI FinFETs with 14, 10 and 8 nm gate lengths are implemented for all the dielectric materials considering an equivalent oxide thickness of 1 nm for SiO_2. Since the devices are developed in the nano regime, the parameters relating to SCEs such as the roll-off of threshold voltage, on-to-off current ratio and DIBL are investigated and analyzed for all the TG SOI FinFETs. Observation of the electrical characteristics of the devices led to the culmination that the I_{on} current is at the same level for all geometrical gate lengths. But the leakage currents reduced drastically with HfO_2 as the gate dielectric material rendering the highest switching speed of the device along with excellent control over the short channel parameters. The results inevitably show that high-*k* dielectric material based devices provide enhanced performance by reducing the leakage current, thereby attaining degradation in the SCEs. It has also been perceived that the HfO_2 based TG SOI FinFET is found to be the most superior among all others even at 8 nm channel length.

Keywords: High-*k* dielectrics, TG FinFETs, Subthreshold swing, DIBL, Silvaco TCAD.

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1. INTRODUCTION

As electronics devices are shortening, the scaling of devices has become the predominant research area to increase the chip density. For the past few decades, MOSFETs have been the choice for the semiconductor industry. Inadequate scaling of a MOSFET when it reaches below 100 nm is called nanotechnology devices [1]. As device scaling followed the Moore's law, these devices needed certain enhancement which could be done by implementing a new design or introducing a new material for a new device. Therefore, when the device channel length is scaled below 32 nm, MOSFETs exhibit degradation in their performance in various applications due to Short Channel Effects (SCEs) like degradation of subthreshold swing (SS), Drain Induced Barrier Lowering (DIBL), punchthrough and Gate Induced Drain Leakage (GIDL) [2-9]. Different approaches have been made by researchers around the globe to enhance the performance of MOSFETs while also shrinking the geometry. Some of their techniques include changing the doping concentration, reducing the gate oxide thickness, introducing a dual material gate, high-*k* dielectric materials, silicon-on-insulator (SOI), multigate architecture, vertical FET, and implementing strained silicon technology [10-12]. Among the different techniques mentioned, a strategy has been introduced termed SOI technology to integrate so as to have more electrical components in a microprocessor chip. This technique enables faster switching speed, deduction of power consumption in the circuit and better current drive while scaling down the device.

In the modern world, a conventional MOSFET has encountered many limitations in nano regime. In order to counter this problem, new architectures are needed to improvise the MOSFET configuration. Several approaches have been made in the past couple of years. Among those different device structures that are being developed, a multigate structure exhibits one of the most efficient approaches. Therefore, a multigate design called FinFET has been adopted to carry out the scaling in nano regime. An analytical study of FinFETs has been one of the most research topics in prominent companies like TSMC, Intel and Samsung to process and fabricate more efficient microprocessors.

Since SCEs are the reason for the set-back of nano regime devices, the ratio between the insulator thickness and the channel length must be maintained at an optimal level in order to have efficient control of SCEs [13]. At the same time, gate leakage current arises when we reduce the thickness of the dielectric beyond 2 nm [14], which degrades the performance efficiency of the device. For this reason, apart from the device model, a new type of materials has been introduced to minimize the SCEs. The new materials are called high-*k* dielectric materials. They have thicker insulators, but still have an efficient effect of the channel region resulting in the reduction of leakage or OFF currents [15]. The introduction of high-*k* materials has increased the capacitance, and thus the ON current of the device rises without actually interfering with leakage effects of the device [16].

Based on the specified parameters and a distinct model described in the statements above, the efficient characteristics of SiO_2 and high-*k* dielectric materials are compared and analyzed for the same TG *n*-FinFETs.

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2. DEVICE STRUCTURE

The three-dimensional (3D) TG FinFET schematic is displayed in Fig. 1 and the different parts are listed in Table 1. The formation of 3D schematic devices and their analyses are carried out using Silvaco Atlas TCAD tools. Different models have been used for the device simulations such as band gap narrowing model, SRH model, Auger model and Lombardi CVT model.

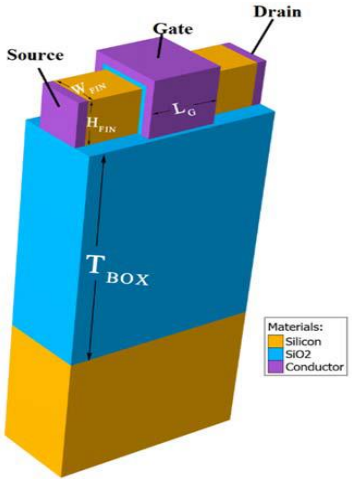


Fig. 1 – 3D formation of a SOI FinFET showing the geometric dimensions of the device

Table 1 – Device properties of the FinFET structure

Notations	Value
L_{Dr}, L_{So}	11 nm
L_G	8-14 nm
T_{ox} (SiO_2)	1 nm
W_{FIN}	10 nm
H_{FIN}	10 nm
T_{BOX}	50 nm
$T_{substrate}$	30 nm
N_A	$1{\cdot}10^{15}$ cm^{-3}
N_D	$1{\cdot}10^{18}$ cm^{-3}

Several TG SOI FinFETs are configured with varied gate insulator materials like SiO_2 ($k = 3.9$) and other high-k dielectric materials such as Si_3N_4 ($k = 7.8$), Al_2O_3 ($k = 9.3$), ZrO_2 ($k = 22$) and HfO_2 ($k = 25$). The oxide thicknesses and electrical characteristics are compared and studied for an Equivalent Oxide Thickness (EOT) of 1 nm SiO_2 and are expressed by [17]

$$EOT = T_{high-k}\frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}}, \quad (1)$$

where k is the dielectric constant and T represents the high-k material thickness. The detailed parameters that are used for the developed devices are presented in Table 1. Different TG SOI FinFETs are simulated for varied gate oxides mentioned each having EOT of 1 nm SiO_2. The channel lengths are varied between 14, 10 and 8 nm for all gate dielectrics. SOI technology has been introduced where a 50 nm thick buried oxide is grown on silicon substrate. The substrate having used in the device has 30 nm thickness. The width and length of the fin are kept at 10 nm for all devices as shown in Fig. 1. The source length as well as the drain length are simulated at 11 nm for each device. The doping concentration level of the source and drain regions is taken to be 10^{18} cm^{-3}, and the channel region is doped at 10^{15} cm^{-3}.

3. RESULTS AND DISCUSSION

The modelling and simulation of 3D TG SOI devices are carried out using Silvaco Atlas simulator for all varied gate oxides utilized for three channel lengths analyzed here. The simulation is first done using 1 nm thick SiO_2 as the gate oxide material for all different gate lengths, because SiO_2 is the most commonly used gate oxide. Then after, SiO_2 is replaced by high-k dielectric materials such as Si_3N_4, Al_2O_3, ZrO_2 and HfO_2 and their features are thereby compared using the EOT of 1 nm on a TG FinFET. The linear I_D-V_{GS} characteristic is observed in Fig. 2 clearly, showing the comparison analysis for different gate dielectric materials. It is also evidently observed from the figure that due to higher metallic properties in the Al_2O_3 layer, the device has a low threshold voltage; therefore, the additional leakage resistance is likely active, whereas the HfO_2 based dielectric device evidently signifies that gate leakage is extensively reduced as the oxide thickness is maximum in comparison to all others, as displayed in Fig. 2.

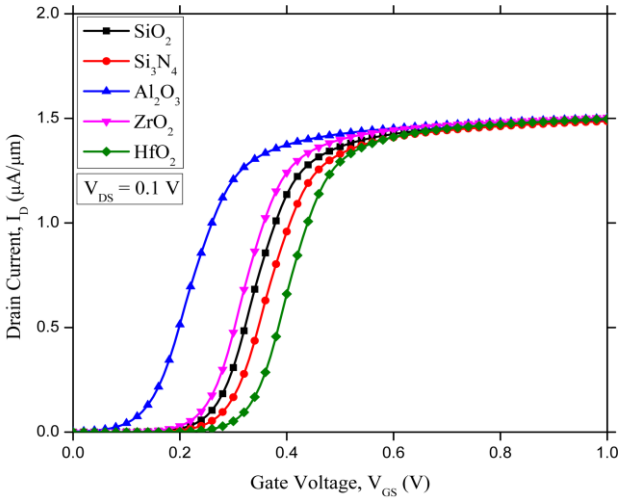
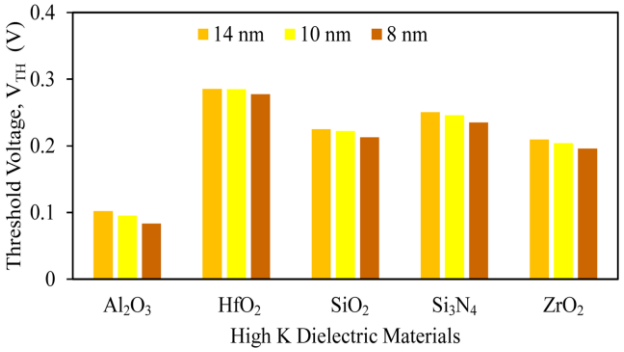


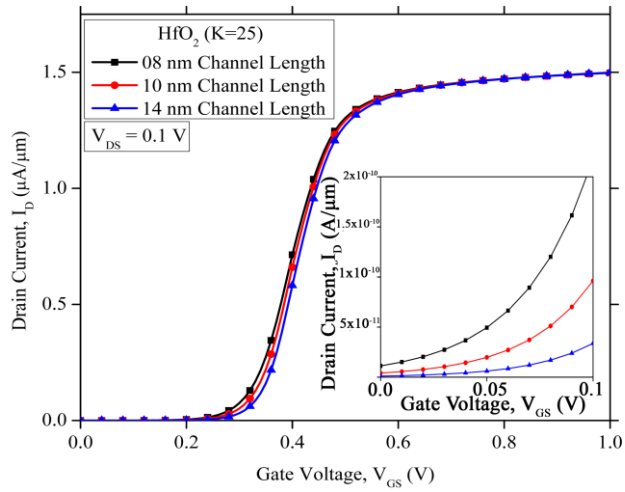
Fig. 2 – Simulated I_D-V_{GS} graph in linear representation with different high-k dielectric materials at 10 nm channel length

The variation of V_{GS} is taken from 0 to 1 V with a step of 10 mV. From Fig. 3a, the threshold voltages of different FinFET devices are determined to be least as 0.083, 0.095 and 0.102 V for Al_2O_3 and maximum as 0.27, 0.28 and 0.285 V for HfO_2 for 8, 10 and 14 nm gate length devices, respectively. With increasing gate voltage, a large increase in the drain current occurs depending on the threshold voltage, which is affected by the drain voltage. This shows an attainment of lesser leakage with HfO_2 as the gate oxide material. Hence, Fig. 3b is acquired which displays the I_D-V_{GS} variation for HfO_2 based FinFET for three different gate length devices and evidently showcases that the 8 nm gate length device has a lower threshold, as observed from the inset figure. The threshold voltage impacts improvements in the I_{on} current and the device having

HfO_2 thus outshines all others in this factor. The ON current (I_{on}) is simultaneously extracted from the I_D-V_{GS} characteristics graph. The I_{on} current is observed to differ moderately around 1.5 μA/μm at V_{GS} = 0.1 V for all simulated devices.



a



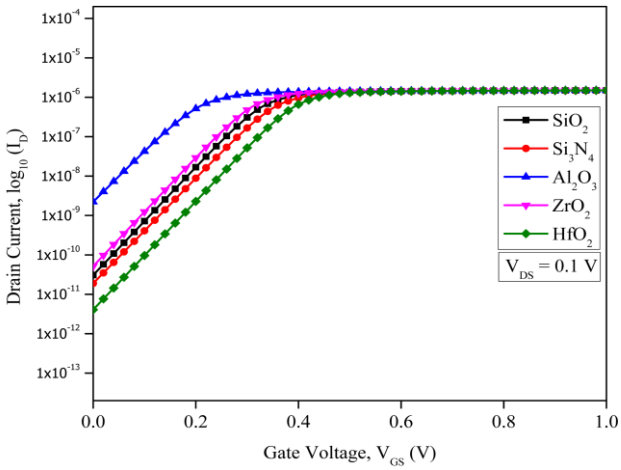
b

Fig. 3 – (a) Variation of V_{th} of SOI FinFETs with various high-k dielectric materials for 14, 10 and 8 nm channel length. (b) I_D-V_{GS} characteristics of SOI FinFET with HfO_2 as high-k dielectric material at 14, 10 and 8 nm channel length in linear scale

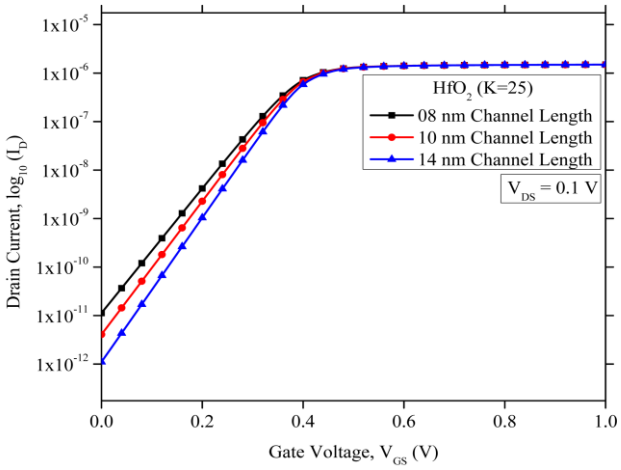
Fig. 4 illustrates the transfer characteristics graphs in logarithmic scale for the TG SOI FinFET structure which portrays the subthreshold swing SS and I_{off} current for the device. From Fig. 4a, it is noticed that devices with HfO_2 as dielectric have the best property in terms of lower leakage and lower I_{off} in comparison to other dielectric-based devices which are employed here. Hence, HfO_2 based TG SOI FinFET invariably outperforms other devices. Based on the equation developed in [18], I_{off} current for the device is therefore calculated using the following equation:

$$I_{OFF}(\text{nA}) = 100\frac{W}{L}10^{\frac{-V_{th}}{SS}}, \qquad (2)$$

where L and W are, respectively, the length and width of the channel, V_{th} is the threshold voltage and SS is the subthreshold swing. As inevitably detected from Fig. 4a, HfO_2 based SOI FinFET provides enhanced leakage performance. An analysis of HfO_2 at three different gate lengths is performed and shown in Fig. 4b, where, as expected, the 8 nm gate length device showed a higher SS and a higher I_{off} current.



a



b

Fig. 4 – (a) Logarithmic transfer characteristics of SOI FinFETs with different high-k materials at 10 nm channel length in log scale. (b) I_D-V_{GS} characteristics of SOI FinFETs with HfO_2 as high-k dielectric material at 14, 10 and 8 nm channel length in log scale

From the I_D-V_{GS} plot in Fig. 4, the I_{on} current as well as leakage currents are extracted and plotted for FinFETs in Fig. 5 and Fig. 6, respectively. Although the I_{on} current is quite similar in all gate length devices at around 1.5 mA/μm for both Al_2O_3 and HfO_2 dielectric devices, the I_{off} current, which basically signifies the leakage parameter during device operation, provides considerable enrichment with leakage current in the range of picoamperes in comparison to nanoamperes for Al_2O_3 based devices. Because of this reason, a distinctive variation in the ON-to-OFF current ratio is vehement, as plotted for all three gate length devices in Fig. 7. The I_{on}/I_{off} ratio shows the variation for different materials, in which HfO_2 shows the maximum ratio, which means that the device developed using HfO_2 material shows minimum gate leakage which is the most desirable characteristic for an efficient device.

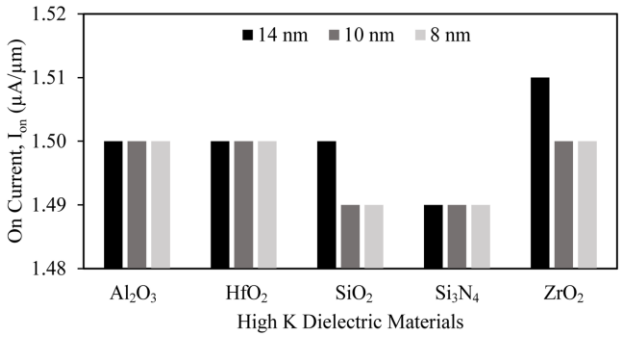


Fig. 5 – Variation of I_{on} of SOI FinFETs with various high-k dielectric materials for 14, 10 and 8 nm channel length

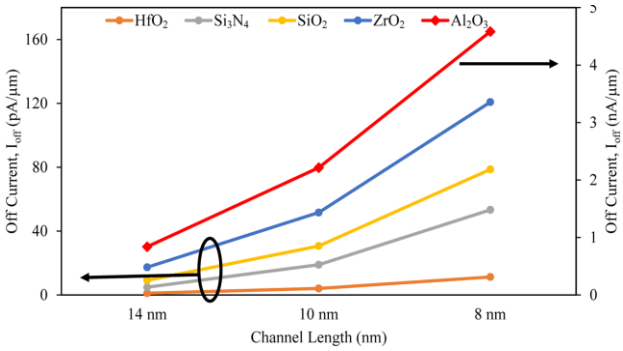


Fig. 6 – Variation of I_{off} of SOI FinFETs with various high-k dielectric materials for 14, 10 and 8 nm channel length

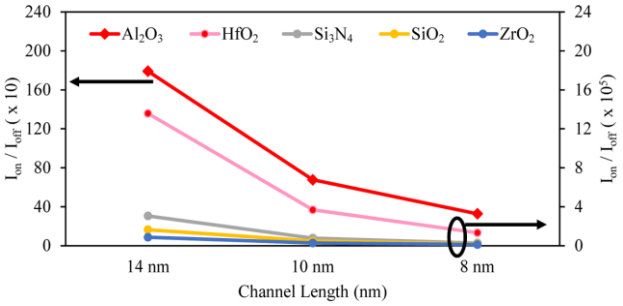


Fig. 7 – Comparison of I_{on}/I_{off} current ratio with various high-k materials for 14, 10 and 8 nm channel length

The comparison of the subthreshold swing for different dielectric materials is plotted in Fig. 8. The subthreshold swing has been one of the primary factors responsible for the observation as well as the calculation of the leakage current in SOI FinFETs. This is the ratio of the change in voltage V_{GS} to a tenfold change in I_{drain} of weak inversion measured in mV/decade. It is also obvious that when the device channel length starts to decrease, SS begins to increase and is calculated as [19]:

$$SS\left(\frac{mV}{decade}\right)=\frac{dV_{CS}}{d\left(\log_{10} I_{DS}\right)}, \qquad (3)$$

where dV_{GS} is the change in gate voltage for $d(\log_{10}(I_D))$ change in drain current, which is a tenfold change in I_D. It is clearly observed from Fig. 8 that though SS increases with a decrease in the device gate length and also for a channel size of 8 nm, SS appears to be 77.8 mV/decade for HfO_2 based FinFET, but still the concerned device stands well within leakage limit as per the ITRS standpoint [21]. Thus, the development of HfO_2 based SOI FinFET for the 8 nm gate length device proved to be better and hence satisfies the earnest quest of the paper.

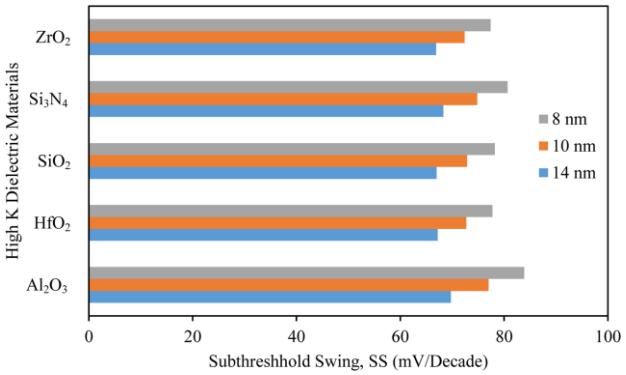


Fig. 8 – Variation of SS of SOI FinFETs with various high-k dielectric materials for 14, 10 and 8 nm channel length

Here another important aspect that has also been considered for comparison is DIBL in the simulated TG SOI FinFET for all different dielectric materials which is displayed in Fig. 9. DIBL is the SCE, defined as the ratio of the modified threshold voltages for a large change in drain voltage, given by:

$$DIBL\left(\frac{mV}{V}\right)=\frac{\Delta V_{th}}{\Delta V_{DS}}, \qquad (4)$$

where ΔV_{th} is the transition of the threshold voltage for variations in drain voltage.

The DIBL values are compared in Fig. 9 where HfO_2 and ZrO_2 materials with the highest dielectric constants show improved performance than the rest of the material-based devices when used for the development of SOI FinFETs.

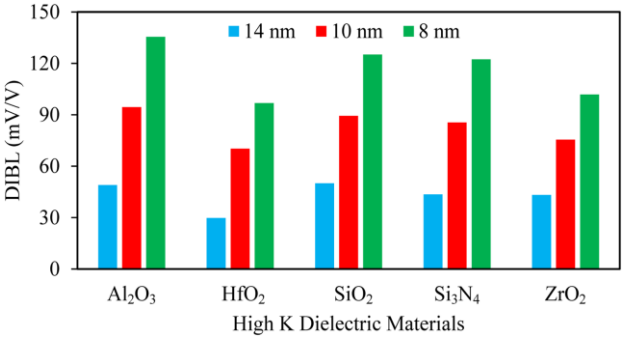


Fig. 9 – Variation of DIBL in FinFETs with different high-k dielectrics for 14, 10 and 8 nm channel length

With diminishing channel dimensions, the leakage current increases due to the SCEs, but still, even for an 8 nm gate length, the leakage acquired is within the ITRS limit and hence the device satisfies the requirement. From the analysis carried out, it has been estimated that SOI FinFETs with HfO_2 as a dielectric material are superior to others, especially in terms of leakage parameters of the device. Therefore, to have a detailed investigation-based analysis, all the performance parameters of FinFETs based on different dielectric materials are tabulated in Table 2.

Table 2 – Comparison of the performance parameters of various high-*k* dielectric materials

	Al_2O_3	HfO_2	Si_3N_4	SiO_2	ZrO_2		Al_2O_3	HfO_2	Si_3N_4	SiO_2	ZrO_2
Threshold voltage, V_{th} (V)						I_{on}/I_{off} current ratio					
14 nm	0.102	0.285	0.250	0.224	0.209	14 nm	$1.79{\cdot}10^3$	$1.36{\cdot}10^6$	$3.05{\cdot}10^5$	$1.64{\cdot}10^5$	$8.68{\cdot}10^4$
10 nm	0.095	0.285	0.245	0.222	0.204	10 nm	$6.78{\cdot}10^2$	$3.68{\cdot}10^5$	$7.85{\cdot}10^4$	$4.87{\cdot}10^4$	$2.91{\cdot}10^4$
8 nm	0.083	0.277	0.235	0.212	0.195	8 nm	$3.27{\cdot}10^2$	$1.33{\cdot}10^5$	$2.79{\cdot}10^4$	$1.90{\cdot}10^4$	$1.24{\cdot}10^4$
On current, I_{on} (μA/μm)						Subthreshold swing, SS (mV/Decade)					
14 nm	1.50	1.50	1.49	1.50	1.51	14 nm	69.72	67.17	68.28	66.98	66.90
10 nm	1.50	1.50	1.49	1.49	1.50	10 nm	76.99	72.70	74.82	72.88	72.40
8 nm	1.50	1.50	1.49	1.49	1.50	8 nm	83.87	77.73	80.69	78.22	77.40
Off current, I_{off} (A/μm)						DIBL (mV/V)					
14 nm	0.84	1.10	4.87	9.12	17.3	14 nm	49.03	29.75	43.57	49.99	43.18
10 nm	2.22	4.07	18.9	30.7	51.6	10 nm	94.46	70.21	85.56	89.40	75.52
8 nm	4.58	11.3	53.3	78.7	121	8 nm	135.51	96.82	122.35	125.15	98.86

4. CONCLUSIONS

TG FinFETs with gate lengths of 14, 10 and 8 nm as are considered in this paper. The developed devices are compared for improved performance analysis that is carried out using high-*k* materials like Si_3N_4, ZrO_2, HfO_2 and Al_2O_3 as different dielectric materials. The thicknesses of the gate oxide for all simulated devices are prepared based on 1 nm EOT of SiO_2. The different short channel parameters are differentiated by analytical observations for all simulated devices. When devices are scaled down from 14 to 8 nm, the SCEs are incorporated and the performances are observed to degrade, though optimization has been carried out. The I_D-V_{GS} and I_D-V_{DS} characteristics are plotted and in parallel the threshold voltage V_{th}, I_{on} current, I_{off} current, I_{on}/I_{off} current ratio are also compared for all material-based devices being simulated, in which improvement is observed for the FinFET with HfO_2. Consequently, the subthreshold swing and DIBL are also compared where HfO_2 based FinFET outperformed others as the best performer for simulated devices. So, in conclusion, it is clear that high-*k* dielectric materials show an increase in SCEs, and HfO_2 in particular is the most promising dielectric material that can be employed even at 8 nm technology FinFET devices.

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Вплив high-*k* діелектричних матеріалів на короткоканальні ефекти в тризатворних SOI FinFETs

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Технологія CMOS досить довго панує в світі кремнієвих матеріалів і вже наближається до своїх обмежень. Зі зменшенням товщини оксидного шару затвора зростає струм витоку, що різко знижує надійність пристрою. Впровадження high-*k* матеріалів значно зменшило вплив короткоканальних ефектів (SCEs) в нанопристроях. Ці матеріали також забезпечують електричну стабільність і зарекомендували себе як масштабовані. Різні пристрої було розроблено для різних оксидів затвора, таких як SiO_2, і high-*k* матеріалів, таких як Si_3N_4, Al_2O_3, ZrO_2 та HfO_2. Параметри цих high-*k* діелектричних матеріалів порівнюються з характеристиками SiO_2 в тризатворному (TG) пристрої SOI FinFET. TG SOI FinFETs з довжинами затвора 14, 10 і 8 нм реалізовані для всіх діелектричних матеріалів з урахуванням еквівалентної товщини оксиду в 1 нм для SiO_2. Для всіх TG SOI FinFETs досліджено і проаналізовано параметри, які стосуються SCEs, такі як спад граничної напруги, відношення струмів включення та виключення і DIBL. Спостереження за електричними характеристиками пристроїв привело до висновку, що струм I_{on} знаходиться на одному рівні для всіх геометричних довжин затвора. Але струми витоку різко знижуються з використанням HfO_2 як діелектричного матеріалу затвора, що забезпечує найвищу швидкість перемикання пристрою поряд з відмінним контролем короткоканальних параметрів. Результати показують, що пристрої на основі high-*k* діелектричних матеріалів забезпечують покращені характеристики за рахунок зниження струму витоку, тим самим досягаючи зменшення впливу SCEs. Було також встановлено, що TG SOI FinFET на основі HfO_2 є найбільш ефективним серед усіх інших транзисторів навіть при довжині каналу 8 нм.

Ключові слова: High-*k* діелектрики, TG FinFETs, Підпорогові коливання, DIBL, Silvaco TCAD.