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ALD Grown Al_2O_3 as Interfacial Layer in ITO Based SIS Solar Cells

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Conventional diffusion process to form the emitter of a c-Si solar cell is a complicated process with high thermal as well as economic budget. An alternative to avoid this process is to form MIS/SIS structured solar cells, where different process is used to form the emitter portion of the cell. In this study, 3 × 3 (ITO-Al_2O_3-*n*-Si) structured SIS cell is developed, where *n*-Si is the base material, Al_2O_3 and ITO layer act as hole selective layer and emitter layer, respectively. Sputtered ITO layer of thickness 150 nm acts as a degenerative semiconductor as well as ARC. For ITO coated cell, average reflectance reduced to 4.54 % from 13.63% compared with only textured cell. Metallization is done using Ag on both the sides on the front side above the ITO layer and a continuous contact on the back side by vacuum coating unit. Apart from hole tunnelling, ALD grown very thin 1.5 nm layer of Al_2O_3 acts as a passivation layer and increases minority carrier lifetime from 9.732 μS to 17.548 μS. Achieved open circuit voltage (V_{oc}) and short circuit current (I_{sc}) are 684 mV and 35 mA, respectively.

Keywords: SIS, ITO, Al_2O_3, Reflectivity, Degenerative semiconductor, Hole selective contacts.

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1. INTRODUCTION

Conventional c-Si solar cell manufacturing process have few complicated steps to follow. After going through some surface modification processes the c-Si wafer put into diffusion chamber to develop opposite type semiconductor layer and form *p-n* junction. This diffusion process is a high temperature energy extensive process where high thermal budget is required [1]. To avoid such difficulty SIS structured solar cells can be manufactured. From the literature these cells have comparatively poorer performance than the conventional c-Si solar cells though there are several advantages [5]. Major advantages of developing SIS based cell rather than conventional SIS based cell are lesser material requirement and lesser cost [4]. SIS based solar cell uses some TCOs (Transparent Conducting Oxides) as top layer which serves the purpose of emitter. As this TCOs have good anti reflecting property and conductivity, use of ARCs can be minimized and a smaller number of front contacts can easily extract decent amount of current from the cell [6]. The automatically grown SiO_x layer acts as an interfacial layer and minimizes the mismatch losses in the solar cell. In some previous studies it was found that use of some very thin insulating layer between the base c-Si and TCO layer improves the performance of the cell [7]. In this study, to examine such property a very thin insulating layer of Al_2O_3 is developed by Atomic Layer Deposition Process in between c-Si wafer and TCO and its properties are studied.

2. NOTATIONS

SIS: Semiconductor Insulator Semiconductor
TCO: Transparent Conducting Oxide
ITO: Indium Tin Oxide
ALD: Atomic Layer Deposition
ARC: Anti Reflective Coating
V_{oc}: Open Circuit Voltage
I_{sc}: Short Circuit Current
EQE: External Quantum Efficiency
Ag: Silver
c-Si: Crystalline Silicon
n-Si: *n* type Silicon
mV: milli Volt
mA: milli Ampere
nm: Nano meter

3. THE STRUCTURE

The SIS solar cell under study has a 180-micron *n*-type mono c-Si over which a very thin 1.5 nm Al_2O_3 layer has been developed for minimizing the mismatch. Above the interfacial Al_2O_3 layer, ITO (Indium Tin Oxide) layer of thickness 150 nm is formed which acts as ITO layer. At the top, grid structured contacts coated and at the back continuous contacts has been coated with Ag. The cross-sectional structure of the cell is given in the following Fig. 1.

4. WORKING PRINCIPLE

In ITO based *n*-type solar cell, *n*-type silicon is used as base material. Above the n type Silicon ITO is deposited and in between these two layers an insulating layer is deposited to tunnel the minority carrier forming a SIS structure. ITO based *n*-type Si solar cells have different mechanism than the conventional *p-n* junction solar cells. ITO is basically a mixture of Indium oxide (In_2O_3) and ein oxide (SnO_2) with different weight proportions which is a degenerative semiconductor which is *n*-type highly doped. So, a question may

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arise if both the materials are of n-type how barrier potential is formed and how carriers are separated. Though ITO is n-type semiconductor, but it is highly doped than the base n-type Si.

ITO has doping level of about 3.8×10^{20} cm^{-3} on the other n-type base Si has doping level of 2×10^{15} cm^{-3}. This difference in doping level forms a depletion region in the interface region of these two layers and built-in field is likely located in the lightly doped n-Si substrate. For carrier separation, work function difference between ITO and n-Si layer do the key role. The work function difference between these two layers develops maximum built-in potential of 0.69 V which is very much fair enough for carrier separation of photo generated carriers. Though interface traps might lead to decrease in open circuit voltage. So, chemical bonding and electronic structure in between the region of ITO and n-Si do the key role on cell performance of this configuration as the tunnelling and passivation of n-Si is done by this region [2].

5. FABRICATION PROCESS

The fabrication process starts with taking 3×3 n-type mono c-Si wafer. Then the wafer is textured with alkaline KOH solution to reduce the reflection from the wafer surface. After that, the wafer is put into the ALD unit to form very thin 1.5 nm Al_2O_3 layer on the top surface of the wafer with only five spraying cycles. In the next step 150 nm thick ITO (Indium Tin Oxide) layer is deposited on the top surface over Al_2O_3 layer with sputtering process maintaining the process temperature to 180 °C. Then grid structured Ag front contact and continuous back contact is coated with vacuum coating unit by taking Ag strips. In the final step the cell is thermally treated by keeping it in the hot air oven at 250 °C for 30 min.

In this fabrication process major advantage are ITO serves both as emitter and ARC layer which eliminates the requirement of extra ARC layer which involves extra step, and the ITO deposition process requires only 180 °C which is very low compared to conventional emitter formation process where around 900-950 °C is required. The step-by-step process of this fabrication process and the top view of the complete cell are given in Fig. 2 and Fig. 3.

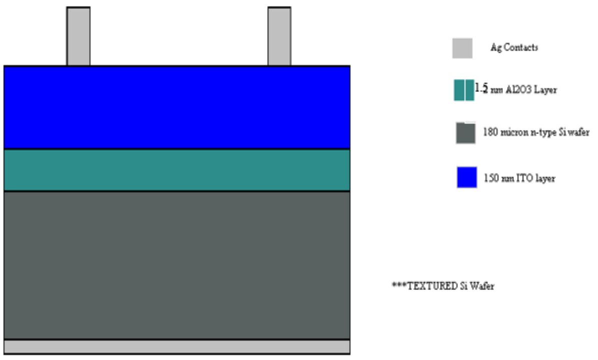

Fig. 1 – Structure of the SIS based solar cell

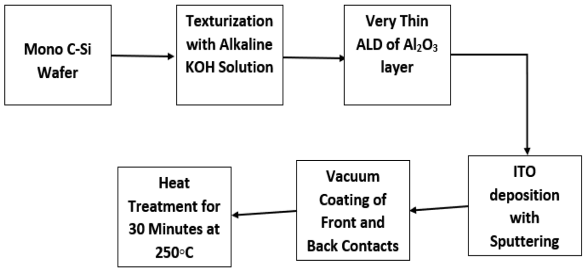

Fig. 2 – Flow chart of the process involved in the fabrication process of the solar cell

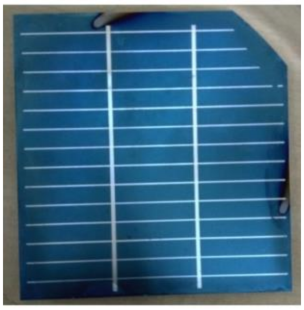

Fig. 3 – Top view of the SIS based solar cell

6. RESULTS AND DISCUSSION

6.1 Electrical Property

The fabricated cell gives Open Circuit Voltage (V_{oc}) of 684 mV and Short Circuit Current (I_{sc}) of 35 mA, but it does not give particularly good fill factor which result in linear *IV* curve.

The reason behind having poor fill factor is higher thickness of base material compared to ITO layer which produces high bulk resistance.

Insertion of ALD grown 1.5 nm Al_2O_3 layer has doubled the carrier lifetime of the cell to 17.548 μS from 9.732 μS which basically gives higher current density compared to the cell with absence of Al_2O_3 layer. Due to the conductive property of ITO, the cell gives decent current performance despite having lesser number of fingers on the front contact.

The performance of the SIS based solar cell is evaluated by measuring the EQE. The EQE curve (Fig. 4) gives the value of EQE at different values of light wavelength in the acceptable range. The EQE ranges between 65-90 % for acceptable range of wavelength.

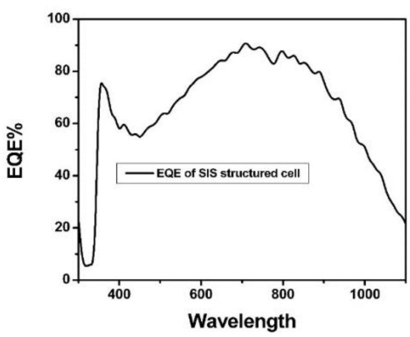

Fig. 4 – EQE curve of the SIS based solar cell

6.2 Optical Property

The optical property of the cell is incredibly good without having dedicated ARC layer. The anti-reflecting property of ITO permits the solar cell to have an exceptionally low reflectivity for the top surface.

The reflectance spectra of ITO based SIS cell and textured only cell are given in Fig. 5 and Fig. 6, respectively. The comparison of the cell with and without ITO layer is discussed in Table 1.

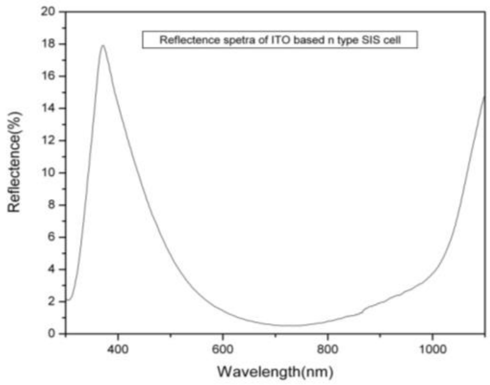

Fig. 5 – Reflectivity vs wavelength curve of the front side of the cell

Table 1 – Comparison of the optical property of the SIS based solar cell

	Average reflectance	SWR	Minimum reflectance
ITO based SIS solar cell	4.54 %	4.03 %	0.507 % at 713 nm
Textured only	13.63 %	12.7 %	10.015 % at 864 nm

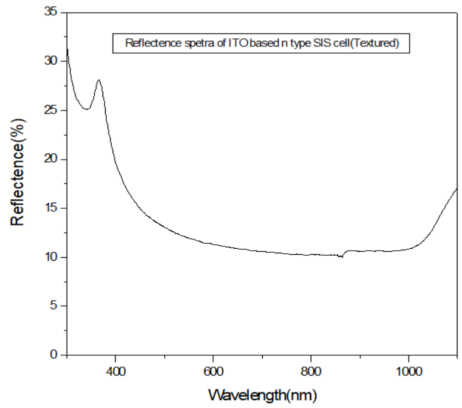

Fig. 6 – Reflectivity vs wavelength curve of the c-Si wafer without ITO layer

7. CONCLUSIONS

ITO based SIS solar cell has a good potential in future as it eliminates complex steps and reduce material use. In this study ITO based SIS solar cell is fabricated with additional ALD grown very thin Al_2O_3 layer.

The Al_2O_3 layer serves very well and increases the carrier density of the cell. The optical property of the cell is exceptionally good, and it gives good EQE which is favorable for solar cells. The electrical properties of the cell must be improved though it gives very good V_{oc} and I_{sc} of 684 mV and 35 mA, respectively. The fill factor of the cell is poor due to large bulk resistance of the base material. This may be improved by using thinner base material.

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Al_2O_3, вирощений методом ALD, як міжфазний шар в сонячних елементах SIS на основі ITO

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Звичайний процес дифузії для формування емітера сонячного елементу c-Si – це складний процес з високими тепловими та матеріальними витратами. Альтернативою для уникнення цього процесу є створення структурованих сонячних елементів MIS/SIS, де для формування емітерної частини сонячного елементу використовується інший процес. У дослідженні розроблено структурований елемент SIS розміром 3 × 3 (ITO-Al_2O_3-*n*-Si), де *n*-Si є вихідним матеріалом, Al_2O_3 та шар ITO виконують відповідно ролі селективного шару дірок та емітерного шару. Розпилений шар ITO товщиною 150 нм виконує роль виродженого напівпровідника так само як і ARC. Для сонячного елементу, вкритого шаром ITO, середня відбивна здатність зменшується з 13,63 % до 4,54 % порівняно з лише текстурованим елементом. Металізація проводиться за допомогою Ag з обох боків на лицьовій стороні над шаром ITO і постійним контактом на тильній стороні блоком для нанесення вакуумного покриття. Окрім тунелювання дірок, дуже тонкий шар Al_2O_3 (1,5 нм), вирощений методом ALD, виступає в ролі пасиваційного шару і збільшує час життя неосновних носіїв заряду з 9,732 мкс до 17,548 мкс. Досягнуті напруга холостого ходу (V_{oc}) і струм короткого замикання (I_{sc}) становлять відповідно 684 мВ і 35 мА.

Ключові слова: SIS, ITO, Al_2O_3, Відбивна здатність, Вироджений напівпровідник, Селективні контакти дірок.