## Investigation of High-K Gate Dielectrics and Chirality on the Performance of Nanoscale CNTFET

L. Renuka Devi<sup>1,\*</sup>, N. Arumugam<sup>1</sup>, J.E. Jayanthi<sup>1</sup>, T.S. Arun Samuel<sup>1,†</sup>, T. Ananth Kumar<sup>2</sup>

<sup>1</sup> Department of ECE, National Engineering College, Kovilpatti, India

<sup>2</sup> Department of ECE, IFET College of Engineering, Villupuram, India

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Carbon nanotube field-effect transistors (CNTFETs) offer peculiar properties such as ultrahigh thermal conductivity, ballistic transport, highest current density, and extremely high mechanical strength. Because of these remarkable characteristics, they were anticipated to be used as cable materials and as an alternative channel material to extend the performance of complementary metal-oxide-semiconductor (CMOS) devices. In this paper, the planar and coaxial geometries with different chirality value are discussed, various parameters are analyzed with different dielectric materials like SiO<sub>2</sub>, HfO<sub>2</sub>, and Y<sub>2</sub>O<sub>3</sub> to improve  $I_{on}$ current as well as subthreshold swing. This enhanced the device performances such as operation voltage,  $I_{on}/I_{off}$ , density/diameter, potential/diameter, and energy/DOS ratios. This approach provides a useful and integrative method for manufacturing electronic devices from nanoscale electronic materials.

Keywords: CNTFET, Planar, Coaxial, Chirality.

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### 1. INTRODUCTION

The electronics industry is focused on the production of devices that should be small, compact, with low power dissipation, and rich in size for performance. In general, complementary metal-oxide-semiconductor (CMOS) technology is related to the VLSI, where a few million or even billions of transistors (MOSFETs to be specific) are integrated into a single chip or die. Reliability, low power consumption, considerably low cost, and, most importantly, scalability are the reasons for the dominant application of CMOS technology in the manufacture of VLSI chips. Every 18 months, as per Moore's law, the number of transistors on a chip doubles. It is difficult to follow this trend beyond 14 nm due to limitations such as short channel effects (SCEs), drain-induced barrier lowering (DIBL), velocity saturation, and degradation of the hot carrier. Other transistor configurations are also available, such as Tri-gate, DG (double gate) MOSFET, and SOI (silicon on insulator) technology, but for potential nanoapplications, the development of these processes is a major problem. Nanoscale devices are promising candidates for replacing CMOS technology. Nanowire or carbon nanotube (CNT) transistors, graphene fieldeffect transistors (FETs), single-electron transistors, and spin transistors are used in these nanoelectronic devices. The CNTFET will be addressed from all these nanoelectronic devices. These CNTFETs have strong control over the development of channels with improved threshold voltage, increased subthreshold slope, high electron mobility, high current density, and high transconductance. CNTs have a wide variety of electrical, structural and thermal parameters, which vary depending on the various types of nanotubes (defined by their diameter, length, and chirality or twist). CNTFET based calibrated 2D TCAD was developed by Lin Xu et al. [1]. In this paper, the author explains that the L-shapedspacer of the CNTFET shows substantially reduced leakage current and outstanding scalability, and the gate length is 50 nm, the leakage current has decreased by  $1 nA/\mu m$  and the on-current has increased by  $2.1 \text{ mA/}\mu\text{m}$  at a supply voltage of -1 V. The CNT-film FET drain-engineered model was developed by Srimani et al. [2]. In this paper, the author approaches different parameters like the channel length, on-current, transconductance, and off-current, that have been used to suppress the leakage current. It was found that the channel length is 375 nm, the drain bias is  $V_{ds} = -2$  V, the on-state current is 0.2 mA/µm, the peak transconductance is 0.2 mS/µm, and the leakage current is less than 10 nA/µm at a supply voltage of 1.5 V. CNTFET based feedback-state structure was developed by Chenguang Qiu et al. [3]. In this paper, the author varies different parameters to reduce the leakage current and increase the on-current. It was found that the channel length is 50 nm, the diameter is 1.5 nm, the drain bias is  $V_{ds} = -1$  V, the on-current is larger than  $1\cdot 10^2$ , and low off-state current is smaller than  $1\cdot 10^{13}$  A. Singh Rohit Kumar Shailendra et al. [4] developed a gate all around carbon nanotube field-effect transistor (GAA CNTFET) for the analysis of the ac gain of single-, multiple-, and triple-stage common-source amplifiers. The author mentions a different number of channels with different diameters, oxide thickness and dielectric values in this paper. It was found that the diameter value is 1.25 nm,  $t_{ox} = 1 \text{ nm}$ ; silicon dioxide ( $K_{ox} = 3.9$ ), hafnium silicate ( $K_{ox} = 11$ ), hafnium dioxide ( $K_{ox} = 16$ ), zirconium dioxide ( $K_{ox} = 24$ ) and 40 channels were used. The gain of a single-stage amplifier is 9.102 dB, a multiple-stage amplifier is 38.26 dB and a triple-stage amplifier is 56.34 dB. CNTFET-OTA was developed by Jogad et al. [5]. In this paper, the author varies different parameters like tube (n), diameter  $(d_{CNT})$ , total harmonic distortion (THD), pitch, 3D bandwidth, output

2077 - 6772/2021/13(2)02026(8)

<sup>\*</sup> ramyalingaraj9715@gmail.com

<sup>&</sup>lt;sup>†</sup> arunsamuel2002@gmail.com

resistance, and average power. In this technique, the gain of the dc value is 30.86 dB, the transconductance value is 223 mho, the average power is 5.94 nW, and the THD value is 2.33 %. In the CMOS-OTA technique, the gain of the dc value is 8.12 dB, the transconductance value is 62.63 µmho, the average power value is  $0.81\,\mu W$  and the THD value is 6.21 %. From both the techniques, CNTFET-OTA is better to reduce the dc value, transconductance value and THD value. Singlewalled CNTs (SWCNTs) were developed by Sung-Jin Choi et al. [6] to evaluate the feasibility of highperformance applications. In this paper, the electrical properties of the bottom-gate value are LG = 270 nmand  $I_{ON} = 36 \mu A$ , transfer characteristics at VD = -0.5, the channel length is 15 nm, and the dielectric ZrO<sub>2</sub> film value is 10 nm. CNTs have different structures such as planar and coaxial and were developed by Rasmita Sahoo et al. [7]. Both structures are used to vary different parameters like channel, diameter, and the dielectric constant. In a planar structure, the diameter value is 0.1 and 0.2 V, the number of channels is 10. In a coaxial structure, the diameter value varies from 2 to 5 nm, the threshold voltage is  $V_t = 0.2$  V, and a dielectric material is SiO<sub>2</sub> (k = 3.9). GAA-CNTFET was developed by Ramakrishnan et al. [8]. In this paper, the author explains that the threshold voltage was used to vary various parameters such as the chiral vector, diameter, and dielectric material. If the chiral vector decreases, then the threshold voltage increases (the chiral vector value is 8.0 and the threshold voltage value is 654.468). If the threshold voltage decreases, then the chiral vector increases (the chiral vector is 25.0, the threshold voltage value is 194.136). If the thickness of the layer increases by 3 nm, then the threshold voltage decreases by 355 mV. If the diameter value increases by 2.3 nm, then the chiral vector value increases by 10.0. A sensitive double-gate junctionless FET based on integrated *n*-type CNTs was developed by Abdul Barik et al. [9]. The sensitivity of this system is 1.25 V/decade with good linearity from 0.01 to 0.2 pH in *n*-type CNTFET, the drain voltage differs from 0 to 1 V in the 0.2 V phase. There are two types of CNTs considered by Parijat Pandey et al. [10]. In this paper, the first type is single-walled CNTs and the second one is multi-walled CNTs. In several different applications, the functionalization of CNTs makes them useful. The applications of CNTs in the field of biomedicine are particularly investigated in three main fields: biomedical imaging, drug delivery biosensors, and tissue engineering scaffolds. CNT-based three-stage operational amplifiers were developed by Nizamuddin et al. [11]. In this paper, the author discusses various parameters such as dc gain, average power, output resistance, and OP-AMPs 3-dB bandwidth performed by varying the number of CNTs (N). The dc gain increases by 17 percent, the output resistance decreases by 90 %, and the power consumption decreases by 40 %. A double-gate CNTFET was developed by Reena Monica Ponnayan. et al. [12]. This paper changes the electrical pattern in an inhomogeneous dielectric material at both the top and bottom of a CNT. In both the top and bottom, different dielectric materials were used. The top gate dielectric is Al<sub>2</sub>O<sub>3</sub> and the top value is 9.8; the bottom gate dielectric is  $HfO_2$  and the bottom value is 16. Gigahertz integrated circuits based on CNT films are considered in [13]. CNTs directly integrated into CMOS by local synthesis – towards a waferlevel process – are studied in [14]. A new two-dimensional (2D) analytical model of a single-gate (SG) silicon-oninsulator (SOI) tunnel field effect transistor (TFET) is proposed by T.S. Arun Samuel in [15]. A new 2D analytical model of a dual-material gate TFET (DMG TFET) is developed by T.S. Arun Samuel in [16]. The authors developed different types of CNTs, respectively.

However, there are some drawbacks in subthreshold swing and input/output current. The main purpose of this paper is to summarize the experimental results on planar and coaxial geometries with different parameters such as the channel length, oxide thickness, top gate and dielectric materials, and the chirality value is used to achieve low leakage current and reduce the CNT length.

In this paper, Section 2 discusses the device structure of CNTFET, Section 3 discusses the proposed structures of CNTFETs, and Section 4 contains the results and their discussion.

### 2. DEVICE STRUCTURE OF CNTFET

One of the most promising possible descendants of MOSFETs is a CNTFET. A CNT is the main part of a nanocylinder consisting of a sheet of carbon atoms with excellent electrical, thermal, and mechanical properties. CNTFETs are classified into two forms such as single-walled CNTFETs (SWCNTFET) and multiwalled CNTFETs (MWCNTFET). SWCNTFETs have single graphene sheets with one atomic layer in thickness and are divided into three classes, namely, armchair, zigzag, and chiral. The electrical conductivity of these three groups depends on the chirality or direction of the distortion. CNTs may be, depending on the chirality, metallic or semiconducting. The chiral vector Cmay be written as  $C = n \cdot a_1 + m \cdot a_2$ , where graphene lattice base vectors are  $a_1$  and  $a_2$ . The pair of integers is called the chiral index (n, m). The zigzag CNTFET is used in this paper because it shows larger changes in resistance along length with longitudinal reduction or compression compared to the other two methods. Presently, there are many types of CNTFETs developed, but CNTFET geometries can be grouped into two main types: planar CNTFETs and coaxial CNTFETs.

## 3. PROPOSED STRUCTURES OF PLANAR AND COAXIAL CNTFETs

The basic theory is based on planar and coaxial CNTFETs, although it is regulated by additional phenomena such as 1D density of states (DOS), ballistic transport, and phonon dispersion. To date, planar CNTFET equipment has been manufactured mainly due to its relative simplicity and moderate compatibility with existing production technologies. The nanotube and the metallic source-drain contacts are placed on an insulating substrate with either the nanotube draped over the pre-patterned contacts or the contacts patterned above the nanotube. Coaxial geometry maximizes the capacitive coupling between the gate electrode and the nanotube surface, generating, at a given bias,

INVESTIGATION OF HIGH-K GATE DIELECTRICS AND ...

more channel charge than other geometries, with the effect of quantum mechanical size quantization and phase coherence in zigzag CNT structures.



Fig.  $1-\mbox{The proposed structures of CNTFETs}$ 

In both proposed device structures, the dimensions of the main system include the nanotube length (10 nm), source and drain doping, top gate length (8 nm), planar oxide thickness (8 nm) and coaxial oxide thickness (4 nm), dielectric constant of gate insulators, dielectric substrate, etc. In this paper, the chirality values of 7.0 and 10.0 are obtained. Since the spin for finite-length nanotubes is polarised in one direction at one of the two ends and in the opposite direction at the other end, the chirality value increases, and the diameter also increases. In this manner, the chirality values of 10.0 and 7.0 show larger changes in resistance along length with longitudinal reduction or compression compared to other values. The problem of leakage current increases as the oxide layer thickness decreases. We are looking for various dielectric materials such as silicon dioxide (SiO<sub>2</sub> = 3.9), yttrium oxide  $(Y_2O_3 = 16)$ , and hafnium dioxide  $(HfO_2 = 25)$  to overcome this problem.

### 3.1 Simulation Setup

The CNTFET simulation is carried out by the CNTFET lab tool of nano HUB.org. Tools for simulation are useful for system evaluation, potentials, output characteristics and recommendations for the fabrication process. The manufacturability of devices is the most complicated issue, to overcome such problems nano HUB platform is used. For example, the diameter of the tubes may be regulated in tube synthesis, but not by chirality. Consequently, the tubes are a mixture of semiconductors and metals. CNTFET is a nanodevice that is used in the channel area for CNT application. The zigzag CNTFET is used in this paper since it shows the higher resistance value concerning the length with longitudinal reduction or compression. Currently, there are many types of CNTFETs developed, but CNTFET geometries can be grouped into two main geometries. They are planar CNTFETs and coaxial CNTFETs. Both structures are used to analyze different parameters with various dielectric materials and chirality values.

### 4. RESULTS AND DISCUSSION OF PLANAR STRUCTURE

Fig. 2 shows the graph between the drain current (A) and the gate voltage (V) output characteristics for planar CNTFET. In this simulation, chirality values of 10.0 and 7.0 show higher resistance changes concerning length and analyze different parameters such as the channel length (10 nm), top gate length (8 nm), oxide thickness (8 nm). If the oxide thickness decreases, the issue of leakage current increases. To overcome these issues, we consider different dielectric materials such as silicon dioxide (SiO<sub>2</sub> = 3.9, marked in blue), yttrium oxide  $(Y_2O_3 = 16, marked in red)$ , hafnium dioxide (HfO<sub>2</sub> = 25, marked in green). In Fig. 2a (for a chirality value of 10.0), the drain current vs the gate voltage (log) shows that the on-current increases (-0.5 V) and the leakage current decreases by about  $0.5 \ \mu\text{A}$  in HfO<sub>2</sub>. In Fig. 2b (for a chirality value of 7.0), the drain current vs the gate voltage (log) shows that in  $HfO_2$  the on-current increases (-0.3 V) and the leakage current decreases by about  $-0.5 \ \mu$ A.



Fig. 2 – Drain current characteristics of planar CNTFET device with chirality of (a) 10.0 and (b) 7.0

Fig. 3 shows the graph between the potential (eV) and distance (nm) characteristics for planar CNTFET. In Fig. 3a (for a chirality value of 10.0), the potential (eV) vs the distance (nm) (log) shows that when using HfO<sub>2</sub>, the potential decreases less than that of  $Y_2O_3$ . In Fig. 3b (for a chirality value of 7.0), potential vs distance (log) also shows that when using HfO<sub>2</sub>, the potential decreases less than that of  $Y_2O_3$ .



Fig. 3 – Distance characteristics of planar CNTFET device with chirality of (a) 10.0 and (b) 7.0  $\,$ 

Fig. 4 shows the graph between the transmission coefficient and the energy output characteristics for planar CNTFET. In Fig. 4a (for a chirality value of 10.0), the energy (eV) vs the transmission coefficient (log) shows that transmission depends on the channel length. Analysis shows that the shortest nanotube in the metallic state is induced by contacts with the electrodes semiconducting state, and it is found that the shortest channel length is occupied in HfO<sub>2</sub>. Fig. 4b (for a chirality value of 7.0) also shows that transmission depends on the channel length, the shortest nanotube in the metallic state is induced by contacts with the electrodes semiconducting state, and it shortest nanotube in the metallic state is induced by contacts with the electrodes semiconducting state, and the shortest nanotube in the metallic state is induced by contacts with the electrodes semiconducting state, and the shortest channel length is occupied in HfO<sub>2</sub>.

Fig. 5 shows the graph between the DOS (arb unit) and the energy output characteristics for planar CNT-FET. In Fig. 5a (for a chirality value of 10.0), the energy (eV) vs the DOS (arb unit) (log) shows that the DOS in the contact and channel part of the nanotube is evaluated for different coupling parameters and that  $HfO_2$  has the highest coupling parameter of energy with DOS. Fig. 5b (for a chirality value of 7.0) also shows that the DOS in the contact and channel part of the nanotube is evaluated for different coupling parameters and  $HfO_2$  has the highest coupling parameter of energy with DOS.



**Fig. 4** – Energy characteristics of planar CNTFET device with chirality of (a) 10.0 and (b) 7.0

Fig. 6 shows the graph between the density and the distance output characteristics for planar CNTFET. In Fig. 6a (for a chirality value of 10.0), the density (\m) vs the distance (nm) (log) shows that in HfO<sub>2</sub> the density of electrons increases with the travelled distance of  $10^6$  nm. In Fig. 6b (for a chirality value of 7.0), the density (\m) vs the distance (nm) (log) shows that in HfO<sub>2</sub> the density of electrons increases with the travelled distance distance of  $10^5$  nm.





**Fig. 5** – DOS characteristics of planar CNTFET device with chirality of (a) 10.0 and (b) 7.0



Fig. 6 – Density characteristics of planar CNTFET device with chirality of (a) 10.0 and (b) 7.0

## 5. RESULTS AND DISCUSSION OF COAXIAL STRUCTURE

Fig. 7 shows the graph between the drain current (A) and the gate voltage (V) output characteristics for coaxial CNTFET. In this simulation, chirality values of 10.0 and 7.0 show higher resistance changes with respect to length. Different parameters are analyzed, such as the channel length (10 nm), top gate length

(8 nm), oxide thickness (4 nm), if the oxide thickness decreases, the issue of leakage current increases. To overcome these issues, we consider different dielectric materials such as silicon dioxide (SiO<sub>2</sub> = 3.9, marked in blue), yttrium oxide (Y<sub>2</sub>O<sub>3</sub> = 16, marked in red), and hafnium dioxide (HfO<sub>2</sub> = 25, marked in green). In Fig. 7a (for a chirality value of 7.0), the drain current vs the gate voltage (log) shows that the on-current increases (-1 V) and the leakage current decreases by about 0.5 µA in HfO<sub>2</sub>. In Fig. 7b (for a chirality value of 10.0), the drain current vs the gate voltage (log) shows that in HfO<sub>2</sub> the on-current increases (-1 V) and the leakage current decreases by about 0.5 µA.



**Fig. 7** – Drain current characteristics of coaxial CNTFET device with chirality of (a) 7.0 and (b) 10.0

Fig. 8 shows the graph between the potential (eV) and the distance (nm) characteristics for coaxial CNT-FET. In Fig. 8a (for a chirality value of 7.0), the potential (eV) vs the distance (nm) (log) shows that when using HfO<sub>2</sub>, the potential decreases less than that of Y<sub>2</sub>O<sub>3</sub>. In Fig. 8b (for a chirality value of 10.0), the potential vs the distance (log) shows that in case of HfO<sub>2</sub>, the potential decreases less than that of SiO<sub>2</sub>.

Fig. 9 shows the graph between the density and the distance output characteristics for coaxial CNTFET. In Fig. 9a (for a chirality value of 7.0), the density (\m) vs the distance (nm) (log) shows that the density of electrons increases in HfO<sub>2</sub> flow with a distance of  $10^6$  nm. In Fig. 9b (for a chirality value of 10.0), the potential (eV) vs the distance (nm) (log) shows that the density of electrons increases in HfO<sub>2</sub> flow with a distance of  $10^6$  nm.  $10^5$  nm.

L. RENUKA DEVI, N. ARUMUGAM, J.E. JAYANTHI ET AL.



Fig. 8 – Distance characteristics of coaxial CNTFET device with chirality of (a) 7.0 and (b) 10.0



Fig.  $9-{\rm Density}$  characteristics of coaxial CNTFET device with chirality of (a) 7.0 and (b) 10.0

## J. NANO- ELECTRON. PHYS. 13, 02026 (2021)

Fig. 10 shows the graph between the DOS (arb unit) and the energy output characteristics for coaxial CNTFET. In Fig.10a (for a chirality value of 7.0), the energy (eV) vs the DOS (arb unit) (log) shows that the DOS in the contact and channel part of the nanotube is evaluated for different coupling parameters and that  $HfO_2$  has the highest coupling parameter of energy with DOS. Fig. 10b (for a chirality value of 10.0) also shows in the contact and channel part of the nanotube is evaluated for different coupling parameters, and  $HfO_2$  has the highest coupling parameter of energy with DOS. Fig. 10b (for a chirality value of 10.0) also shows in the contact and channel part of the nanotube is evaluated for different coupling parameters, and  $HfO_2$  has the highest coupling parameter of energy with DOS.



Fig. 10 – DOS characteristics of coaxial CNTFET device with chirality of (a) 7.0 and (b) 10.0

Fig. 11 shows the graph between the transmission coefficient and the energy output characteristics for coaxial CNTFET. In Fig. 11a (for a chirality value of 7.0), the energy (eV) vs the transmission coefficient (log) shows that transmission depends on the channel length. Analysis shows that the shortest nanotube in the metallic state is induced by contacts with the electrodes semiconducting state, and it is found that the shortest channel length is occupied in HfO<sub>2</sub>. Fig. 11b (for a chirality value of 10.0) also shows that transmission depends on the channel length, the shortest nanotube in the metallic state is induced by contacts with the electrodes semiconducting state, and the shortest channel length is occupied in HfO<sub>2</sub>.



Fig. 11 – Energy characteristics of coaxial CNTFET device with chirality of (a) 7.0 and (b) 10.0

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#### 6. CONCLUSIONS

The simulation was successfully demonstrated for planar and coaxial geometries with different channel lengths, chirality values, top gate, oxide thickness, and various dielectric materials. From this simulation, it is observed that for a channel length of 10 nm, the top gate value is 8 nm and chirality values of 7.0 and 10.0 are achieved with different dielectric materials (SiO<sub>2</sub>,  $HfO_2$  and  $Y_2O_3$ ). From the analysis, it is observed that for planar structure with chirality values of 7.0 and 10.0, the on-current increases (-0.3 V) and the leakage current decreases by about  $-0.5 \,\mu\text{A}$  in HfO<sub>2</sub>. The potential value shows that when using HfO<sub>2</sub>, the potential decreases slightly in Y<sub>2</sub>O<sub>3</sub>. The transmission value depends on the channel length, and it is found that the shortest nanotube in the metallic state is induced by contacts, and the shortest channel length is occupied in HfO<sub>2</sub>. The DOS in the contact and channel part of the nanotube is evaluated for different coupling parameters and HfO<sub>2</sub> has the highest coupling parameter of energy with DOS. The density of electrons increases in  $HfO_2$  with the travelled distance of  $10^5$  nm. In coaxial geometry, for chirality values of 7.0 and 10.0, the on-current increases (-1 V) and the leakage current decreases by about 0.5 µA in HfO<sub>2</sub>. In case of  $HfO_2$ , the potential increases less than that of  $SiO_2$ . From the above observation, both planar and coaxial CNTFETs have improved the on-current, distance and channel length.  $HfO_2$  has the strongest coupling bond compared to other dielectric materials.

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# Дослідження впливу high-k діелектриків затвору та хіральності на характеристики нанорозмірного CNTFET

L. Renuka Devi<sup>1</sup>, N. Arumugam<sup>1</sup>, J.E. Jayanthi<sup>1</sup>, T.S. Arun Samuel<sup>1</sup>, T. Ananth Kumar<sup>2</sup>

<sup>1</sup> Department of ECE, National Engineering College, Kovilpatti, India

<sup>2</sup> Department of ECE, IFET College of Engineering, Villupuram, India

Польові транзистори з вуглецевих нанотрубок (CNTFETs) мають особливі властивості, такі як надвисока теплопровідність, балістичний транспорт, найвища густина струму та надзвичайно висока механічна міцність. Завдяки цим чудовим характеристикам очікувалося, що вони будуть використовуватися як матеріал для кабелів та як альтернативний матеріал каналів для розширення характеристик CMOS структур. У роботі обговорюються площинна та коаксіальна геометрії з різними значеннями хіральності, аналізуються різноманітні параметри з різними діелектричними матеріалами, такими як SiO<sub>2</sub>, HfO<sub>2</sub> та Y<sub>2</sub>O<sub>3</sub> для поліпшення струму  $I_{on}$ , а також підпорогових коливань. Це покращило такі характеристики пристрою, як робоча напруга та відношення  $I_{on}/I_{off}$ , густина/діаметр, потенціал/діаметр, енергія/DOS. Запропонований підхід забезпечує корисний та інтегративний метод виготовлення електронних пристроїв з нанорозмірних електронних матеріалів.

Ключові слова: CNTFET, Площинний, Коаксіальний, Хіральність.