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Single Electron Transistor Based Current Mirror: Modelling and Performance Characterization

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Current mirror is basic building block of amplifier, oscillator and comparator circuit. An ideal current mirror is independent of input power and temperature. The output current is constant mirrored image of input current. In order to avoid wrong equilibrium it must have high output impedance. This can be achieved by using super cascode formation. The single electron coulomb blockade structure provides low voltage operation and scaling of transistor to 10 nm. The Single Electron Transistor (SET) based CM is modeled and analyzed by simulation and the results shows improved performance of CM.

Keywords: Self-biased current mirror, MOS current mirror, Nano-scale MOSFET, Power dissipation, CMOS integrated circuit, Amplifier, Single Electron Transistor, Coulomb blockade, Cascode current mirror.

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1. BACKGROUND

The rapid growth in IC manufacturing leads to scaling of transistors to a nanometre range [1-3]. According to Gorden Moore the number of transistors per unit area in ICs becomes double after every 18 months [4]. Over a decade the size of transistors continues to decrease but it reached to optimum value in current years [5, 6]. The promising approach to continue scaling of transistor is single electron transistor (SET) architecture [7, 8].

In the semiconductor physics electron play a very important role. The flow of electron is from higher potential to lower potential [9]. The operation of field effect transistor is controlled by threshold voltage. So FET called as voltage controlled device and complementary BJT are current controlled device [10]. The output characteristic of field emitter transistor shows that width of channel plays an important role in the drain current conduction. Generally area of source is greater than drain. On the other hand scaling of transistors to nano-range leads channel length modulation (CLM) effect. The CLM causes the change in output current in the integrated circuits. To maintain the value of current constant in the electronic circuit the current mirror (CM) circuit is used. The CM is fundamental building block of amplifiers, filters, attenuators, OTA, current conveyors, analog to digital converters, digital to analog converters and VCO [11-13]. The current mirror causes the mirroring of the input current with output current irrespective of its loading. The need of future IC is compactness in size and accuracy of operation [14, 15]. For that purpose modelling of current mirror is important. In the modelling the hybrid combination of SET and CM gives reduced size, low power consumption and higher accuracy performance.

1.1 Basics of Current Mirror

The current mirror circuit is the basic building block of analog circuit design. The circuit which is forced, output current equal to input current. The designs which can be formed by current mirror are analog converters, oscillators and amplifiers [16]. Important characteristic of integrated circuit design is low-voltage operation, low power consumption, wide bandwidth and minimum area requirements therefore, and there is a growing need for new low-voltage analog circuit design [17, 18]. The VCO and delay locked loops are important circuits operated at low power with current mirror [19-21]. The basic block diagram of current mirror is as shown in Fig. 1.

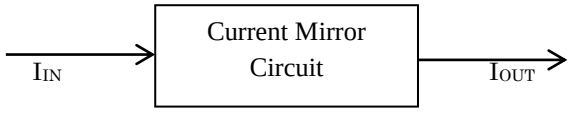

Fig. 1 – Block diagram of current mirror

Ideal current mirror has zero input resistance and infinite output resistance, which implies that the input voltage does vary with the input currents and the output currents are independent of applied voltage [23]. In reality a CM require minimum voltage at the output to ensure that the device operate in saturation [24]. This called the output compliance voltage. Accurate mirroring of the signal requires perfect matching of the mirroring transistor M_1 and M_2.

From Fig. 2 it is observed that if a transistor is biased at I_{REF}, then it produces $VGS = f^{-1}(I_{REF})$. Thus if this voltage is applied to the gate and source terminals of second MOSFET, the resulting current is $I_{OUT} = f f^{-1}(I_{REF}) = I_{REF}$ as shown in Fig. 2. From another point of view, two identical MOS devices that have equal gate source voltage and operate in saturation carries equal current (if $\lambda = 0$). From the figure having M_1 and M_2, neglecting channel-length modulation, the current relations can be expressed as,

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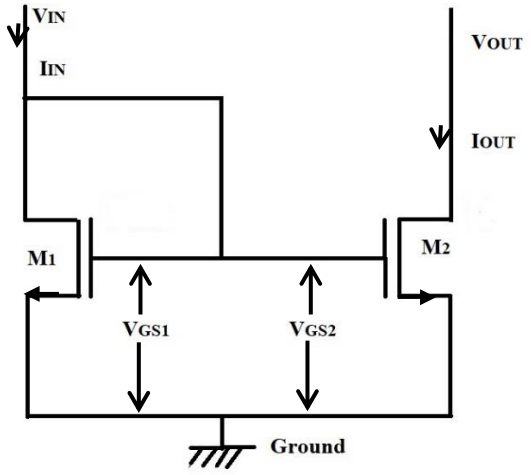

Fig. 2 - Basic MOS current mirror

$$I_{REF} = (1/2)\mu_n C_{ox}(W/L)_1(V_{gs}-V_{th})^2 \quad (1.1)$$

$$I_{OUT} = (1/2)\mu_n C_{ox}(W/L)_1(V_{gs}-V_{th})^2 \quad (1.2)$$

Dividing equation (2) by equation (1), the relation between I_{OUT} and I_{REF} is obtained as,

$$I_{OUT} = I_{REF}\,[(W/L)_2/(W/L)_1] \quad (1.3)$$

If width to length ratio of both transistors is same mirroring of current from input to output takes place.

1.2 Cascode Current Mirror

To remove out the drawback of basic current mirror the new structure is cascode current mirror. In cascode current mirror the two basic CM circuits are connected one above one i.e. in stacked form. This structure increases output resistance as well as increases gain of the CM [25]. The cascade CM is as shown in Fig. 3.

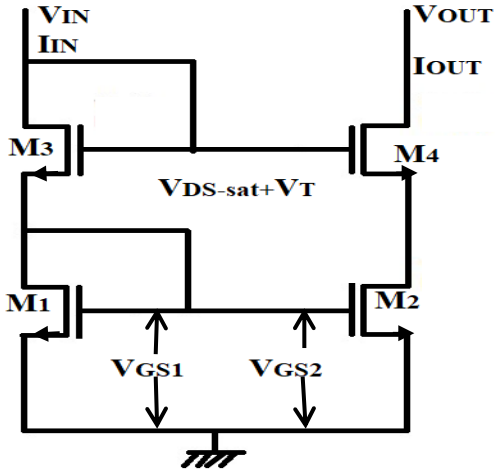

Fig. 3 – Cascode current mirror

The cascade structure is formed by using *n-p-n* MOSFET. In the previous circuit the effect of channel length modulation is not considered due to that accuracy of basic CM is less. This problem is overcome by cascode CM. For cascode CM small signal output resistance is given as,

$$r_{OUT} = r_{03} + r_{02}(1 + r_{03}(g_{m3} + g_{mb3})) \approx g_{m3}r_{03}r_{02} \quad (1.4)$$

Hence the output resistance of cascode CM is equal to output resistance of simple CM multiplied by gain of MOSFET M_3. This means by increasing cascode levels the output resistance of CM increases. But the main drawback is that this also increases the voltage headroom which not applicable for power saving structures [26].

1.3 Basics of Single Electron Transistor

In electronics transistor is most important device. The transistor can work as switch and amplifier. In computers transistors are used as tiny switches for turning ON and OFF. It is also used to amplify the signals. In modern days transistors are large in size but now a day's transistor size is reduced to nanoscale [27]. In a microchip now a days billions of transistors are available each one turning ON and OFF bullions time per second. Every year the size of transistor is reduced. In modern days to switch ON the transistor it requires 10 million electrons. But in present day transistor requires approximately 10 thousand electrons rather than moving many electrons through transistor it is necessary to move one electron at a time for better efficiency. This concept is called single electron phenomenon [28].

Fig. 4 shows single schematic of single electron transistor. The single electron transistor consists of conductive island dot separated by three conducting terminals [29]. These three connecting terminals are gate, source and drain. In this structure possible to add fourth gate terminal to form four terminal transistor devices. The SET structure consists of two tunnel junctions having high resistance (RD and RS). These high resistive junctions provide path for flow of electron. As these three electrodes are separate in between Quantum dot and electrode the capacitances formed are gate capacitance Cg, source capacitance Cs and drain capacitance Cd. The capacitance is also called as tunnelling capacitance [30]. Due to wave properties of electron tunnelling can easily done through barrier junction. The SET is in conduction when the voltage is applied to the gate terminal, this is Coulomb Blockade effect [31].

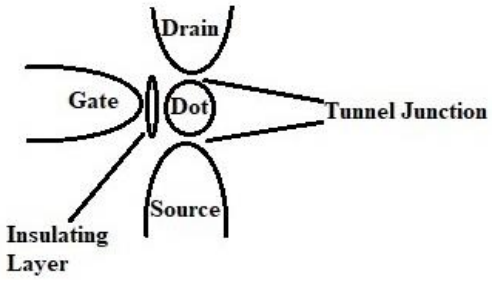

Fig. 4 – Schematic of single electron transistor

The quantum dot is nano-size particle. As the size of quantum dot is small, its capacitance decreases when size is large it has greater capacitance when the size is small the capacitance is small. So the size of quantum dot decreases its charging energy denoted by

wc increases. Charging energy is the energy needed to add the electron to the quantum dot. When this charging energy is greater than thermal energy it does not allow the electron to enter or exit from the quantum dot. So no electrons can tunnel to or from quantum dot [32]. So coulomb blockade is the charging effect which blocks the injection or rejection of a single charge in to or from a quantum dot.

For proper operation of CB effect:

a) The bias voltage is less than $V_b < e/c$. Where e is the electron charge and c is the capacitance of the junction;

b) The electrostatic charging energy must be greater than thermal energy $e^2/2c$;

c) Quantum hall resistance h/e^2 must be greater than tunnelling resistance.

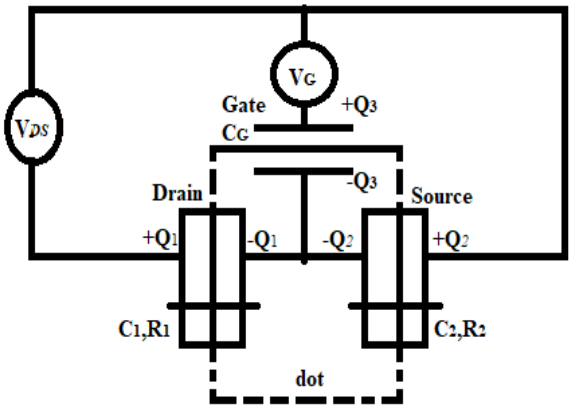

Fig. 5 – Voltage diagram of single electron transistor

Fig. 5 shows voltage diagram of single electron transistor. It consists of quantum dot having nano-size. Across this quantum dot three electrodes are placed these are source, drain and gate. In between source and drain it has quantum dot structure. Also it has capacitor between gate and the quantum dot. The capacitor tune the energy level of quantum dot to flow electron. The quantum dot (QD) structure is mesoscopic structure. The source acting as electron donor and drain acting as electron collector. QD acting as resister bellow the bias voltage based on energy level. When some voltage is applied to gate the capacitance will change and tune the energy level. This brings down the energy level to the fermi energy of source. This causes electron tunnel through the barrier junction and collected by drain terminal.

Fig. 6 shows energy level diagram of electron tunnelling. It has shadow region at left and right side these are source and drain. The source and drain are filled with electron, one electron is shown by dot. In between source and drain the central material is quantum dot. The quantum dot is nano size so that energy level of quantum dot is discrete in nature. There are two barriers first barrier is in between source and Quantum dot and another one is in between quantum dot and drain. Without bias the energy level of source electron is not matching with quantum dot so there is no conduction of electron. After providing bias in between drain and source still the energy level not change. If the voltage (V_g) applied to gate terminal the capacitance change between gate and quantum dot. The capacitance tune the energy level so it brings energy level to Fermi level of the source value. Due to tuning energy level electron tunnels through the barrier and quantum dot to reach at drain. Only one electron conduction occurs.

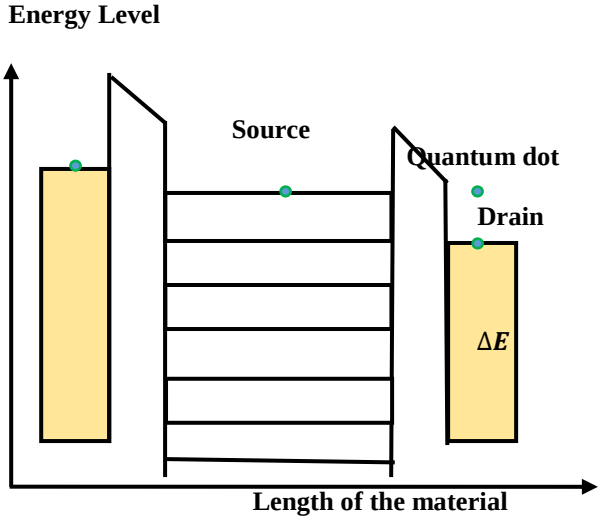

Fig. 6 – Energy level diagram of electron tunnelling

Fig. 7 shows equivalent circuit of an SET. It is in separate input and output form. It has four resistors, two diodes and two voltage sources. Drain source current-voltage characteristic ($I_{ds} - V_{ds}$) are shown by two branches, these are $R_2 - V_p$ and D_2 and R_3, V_p and D_3 respectively. To have positive and negative current flow in the source-drain bias the directions of voltage and diode are opposite. The charging energy is the cosine function of the gate bias voltage. These are shown as,

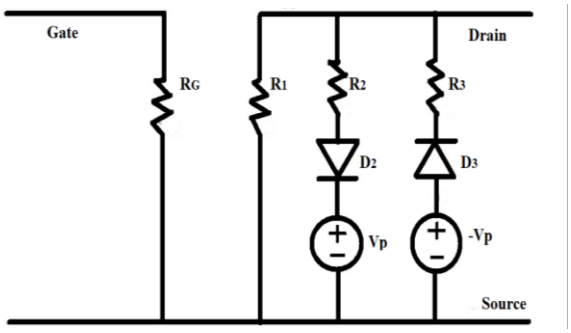

Fig 7 – Equivalent model of SET

$$R_1(V_g) = CR_1 + CR_2\cos(Cf_1 \cdot V_g), \quad (1.4)$$

$$R_2(V_g) = R_3(V_g) = CV_p/[CI_2 - 2CV_P/R_1(V_g)]. \quad (1.5)$$

From the above equation the *I-V* characteristic find out at various gate voltage.

In this paper, improved current mirror based on single electron transistor is proposed. By applying cascode configuration the MOSFETs are connected in stacked form which ensures high output impedance at output side. Section 2 described the proposed single electron based transistor current mirror architecture. In section 3 the result analysis of SET CM is discussed and presented in graphical form. Finally, conclusions are given in section 4.

2. METHOD

Previously the modelling of single electron transistor has been restricted by temperature. Due to this application of set are limited but today the modelling of set is independent of temperature range. The set model plays an important role in stable operation of set circuits. Set has advantages such as low voltage requirement, high output impedance and compact in size but has limitations like background charge effect and lower gain. Hybrid circuits are formed by cmos-set circuit architecture. The hybridization of set with cmos removes the limitations of set and high voltage gain and high speed driving.

2.1 The Model

The modelled CM is bilateral gate implemented self-biased current mirror. The circuit consists of four *n*-MOS field effect transistor and two SETs. The circuit is bilateral and symmetric which provides stable operation. The transistor M_1 and M_2 form basic current mirror in this the drain and gate terminal of M_1 are shorted to form diode connected configuration. The gate to source voltage of both transistors (V_{gs1} and V_{gs2}) are equal which ensures the output current is mirror image of input current. The V_g voltage provides control gate bias voltage to the quantum dot. This causes electrically induced quantum dot to provide high performance in terms of parasitic MOSFET operation.

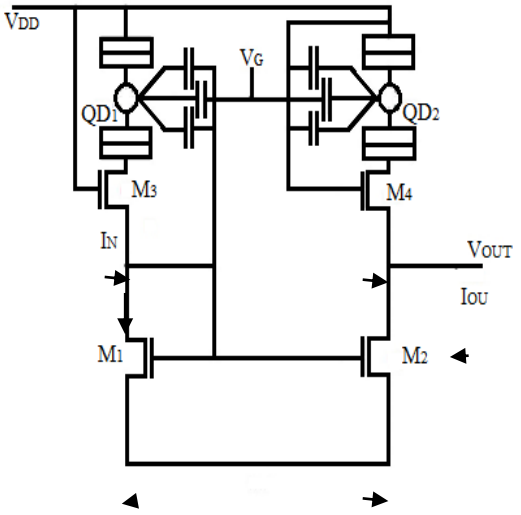

Fig. 8 – Single electron transistor based current mirror (SET-CM)

Imperial set modelling SET valley current modulates as per input voltage and better operation in terms of phase shift and coulomb oscillation period. This duplicates the complementary current to the output stage regardless of leakage current.

3. RESULTS

Tanner EDA is used to model the circuit and Monte Carlo simulation. The 1V input power supply used. Simulations are carried out to find out input characteristic, output characteristic and frequency response. At temperature $T = 30$ K the gate capacitance of SET is $C_g = 3.3$ af with junction capacitance of $C = 1.5$ af, the barrier resistance is $R = 100$ MΩ.

3.1 I-V characteristic

Fig. 9 shows IV_t characteristics of SET. Due to application of input voltage current starts to flow in the CM.

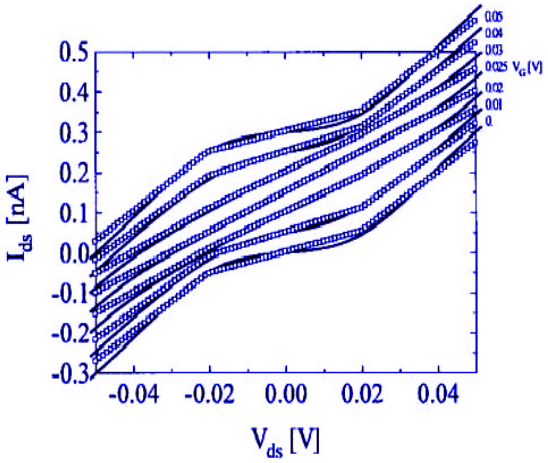

Fig. 9 – *I-V* characteristics

The current value is zero up to 0.5 V as input beyond this current starts increasing exponentially. The minimum compliance voltage obtained at the input side is 0.6 V; this implies that ACM has low input resistance.

3.2 *I-V* Characteristic at Various Temperature

Fig. 10 shows output characteristics of ACM. In VLSI output resistance should be high. The minimum compliance voltage obtained for the CM is 0.2 V.

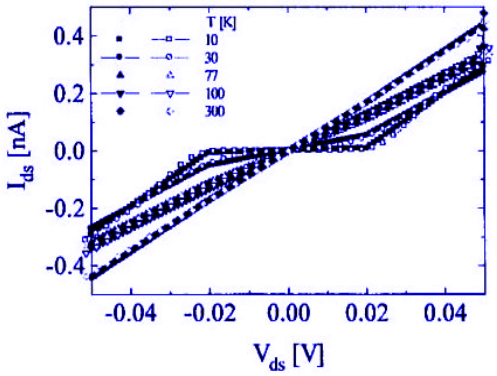

Fig. 10 – *I-V* Characteristic at Various Temperature Values

The specification of proposed CM with temperature is given in Table 1 and the values are compared with related CM circuit. It can be seen the output resistance significantly increased with minimum input resistance. In addition, its bandwidth is increased without sacrificing any performance.

Table 1 – Model parameters at various temperature

Temperature	10 K	30 K	80 K	100 K	300 K
CI_1 (nf)	0.21	0.22	0.25	0.27	0.37
CR_1 (GΩ)	1.35	0.3	0.18	0.15	0.1
CR_2 (GΩ)	1.2	0.1	0.01	0.005	0

4. CONCLUSION

In this paper, proposed current mirror using single electron transistor is presented. Using this technique input resistance and input compliance voltage get reduced to 5 Ω and 0.2 V respectively. The frequency response is stable in nature and relatively high. Simulation result support the utility of SET-CM for low voltage, high output resistance and high performance. The proposed SET-CM is simulated by Mentor Graphics Eldo-SPICE with a 18nm CMOS technology. Experimental results demonstrate that proposed SET-CM achieves significant improvement in output impedance and high degree of accuracy. In the future, we intended to extent hybrid SET-CM structure to a pure SET-CM structure consisting of single electron transistors to cope with temperature variation.

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