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An Ultra-low Power, High SNM, High Speed and High Temperature of 6T-SRAM Cell in 3C-SiC 130 nm CMOS Technology

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Semiconductor memories are becoming more and more present in the most hostile environments. In this paper, the electrical behavior of the 6T-SRAM memory cell in 3C-SiC in 130 nm CMOS technology was studied. The study of the effect of the cell ratio (CR), supply voltage (V_{DD}) and temperature (T) on the static noise margin (SNM), as well as the influence of temperature on write time showed that this cell is characterized by a low power ($P = 27$ nW), a high speed (write time $\tau_{write} = 0.305$ ns) and a wide noise margin (RSNM = 320 mV), and also it works under a low voltage $V_{DD} = 1.2$ V and a high temperature up to 350 °C. The comparison with the literature has shown that the 6T-SRAM cell in SiC with 130 nm CMOS technology is characterized by good electrical behavior and high electrical performance.

Keywords: 3C-SiC, BSIM3v3, CMOS, 130 nm technology, SRAM.

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1. INTRODUCTION

Conventional silicon circuits are limited in proper operation when the conditions of use are very severe (very high temperature, high magnetic and high electric fields, chemical aggressivity, strong irradiation, nuclear power plant, etc.). Due to this, the manufacture of circuits that can operate in these hostile environments is necessary. Large gap materials such as silicon carbide (SiC) replace advantageously silicon (Si) [1]. The latter is a material which is currently making great advances linked to a wide application field in electronics. Due to the main physicochemical properties of silicon carbide, such as thermal conductivity (5 W/K.cm), the large gap (3 eV), the very high critical electric field (3 MV/cm), the high electron saturation speed (2.10^7 cm·s^{-1}) and the high mobility on the order of 1000 (cm^2·V^{-1}·s^{-1}), SiC is well adapted to high power applications, high temperature, high frequency under radiations etc. [2, 3].

There are several polytypes of silicon carbide. Among these ones, 4H-SiC, 6H-SiC and 3C-SiC are the most used in electronics. A plenty of components such as diodes, bipolar transistors, field effect transistors and others have been produced and studied based on these polytypes in recent years.

During the last decade, digital systems based on electronic circuits have developed remarkably, particularly circuits integrating memory cells. Among the most popular of these memories are the Static Random-Access Memory (SRAM) cells. So, several recent researches have focused on the study of SRAM cells in terms of low voltage, low power, high noise immunity, high speed in different technologies, small dimensions and materials.

The study of MOSFETs and electronic circuits in SiC 130 nm submicron technology showed that they operate at low voltage and low power [4-7].

In this work, we will study the electrical behavior of the 6T-SRAM memory cell using N- and P-MOSFETs in 3C-SiC 130 nm technology. To carry out this study, we will see the influence of supply voltage V_{DD}, temperature T and cell ratio CR on different static noise margins (in retention HSNM, in writing WSNM and in reading RSNM) of this cell. To investigate the speed of the 6T-SRAM cell in 3C-SiC 130 nm technology, we will study the write time of this cell in a temperature range from 27 °C to 350 °C with $V_{DD} = 1.2$ V and CR = 3. Consequently, we will carry out a comparative study between our results and those in the literature. We use Cadence OrCAD (PSpice) as a simulation tool.

2. DESCRIPTION OF THE 6T-SRAM MEMORY CELL IN 3C-SIC

The architecture of six transistor SRAM memory is used to carry out this study. The 6T-SRAM is a simplified RS Flip-Flop made up of two back-coupled CMOS inverters (T_1, T_2, T_3 and T_4) and two NMOS transistors (T_5 and T_6) called access transistors, as shown in Fig. 1. PSpice parameters of N- and P-MOSFETs implanted in this cell are calculated using 3C-SiC 130 nm technology and the BSIM3v3 model.

For the SRAM cell, the static noise margin (SNM) is the most important characteristic. It is defined as "the minimum noise voltage that must be applied to the retention node's to toggle the state of the cell" [8]. There are three modes of SNM for an SRAM cell according to the different operations on this cell: in retention HSNM, in writing WSNM and in reading RSNM, the last one is the most important.

The SNM can be obtained graphically by the length of the side of the largest square that can be inserted between the two curves in the graph called "butterfly" as shown in Fig. 2 [2].

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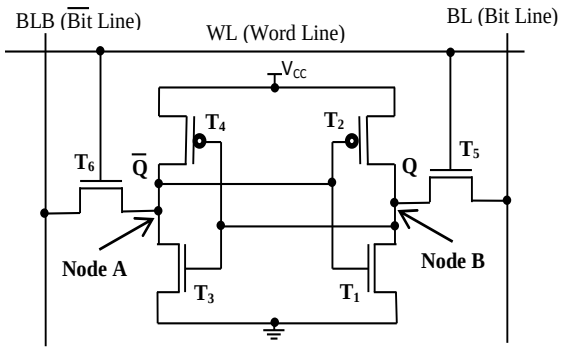

Fig. 1 – 6T-SRAM CMOS memory cell

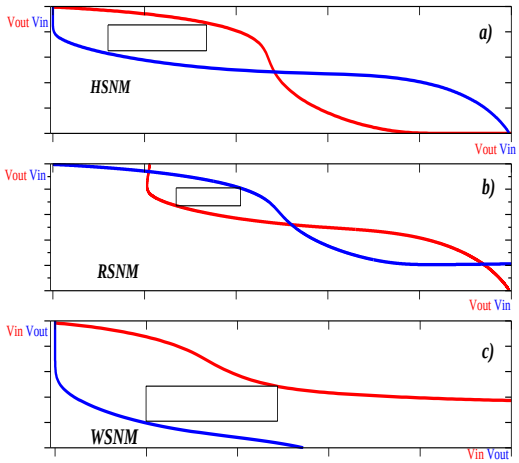

Fig. 2 – SNMs of an SRAM: a) HSNM, b) RSNM, c) WSNM

3. RESULTS AND DISCUSSION

3.1 Effect of Cell Ratio on SNM

To study the effect of the sizing of the transistors on the different noise modes, we must look at the influence of the geometric ratio between the inverter transistors and the access transistors, called the cell ratio (CR) [9]. The following relation gives it:

$$CR = \frac{W_1}{W_5} = \frac{W_3}{W_6} \text{ with } W_1 = W_3 \text{ and } W_5 = W_6, \quad (1)$$

where W_1, W_3, W_5 and W_6 are respectively the channels widths of the transistors T_1, T_3, T_5 and T_6. Fig. 3 shows the evolution of the two noise modes RSNM and WSNM as a function of CR of the 6T-SRAM cell in 3C-SiC technology for a supply voltage V_{DD} = 1.2 V and at room temperature.

The read static noise margin (RSNM) increases considerably with the increase in the CR ratio of the 6T-SRAM cell in 3C-SiC technology, while it decreases in write mode (WSNM) as shown in Fig. 3; and on the other hand, there is no influence of the CR ratio on the hold static noise margin (HSNM).

The increase in the CR has limits, because the access transistor should not be very small compared to the PMOS transistor (T_2) of the inverter, for a successful write operation. That is why we chose a CR equal to 3 in the study of the other effects.

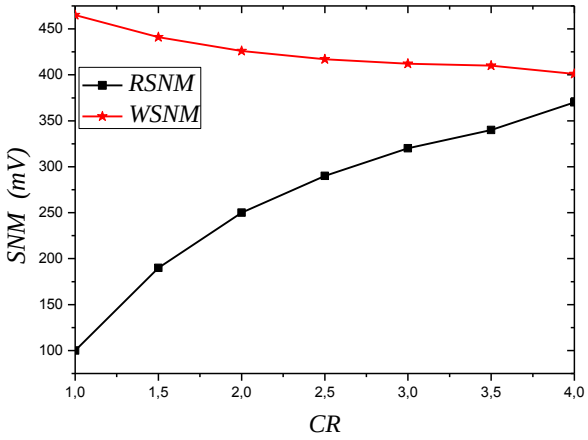

Fig. 3 – SNM as a function of CR (V_{DD} = 1.2 V)

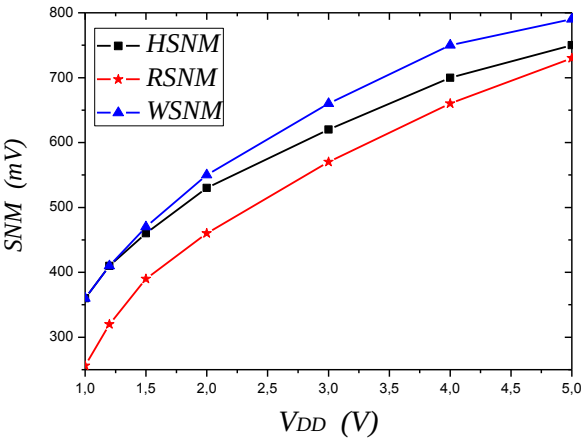

Fig. 4 – SNM as a function of V_{DD} (CR = 3)

3.2 Effect of Supply Voltage on SNM

To study the effect of the supply voltage on the functioning of the 6T-SRAM cell in 3C-SiC technology, we vary the V_{DD} voltage from 1 V to 5 V. This range of voltage is chosen to cover the different values of supply voltage V_{DD} used in literature (Table 1). After simulation, we get Fig. 4.

Fig. 4 shows the evolution of the noise margins as a function of the supply voltage V_{DD} of the 6T-SRAM cell in 3C-SiC at room temperature and with a cell ratio CR = 3. At the submicron dimensions, the different noise modes of the 6T-SRAM cell in 3C-SiC technology are directly proportional to the supply voltage V_{DD} as shown in Fig. 4, this shows that our cell works correctly as in the literature [8, 9].

The results show that the noise margins in HSNM and RSNM modes are the same at low supply voltage (V_{DD} < 1.5 V), as well as the 6T-SRAM cell in 3C-SiC technology is characterized by a low value of the noise margin in WSNM mode compared to other noise margin modes (HSNM and RSNM) in the range of the selected supply voltage.

Increasing the supply voltage increases the SNM but it simultaneously increases the dissipated power, which is not advised in digital electronics. For this, the value of the supply voltage V_{DD} = 1.2 V is chosen in this work to decrease the power dissipation.

3.3 Effect of Temperature on SNM

Temperature is a very important physical parameter in the electrical behavior of electronic components and circuits [4, 5, 10]. So, to study the influence of temperature on the different noise margin modes, we vary the temperature from 25 °C to 350 °C.

Fig. 5 shows the evolution of the different SNM modes as a function of the temperature of the 6T-SRAM cell in 3C-SiC technology for a supply voltage of 1.2 V and CR = 3. In the temperature range (T < 300 °C), the noise margin in HSNM mode decreases remarkably as a function of the temperature. On the other hand, the two other noise modes RSNM and WSNM decrease slightly (remain approximately constant). The different noise margins of this cell decrease considerably when the temperature becomes higher than 300 °C as shown in Fig. 5. This decrease of the SNM is always satisfactory for our cell according to the literature [11].

3.4 Write Time

Write time (τ_{write}) is defined as the necessary time for the cell to toggle from one state to another. This time is measured as the necessary time for Q to reach 90 % of its full voltage. Fig. 6 shows the switching of the output voltage Q from 0 V to 1.2 V of the 6T-SRAM memory cell in 3C-SiC technology at different temperature values with a supply voltage V_{DD} = 1.2 V.

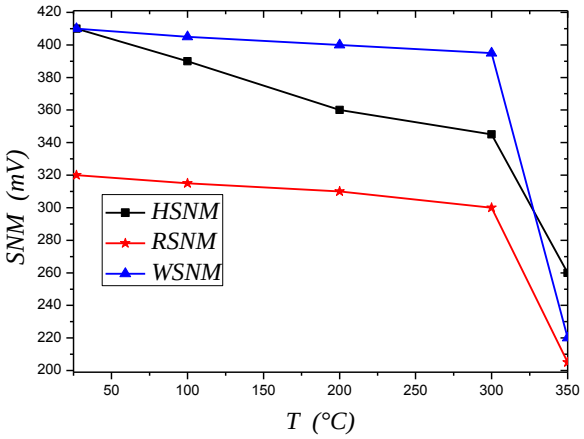

Fig. 5 – SNM as a function of temperature

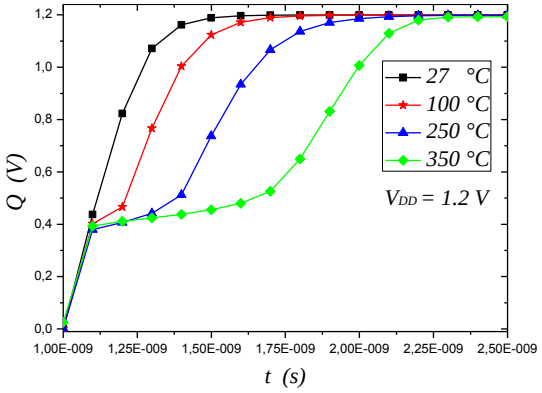

Fig. 6 – Output voltage Q as a function of time

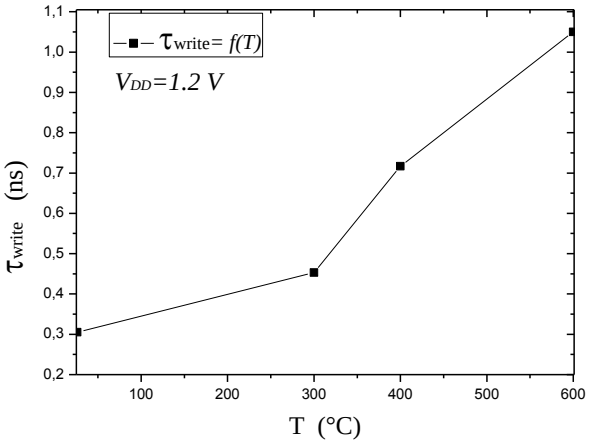

Fig. 7 – Write time as a function of temperature

Fig. 6 is used to plot the curve of Fig. 7, that shows the evolution of the write time as a function of temperature of the 6T-SRAM cell in 3C-SiC technology.

For the 6T-SRAM cell in 3C-SiC 130 nm technology, the write time is directly proportional to the temperature variation as shown in Fig. 7. This causes reduction in the write speed of this cell. This is due to the degradation of the charge carrier mobility when the temperature increases.

The results show that the 6T-SRAM cell in 3C-SiC submicron technology is characterized by a high write speed, and that it always remains functional at high temperatures about 350 °C, due to the good thermal properties of the 3C-SiC semiconductor.

Table 1 shows the properties of our 6T-SRAM cell in 3C-SiC 130 nm submicron technology, as well as the comparison between our results and those in the literature.

Table 1 – Properties of 6T-SRAM in 3C-SiC compared to other different 6T-SRAMs

References	Technology (nm)	V_{DD} (V)	Power dissipation	τ_{write} (ns)	RSNM (mV)
[12]	180	1.8	519.7 nW	0.1913	350
	90	1.2	59.58 nW	0.5141	170
[13]	180	1.8	1.0909 mW	21.981	200
[14]	180	1.8	1.69 µW	0.267	400
[15]	130	1.5	76.5 µW	/	300
[11]	130	1.2	/	/	180
This work	130	1.2	27 nW	0.305	320
		1.5	37 nW	0.219	390
		1.8	48 nW	0.184	440

The write time is inversely proportional to the variation of the supply voltage of the 6T-SRAM cell in 3C-SiC 130 nm submicron technology as shown in Table 1. This leads to an increase in the write speed of this cell. The results obtained show that the 6T-SRAM cell in 3C-SiC designed using 130 nm technology is characterized by low power dissipation, a high write speed and a large noise margin in RSNM mode compared to other cells which have used 180 nm and 130 nm technologies, even those which are designed using 90 nm technology [12] proposed in the literature.

4. CONCLUSIONS

This work focused on the design and the study of SRAM in 3C-SiC 130 nm technology. During this work, we simulated this cell according to the study of static noise margin (SNM), the effect of the cell ratio (CR) and the supply voltage on functioning, as well as the effect of temperature on the noise margin and the write time. The results obtained showed that the write static noise margin (RSNM) increases when the cell ratio increases and/or if the supply voltage increases, while the margin decreases and the write time increases with temperature rise. Also, the cell produced has good characteristics in terms of low voltage, low power, submicron dimension, and temperature resistance; this is what is required in embedded electronics.

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Комірка пам'яті 6T-SRAM з наднизьким енергоспоживанням, високим SNM, швидкодією і високою температурою в 3C-SiC за 130 нм технологією CMOS

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У роботі було вивчено електричну поведінку комірки пам'яті 6T-SRAM в 3C-SiC за 130 нм технологією CMOS. Вивчення впливу співвідношення комірок (CR), напруги живлення (V_{DD}) і температури (T) на статичний запас шуму (SNM), а також впливу температури на час запису показало, що така комірка характеризується низькою потужністю (P = 27 нВт), високою швидкістю (час запису τ_{write} = 0,305 нс) і широким запасом шуму (RSNM = 320 мВ), а також працює при низькій напрузі V_{DD} = 1.2 В і високій температурі до 350 °C. Порівняння з літературою показало, що комірка пам'яті 6T-SRAM в SiC за 130 нм технологією CMOS характеризується гарною електричною поведінкою та високими електричними характеристиками.

Ключові слова: 3C-SiC, BSIM3v3, CMOS, 130 нм технологія, SRAM.