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Numerical Simulation of FinFET Transistors Parameters

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Complementary afin field-effect transistors (FinFET) with high parameter stability and low power consumption are used as power supplies, amplifiers, frequency converters in sensors and electronic equipment, as well as high-frequency switching generators and modulators in medical devices for welding biological tissues. Results of 3D numerical simulation of *p*- and *n*-types of SOI TG FinFET transistors are presented. The structure of 3D devices based on SOI (Silicon-On-Insulator) technology with TRI-GATE (TG) shutter is described and modeled using SILVACO TCAD tools. The current-voltage characteristics have been constructed, and allowable values of leakage current and threshold voltage of *n*- and *p*-transistors with gate electrodes have been calculated on the basis of film systems with effective outputs of 4.40 eV and 4.85 eV. The implementation of multi-gate film electrodes based on Ni and Ta is essential for the digital design of ultra-large integrated circuits (VLSI). The simulation results allow us to determine the permissible values of the threshold spread, the DIBL, the leakage current, and the coefficient I_{on}/I_{off}. The basis of the design of transistor structures is to study the operating parameters of the transistor in the open state and the geometric dimensions of the individual structural elements. These results may be used for designing the 3D CMOS transistors.

Keywords: SOI TG FinFET, Short-channel effects, Effective work function, Threshold voltage, High-*k* dielectric.

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1. INTRODUCTION

A fin field-effect transistors (FinFET) are the basis for modern complementary metal-oxide-semiconductor (CMOS) technology. Miniaturization of the components and low energy consumption make it possible to use them as switching power supplies, amplifiers, frequency converters in electronic equipment [1, 2], sensors [3-6], as well as high-frequency switching generators and modulators in medical surgical devices for high-frequency and ultrasonic welding of biological tissues [7, 8].

Nowadays, as CMOS components the «Silicon-on-Insulator» TRI-GATE FinFET (SOI TG FinFET) transistors are most commonly used. But, while the general geometric parameters (gate length (L_G), structure's thickness (T_{FIN}), height (H_{FIN}), etc) are decreased there are observable short-channel effects (SCEs). Besides, with decreasing L_G value the following parameters change: subthreshold swing (SS), drain induced barrier lowering (DIBL). Moreover, as an additional negative effect the decrease in the threshold voltage *Vt* is observed [9-11].

Fin alloying impurities concentration is also a key parameter that influenses the SS and DIBL values and carrier mobility. In case of high electron mobility the doping concentration must be as low as possible. But, decrease in doping concentration leads to DIBL increase and SS decrease. It is well-known that for FinFET technology a pure fin-channel is desirable.

However, to improve leakage current control, low level of Fin-channel doping is acceptable with inpurities concentration of 10^{15}-10^{17} cm^{-3}. In case of leakage and drain contact areas the higher impurities concentration (10^{19}-10^{21} cm^{-3}) are necessary [11, 12]. As a solution of described problems the following modern techniques are used: ion implantation, in situ epitaxial doping close to leakage and drain, etc. So, in this case it is possible to observe the increase of Fin-channel's resistance.

In recent years 3D numerical simulation techniques are widely used [11-15] and they allow to obtain the necessary data in technology designing and electrophysical properties. In [12], a three-dimensional conical SOI TG FinFET model is presented that is similar to a real device. This model was designed using Silvaco TCAD program package with description of type of materials and Fin-channel doping profile.

Study of FinFET's working parameters in condition of their conductivity and model's geometric dimensions is used as a basis of these structures designing.

2. NUMERICAL SIMULATION PROCEDURE

SOI TG FinFET transistor structures are designed using the Silvaco TCAD [15]. This program package is a set of specialized programs connected with each other. «DeckBuild» application is a basis program because of its possibility to create and implement the command files. This program can also set the actions order and allows to implement other programs and their further co-ordination. Other general applications are «Atlas» device simulation package and «Tony Plot» visualization set. «Atlas» forms three types of excluding files: the first file is outgoing working time which represents the information about simulation progress and provides the information about errors and alerts during simulation; the second file is a log file which accumulates all terminal voltages and currents during the device analyzing; the third file is a solution file which accumulates the 2D- and 3D-grafical data, that are connected to changes in values in a determined working point.

Fig. 1 presents the FinFET transistors simulation algorithm in Silvaco TCAD environment using «Atlas» application. On the basis of experimental data there were simulated a corresponding devices and their working characteristics.

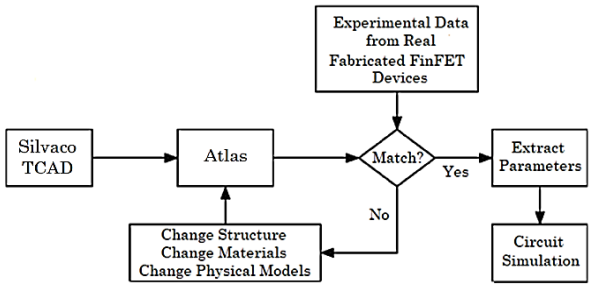

Fig. 1 – Simulation algorithm

It should be noted that Silvaco TCAD library models structure is universal, so the same module may be used in all applications. The own C-interpreter is used in "Silvaco". It is designed especially for optimized machine codes obtaining using the basis model description. Build-in C-interpreter codes debugging interface allow to significantly decrease the compilation time [14].

3. WORK FUNCTION

Vt threshold voltage saves almost the same values for different channel's doping concentrations but its value significantly depends on the electron work function for gate electrode or on the so-called "effective work function" (EWF or W_{eff}). In work [1], the optimal value of W_{eff} for FinFETs is determined as 4.40 eV and 4.85 eV in case of *n*-type and *p*-type conductivity devices, respectively. W_{eff} values for planar *n*- and *p*-MOS transistors are 4.2 eV and 5.0 eV, respectively depending on their working regime.

Using the experimental data on W_{eff} value of individual components it is possible to calculate this characteristic in case of film systems according to the following concentration dependence:

$$W_{eff} = \sum_{i=1}^{n} c_i \cdot W_{eff_i}, \qquad (1)$$

where W_{effi} and c_i are the effective work function and concentration of individual metal components in films based on Ni and Ta, respectively.

As it has been shown earlier, W_{eff} value for gate electrode determines device's type of conductivity. For CMOS structures designing it is necessary to have data on the corresponding W_{eff} values of metal electrodes. But this value significantly depends on a wide range of factors, among which metal layers thicknesses and their topologies [15], substrate (isolator) material, etc. [18, 19].

Among them the FinFETs designing technology provides their thermal processing at high temperatures. In work [18], it was studied the influence of concentration and thermally activated diffusion in different FinFET systems. TiN typical electrode was additionally doped with chemical stable to oxidation tantalum (Ta) and nickel (Ni) metals. These metals have standard work functions in vacuum conditions W_f (Ta) = 4.25 eV and W_f (Ni) = 5.05 eV. It has been shown [16] that combination of materials with low and high values of W_{eff} influences general electrophysical properties of the electrode. TiN(10)/Ta(10) structure is characterized by low values of W_{eff}: 4.35 eV and 4.40 eV before and after thermal annealing at 500 °C, respectively, while in TiN(5)/Ni(10)/Ta(2) system it was observed the effect of W_{eff} increase by 0.4 eV before annealing procedure, i.e. 4.75 eV. Moreover, after thermal annealing procedure (TiN/Ni/Ni_xTa_y/Ta system) at 500 °C this value is close to the previous (4.74 eV). Carried out measurement based on equation (1) allows us to determine the work function for described earlier electrodes: 4.41 eV in case of Ta and 4.82 eV in case of Ni, respectively. The difference in work function values for *p*-type electrodes may be caused by the formation of Ni_xTa_y alloy or solid solution. So, this data was not checked by us. It should be also noted that for gate electrodes designing the complex nitrides and carbides of metals, their alloys gain higher attention of researchers.

It is also necessary to highlight among them the dependences of work functions on concentrations of the individual components [1]. Moreover, a study of the influence of condensation and thermally activated diffusion on film systems phase compositions also gains higher attention of researchers [17-21].

4. DEVICE STRUCTURE

In this section we present the results of 3D numerical simulation of SOI TG FinFET structures using Silvaco TCAD instruments.

Gate electrodes have the following values of work functions: W_{eff} = 4.40 eV in case of *n*-FinFET and W_{eff} = 4.85 eV in case of *p*-FinFET, which may be formed based on TiN(10)/Ni(10) and TiN(6)/Ni(12)/Ta(2) film systems. So, the W_{eff} value of film systems may be matched by the variative part of corresponding components concentrations. But, during the simulation in Silvaco TCAD environment only electrodes EWF are taken into acount. So, in our proposed models, Ni/Ta conductor with described above characteristics was used as EWF gate electrode. HfO_2 (k = 22) layer with a thickness of 2 nm was used as a high-k dielectric. To calculate the electrical characteristics of SOI TG *n*- and *p*-FinFETs, taking into account the geometric dimensions dependence, the following models were used. The first model, according to measured in [12], has gate length L_G = 30 nm, Fin-channel's thickness and height T_{FIN} = 20 nm and H_{FIN} = 50 nm, respectively.

The second model (Fig. 2) has the following parameters: L_G = 14 nm, T_{FIN} = 8 nm and H_{FIN} = 20 nm respectively. According to [10], the geometrical ratios L_G:T_{FIN} and H_{FIN}:T_{FIN} were 3:2 and 5:2, respectively.

Basis parameters of film structures for *n*- and *p*-type devices are presented in Table 1. Devices working characteristics are simulated by Atlas Silvaco environment.

For *n*-type and *p*-type devices designing it was used the corresponding doping procedure by *p*-type and *n*-type impurities with low volume concentration of 5×10^{15} cm^{-3} of Fin-channel and with higher concentration of 5×10^{17} cm^{-3} in drain and source contact areas. A concentration distribution of impurities in SOI TG *n*-FinFET channel is demonstrated in Fig. 2b.

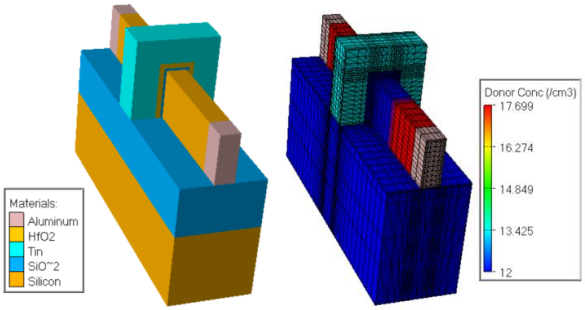

Fig. 2 – SOI TG *n*-FinFET 3D-model in case of the structure demonstration (a) and of impurities concentration distribution (b)

Table 1 – Basis parameters used for SOI TG FinFET simulation

Device parameters	*n*-type device	*p*-type device
Body doping concentration, cm^{-3}	$5 \cdot 10^{15}$	$5 \cdot 10^{15}$
Drain/Source doping concentration, cm^{-3}	$5 \cdot 10^{17}$	$5 \cdot 10^{17}$
Gate length, nm	30/14	30/14
Equivalent oxide thickness EOT, nm [8]	1.2	1.2
Fin width, nm	20/8	20/8
Fin height, nm	50/20	50/20
Buried oxide thickness, nm	20	20
Substrate thickness, nm	30	30
Effective work function EWF, eV	4.40	4.85

5. SIMULATION AND RESULTS

During the 3D transistors simulation procedure the following values of the work function are used: W_{eff} = 4.40 eV in case of *n*-FinFET and W_{eff} = 4.85 eV in case of *p*-FinFET. Devices are simulated in case of drain bias voltage of 0-1.2 V and in case of gate bias voltage close to 0.8 V for *n*- and *p*-FinFET the corresponding value was used in a negative range. It was estimated that drain saturation current I_{dsat} for SOI TG FinFETs with gate lengths of 30 nm and 14 nm was 1.14×10^{-6} A and 8.21×10^{-6} A in case of *n*-type devices or 2.99×10^{-7} A and 8.04×10^{-6} A in *p*-type devices, respectively. Fig. 3a presents the typical I_{DS}-V_{DS} curves for *n*-SOI TG and *p*-FinFET with the gate length L_G = 14 nm, Fin-channel's thickness and height T_{FIN} = 8 nm and H_{FIN} = 20 nm, respectively. Threshold voltage was estimated for drain's bias of 0.1 V, while the gate's voltage was varied in the range of 0-1.2 V for *n*-FinFET and 0-(– 1.2) V for *p*-FinFET (Fig. 3b).

Simulation results showed the following values of threshold voltages *Vt* in case of devices with gate lengths of 30 nm and 14 nm: 0.327 V and 0.318 V for *n*-FinFET and 0.329 V and 0.326 V for *p*-FinFET, respectively. It was also estimated that similar values of SS for *p*-FinFET and *n*-FinFET are observed.

Estimated SS values for transistors with gate lengths of 30 nm and 14 nm are 63.9 mV/decade and 62.7 mV/decade (in case of *n*-FinFET) or 64.2 mV/decade and 62.9 mV/decade (in case of *p*-FinFET), respectively. Current in «switch-off» condition (I_{off}) was estimated using the drain voltage V_{DS} = 1.2 V and gate voltage V_{GS} = 0 V

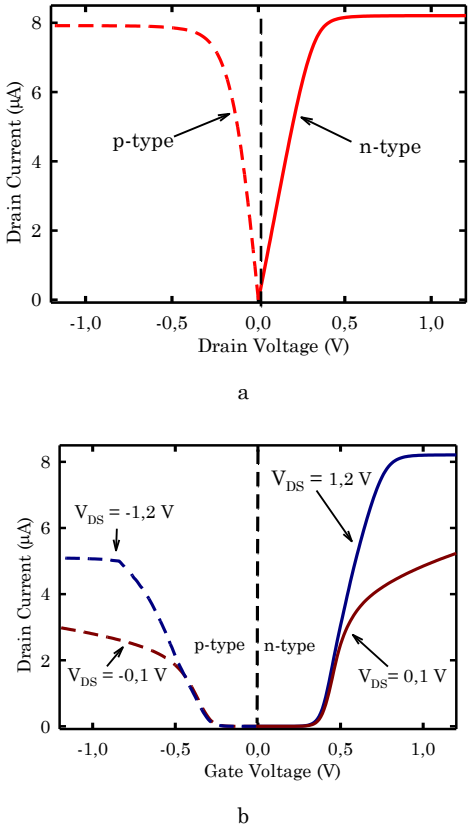

Fig. 3 – I_{DS}-V_{DS} (a) and I_{DS}-V_{GS} (b) characteristics of SOI TG *n*-FinFET and *p*-FinFET

in case of *n*-FinFET; in case of *p*-FinFET the value of drain voltage was V_{DS} = – 1.2 V. In case of transistors with gate lengths of 30 nm and 14 nm I_{off} was 7.85×10^{-13} A and 8.75×10^{-13} A (in case of *n*-FinFET), 4.72×10^{-13} A and 5.78×10^{-13} A (in case of *p*-FinFET).

Current in «switch-on» condition (I_{on} was estimated using the drain voltage V_{DS} = 1.2 V and gate voltage V_{GS} = 0 V in case of *n*-FinFET; in case of *p*-FinFET the value of drain voltage was V_{DS} = – 1.2 V. In case of transistors with gate lengths of 30 nm and 14 nm I_{on} was 7.58×10^{-6} A and 8.21×10^{-6} A (in case of *n*-FinFET); 4.42×10^{-6} A and 5.25×10^{-6} A (in case of *p*-FinFET). These data correlate well with the earlier obtained results of other authors [11-13].

Current ratio coefficient I_{on}/I_{off} has a significant role in digital designing; it is also well-known as very large scale integration (VLSI). VLSI coefficient was calculated in case of drain voltage V_{DS} = 1.2 V and in case of gate voltage variation in the range of 0-1.2 V for FinFET these data were negative. In case of transistors with gate lengths of 30 nm and 14 nm I_{on}/I_{off} coefficient was 9.6×10^6 and 9.4×10^6 (*n*-FinFET) or 9.3×10^6 and 9.1×10^6 (*p*-FinFET). Simulation results allow us to conclude that designed transistors have a high level of efficiency.

Moreover, in case of VLSI it is necessary to have a lower value of the DIBL parameter. This parameter is calculated as a two-threshold voltage ratio at fixed drain voltages. The first voltage is a low drain voltage V_{DS1} = 0.1 V, the second is a higher level of drain voltage V_{DS2} = 1.2 V. At the gate lengths of 30 nm and 14 nm the

DIBL values were 51 mV/V and 71 mV/V (n-FinFET); 58 mV/V and 77 mV/V (p-FinFET), respectively. These DIBL values are higher than estimated in works [14-16] that may be caused by the different structure geometries. Decreasing DIBL values may be realized by using an additional drain/source contact and by using the drain with individual shielding plane [21].

6. CONCLUSIONS

SOI TG FinFET structures were successfully designed and studied by the influence of EWF, gate materials and model geometries varying their working characteristics. Models with the gate length of 14 nm have better values than the models with gate length of 30 nm. However, high DIBL values are observed in both cases that may be caused by chosen Fin-channels geometries. Also, proposed n- and p-type transistor models demonstrated allowable values of subthreshold swing, drain induced barrier lowering, drain current, etc. This allows us to conclude that obtained simulation results may be used for designing the 3D CMOS transistors.

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Числове моделювання параметрів FinFET транзисторів

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Комплементарні польові метал-окисел-напівпровідник (МОН) транзистори з високою стабільністю параметрів та низьким енергоспоживанням використовуються як джерела живлення, підсилювачі, перетворювачі частоти в сенсорах та електронному обладнанні, а також як високочастотні комутаційні генератори та модулятори в медичних приладах для високочастотного і ультразвукового зварювання біологічних тканин. У роботі наведені результати 3D-числового моделювання p- та n-типів транзисторів SOI TG FinFET. Побудовано вольт-амперні характеристики, розраховані допустимі величини сили струму витоку та порогової напруги n- та p- транзисторів з електродами затвору на основі плівкових систем з ефективними роботами виходу 4,40 еВ і 4,85 еВ. Реалізація мультизатворних плівкових електродів на основі Ni і Ta має важливе значення для цифрового проектування надвеликих інтегральних схем. Результати моделювання дозволили визначити допустимі значення допорогового розкиду, зниження бар'єру, спричинене стоком, силу струму витоку та коефіцієнт I_{on}/I_{off}. Основою проектування транзисторних структур є вивчення робочих параметрів транзистора у відкритому стані та геометричних розмірів окремих структурних елементів. Результати моделювання можуть бути використані для проектування 3D-транзисторів CMOS.

Ключові слова: SOI TG FinFET, Короткоканальні ефекти, Ефективна робота виходу, Порогова напруга, High-k діелектрик.