

Impact of the High- K Dielectric Material as Spacer on Analog and RF Performance of the GS-DG-FinFET

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In multi-gate technology, the DG-FinFET is an emerging structure due to its better electrostatic control over the channel. This paper shows a systematic study of the structure, double gate (DG) FinFET, which has been modified using the high- K dielectric material as the gate stack (GS) and spacer engineering which is going to boost its properties. The analyzed SCEs are sub-threshold slope (SS), drain induced barrier lowering (DIBL), and the switching current ratio (I_{ON}/I_{OFF} ratio). The analog performance of the devices is studied on the basis of parameters are transconductance (g_m), trans-conductance gain factor (TGF), the output conductance (g_d), drain current (I_D), early voltage (V_{EA}), intrinsic gain (A_V). The RF performance is analyzed on the merits of parasitic gate capacitance (C_{gd} , C_{gs} and C_{gg}), cutoff frequency (f_T), gain frequency product (GFP), and transconductance frequency product (TFP). With this we intended to provide a comparative study to suggest the possibility for better performance of the GS-DG structure at $V_{DS} = 0.05$ V and 1.0 V. Here, DIBL exhibits 49.8 % and SS value is decreased by 32.65 %. For the analog performance study, the V_{EA} is raised by 4.31 %, the TGF of the device is improved by 33.9 % and the gain has been also improved as compared to the conventional one. The simulation is carried out considering 45 nm node parameters according to the ITRS road map for the high-speed applications and low power consuming circuits.

Keywords: Gate stack-double gate-FinFET, Spacer engineering, Intrinsic capacitances, High- K , SCEs.

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1. INTRODUCTION

High- K dielectric materials are vital for next-generation low power, low leakage and high performance logic devices [1, 2]. The gate oxide leakage increases with decrease in SiO_2 thickness, and also SiO_2 is running out of atoms for further scaling [3]. Due to these reasons, the continual gate oxide scaling will require the use of high- K dielectric materials. FinFETs were introduced to avoid problems due to downscaling of MOSFET size, i.e. to reduce short channel effects (SCEs) like drain induced barrier lowering (DIBL), hot electron effects etc. [4, 5]. The spacer engineering is a technique, which can be used for further improvement of device performance by reducing the SCEs [6]. Use of high- K spacer enhances the fringing electric fields through the spacer [5, 6].

The fin shaped field effect transistor (FinFET) is widely adopted in semiconductor industries for its high performance and low-power applications due to great scalability and high electrostatic control. Gate-stack (GS) high- K dielectrics are introduced in order to control the SCEs [8]. Double-gate (DG) FinFET is a suitable structure because of its high performance, high speed and low-power applications [7, 9, 10, 11].

It is in recent years that the FinFETs are being considered as the radio frequency (RF) technology of choice. The rapid downscaling of FinFET structure is one of the important parameters in the growth of IC industries. The status of analog and RF figures of merit (FoM) is essential to measure the reliability of the structure with very good performance [12]. The performance can be analyzed by showing low drain induced barrier lowering (DIBL), sub-

threshold slope (SS) [13] and high gate transconductance (g_m), early voltage (V_{EA}), cut-off frequency (f_T), etc. The dependence of these FoMs on the device structure will help to understand the SCE challenges.

In this paper, the introduction section gives a brief idea about the use of high- K dielectric material, spacer technique, and GS-DG-FinFET and analog/RF performances. The next section gives the pictorial representation of different DG-FinFET structures with proper dimensions. The first subsection deals with the analog performance analysis of different parameters like variation of transconductance (g_m), transconductance gain factor (TGF), the output conductance (g_d), drain current (I_D), early voltage (V_{EA}), intrinsic gain (A_V) as a function of the gate over the drive voltage (V_{GS}) for fixed drain to source voltage (V_{DS}). The next subsection involves the RF performance analysis which is observed through the variation of gate to source capacitance (C_{gs}), gate to drain capacitance (C_{gd}), total gate capacitance (C_{gg}), cut-off frequency (f_T), gain frequency product (GFP), transconductance frequency product (TFP) as a function of gate to source voltage (V_{GS}) with constant drain to source voltage (V_{DS}). Finally, section 4 contains the conclusions, which summarizes the analog and RF performances performed on the different DG-FinFET structures.

2. DEVICE DIMENSION AND SIMULATION SETUP

Here, three different structures of DG-FinFET with high- K material as GS with an interfacial oxide SiO_2 and spacer are considered to compare their digital pa-

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rameters, analog and RF FoMs. The analysis is carried out through these structures to study the improvement in the carrier mobility, reduction in the leakage current and increase in the output conductance. (Fig. 1) shows the cross-sectional view of the three different device structures with GS and the spacer engineering, wherein Fig. 1a is a conventional DG-FinFET denoted as D1, Fig. 1b is GS-DG-FinFET denoted as D2 and Fig. 1c is GS-DG-FinFET with spacer denoted as D3. The device description has been considered in accordance with the ITRS roadmap [11] and it is shown in Table 1.

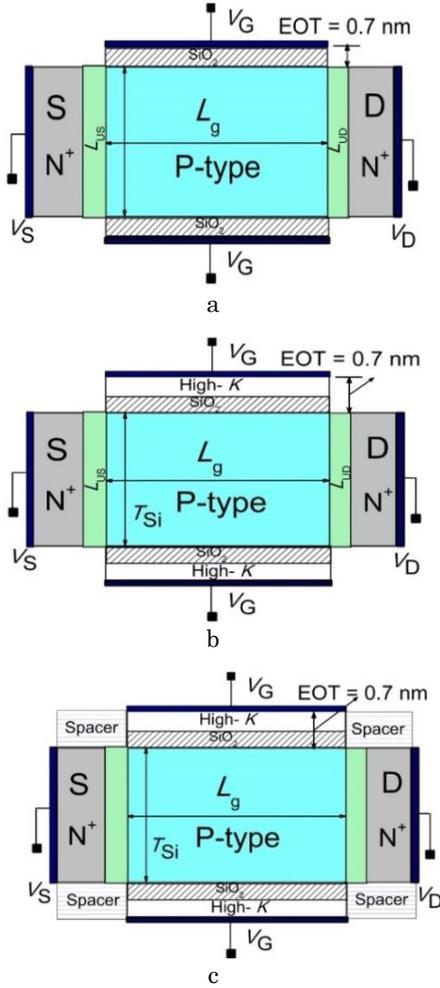


Fig. 1 – Schematic view of DG-FinFET (a), GS-DG-FinFET (b), GS-DG-FinFET with spacer (c)

In all three structures, both the length of the gate (L_g) and the ratio of length of the source (L_s) to length of the drain (L_d) i.e. L_s/L_d are taken as constant. The silicon layer thickness (T_{Si}) is taken as 10 nm. The doping concentration is uniformly distributed throughout the channel of about 10^{16} cm^{-3} for p -type semiconductor material and 10^{20} cm^{-3} for n -type source and drain regions. The effective oxide thickness (EOT) is fixed for all three structures at 0.7 nm. The three different models named as D1, D2 and D3 have been presented here in Fig. 1. The structures are calibrated to meet to requirement of the ITRS roadmap [11] semiconductor for 45 nm physical gate length. In our investigation, the HfO_2 and Si_3N_4 are considered as high- K dielectric ma-

terial and spacer material respectively [16]. In all cases, the gate metal work function is maintained at 4.6 eV. The threshold voltage is chosen as 0.45 V for better result (among the different values of V_{TH}). Two different sources to drain voltages (V_{DS}) have been tested with the values of 0.05 V and 1.0 V, respectively.

The 2D device simulator tool [13], TCAD, is used to simulate the DG-FinFET with high- K or metal gate. As per ITRS rule, the supply voltage V_{DD} is kept fixed at 1.0 V [11]. To study the analog performance, the simulation is carried out with variation of V_{GS} from 0 to -1.0 V keeping the drain to source $V_{DS} = 0.5$ V (which is half of the $V_{DD}/2$), as per the literature study [17]. The V_{TH} is extracted using constant drain current I_D . The V_{GS} is extracted from the V_{TH} value and it is an important parameter due to which the circuit is amplified as it decides the operated region. The V_{GS} value increases with increasing drain current till it reaches the saturation point. Hence the analysis is carried out for all analog and RF FoMs against V_{GS} . By the help of the tool, various modeling methods are taken into consideration to obtain the accuracy of the device. The mobility degradation model is being carried out inside the inversion regions. Due to the scattering effect, the degradation, which occurs near the interfacing layers of the semiconductor to insulators, the simulation is carried out by activating Arora mobility model, to determine the doping dependence parameter set. This model describes the carrier velocity, which works under the saturation with the impact of the high electric field. It also describes that the mobility of the carriers is degraded due to the influence of the Coulomb scattering effect. The Shockley-Read-Hall (SRH) [14] recombination model is used to include the carrier generation and recombination model. Furthermore, the simulation is incorporated using the enhanced Lombardi model for the study of the effect of high- K mobility degradation of carriers in the silicon inversion layer [15].

Table 1 – Device parameters taken for the simulation

Parameters	Values
n^+ -type (Arsenic doping concentration) at source/drain regions	10^{20} cm^{-3}
p -type (Boron doping concentration) at channel region	10^{16} cm^{-3}
Channel length (L_g)	20 nm
Effective oxide thickness (EOT)	0.7 nm
Silicon body thickness (T_{Si})	10 nm
The thickness of SiO_2 layer (T_{OX1})	0.2 nm
The thickness of HfO_2 layer (T_{OX2})	0.5 nm
Gate thickness (T_g)	10 nm

3. RESULT ANALYSIS

DIBL and SS are the SCEs, which are noted as important parameters for discussion. When the interaction of the depletion regions of the drain and the source takes place near the channel region for lowering the surface potential barrier, this leads to the occurrence of DIBL. It is enhanced due to the high drain voltages and short channel lengths. Therefore, this induces leakage current and injected hot carriers for the gate oxide layer [18]. The parameters are calculated as per the equations (1) and (2) [20]:

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{DS}} = \frac{V_{th1} - V_{th2}}{V_{DS2} - V_{DS1}}, \quad (1)$$

$$SS(mV/dec) = \frac{\partial V_G}{\partial(\log I_D)}. \quad (2)$$

In (1), the threshold voltages V_{TH1} and V_{TH2} are calculated at V_{DS1} and V_{DS2} , which are two different drain voltages of 0.05 V and 1.0 V respectively. A steep SS is an important measure for the device to get into turn-off state and the ideal value is 60 mV/decade for conventional multi-gate MOSFET [18]. The extracted values of DIBL and SS for all three devices are tabulated in Table 2. By comparing the values of the three devices, it is observed that the structure D3 exhibits the lowest DIBL value of 26.32 mV/V, whereas the SS and I_{ON}/I_{OFF} ratio are found minimum for D3.

Table 2 – Extracted parameters for devices with different configurations

Device	DIBL (mV/V)	SS (mV/decade)		I_{ON}/I_{OFF} ratio	
		$V_{DS} = 0.05$ V	$V_{DS} = 1.0$ V	$V_{DS} = 0.05$ V	$V_{DS} = 1.0$ V
D1	105.26	97.98	96.28	6.08×10^4	1.16×10^5
D2	52.63	67.998	68.101	1.38×10^7	4.42×10^7
D3	26.32	68.330	68.320	2.43×10^7	4.82×10^7

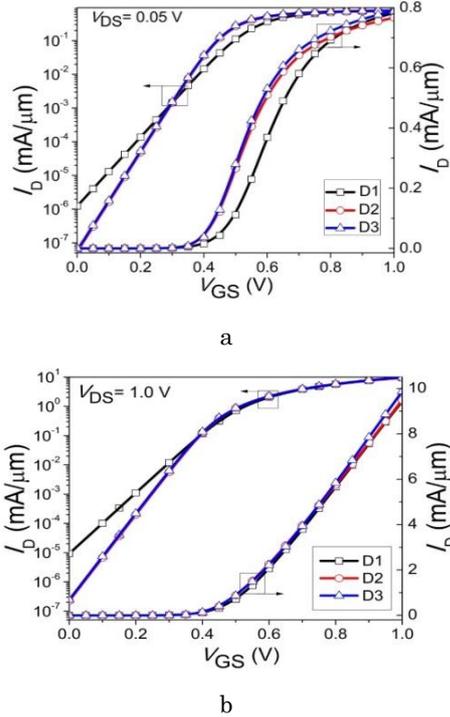


Fig. 2 – I_D - V_{GS} characteristics for the devices under study at (a) $V_{DS} = 0.05$ V, (b) $V_{DS} = 1.0$ V

The steep slope of SS is an important parameter of the device due to which it turns off [16]. In this investigation, among the three devices D3 shows a good agreement with the typical value of SS which is nearly equal to 60 mV/decade according literature survey and due to which it can be claimed for better immunity to the SCEs [19, 20].

The transfer curve of the I_D - V_{GS} in linear and logarithmic scale is shown in Fig. 2. Fig. 2a and Fig. 2b

show the drain current responses at $V_{DS} = 0.05$ V and 1.0 V respectively. The value of V_{TH} of the three devices is taken around 4.5 V from different values for better result. From the results it is clear that the I_{OFF} varies from 10^{-9} A/ μ m to 10^{-10} A/ μ m for all three devices. From Fig. 2b, it is observed that when the high-*K* material is introduced with the single oxide layer device that is D2 and D3, results increased I_{ON} as well as I_{OFF} due to fringing field effect. The gate leakage current reduces due to stacking effect. Also coupling capacitance increases by decreasing the leakage current [16, 18].

3.1 Analog Performance

The important FoMs of the devices are transconductance (g_m), output conductance (g_d), early voltage (V_{EA}), intrinsic gain (A_v), transconductance generation factor (TGF) and cut-off frequency (f_T) [20]. The FoMs on RF performances are discussed in the subsection 3.2 of this paper as an extended work to make a comparative study among the three devices.

In this section, the devices govern better SCEs, so it is important to understand the analog performances, taking the two parameters g_m and the TGF all together as a function of V_{GS} as shown in Fig. 3. The higher transconductance is achieved at lower values of V_{GS} and shows better result in case of the device D3. Hence, incorporating the spacer engineering in the DG-FinFET with gate stacking improves the device performances. The transconductance (g_m) value of the devices is calculated as:

$$g_m = \partial I_D / \partial V_{GS}. \quad (3)$$

At the minimum value of the sub-threshold, the TGF enhances the performances of the analog circuit when operating at low source voltages. From Fig. 3b, it is evident that devices D2 and D3 that is double layer (device with GS) and the device with the spacer concept show better performances and result as compared to the single layer device (D1).

The output conductance (g_d) and drain current (I_D) against the drain to source voltage are measured at two different values of V_{GS} , i.e. at 0.05 V and 1.0 V, and are shown in Fig. 4 for the above mentioned three different devices. The output conductance is shown in linear scale and I_D versus V_{DS} curve is shown in logarithmic scale. The output conductance (g_d) is calculated as per the equation:

$$g_d = \partial I_D / \partial V_{DS}. \quad (4)$$

As per the graph shown in Fig. 4a, the I_D against V_{DS} increases with higher permittivity value of the high-*K* material for the single layer configuration [18, 9]. So, D1 shows higher value of I_D versus V_{DS} as compared to other three structures, whereas D2, D3 show close responses.

As per the literature study, the CMOS analog circuits having transistors should have low g_d in order to achieve high gain [19]. In saturation region, the value of g_d is high as the output resistance is low due to which there is an increase in I_D versus V_{DS} . Hence, lower value of g_d propagates a higher drain current (I_D) to output conductance ratio is known as the early voltage (V_{EA}) [20]. Fig. 5 shows the plots of V_{EA} and the intrinsic gain A_v .

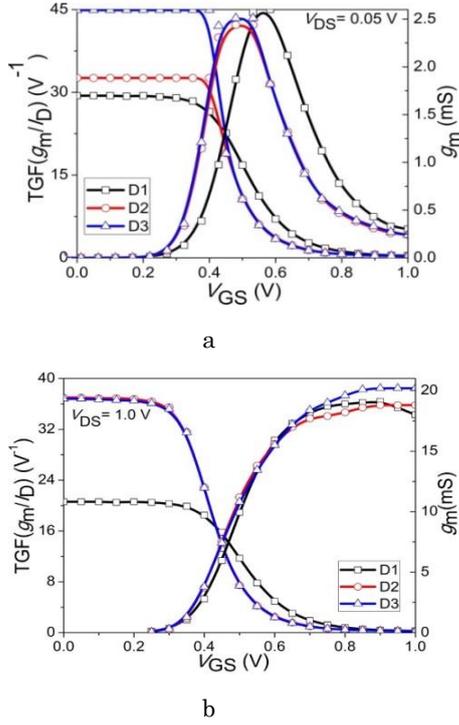


Fig. 3 – Transconductance (g_m) and transconductance generation factor (TGF) for (a) $V_{DS} = 0.05$ V, (b) $V_{DS} = 1.0$ V

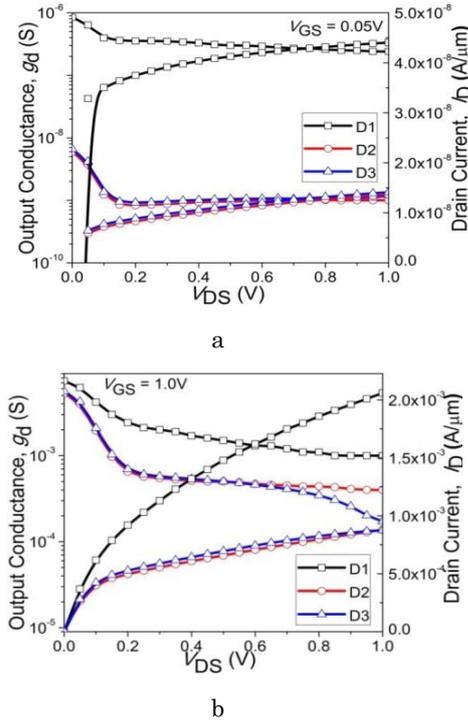


Fig. 4 – Output conductance (g_d) and I_D as a function of V_{DS} for V_{GS} of (a) 0.05 V, (b) 1.0 V

Table 3 – Analog performance of devices for $V_{DS} = 0.05$ V

Devices	g_m (S)	g_d (S)	V_{EA} (V)	TGF (V^{-1})
D1	2.60×10^{-3}	8.46×10^{-7}	1.39	29.4
D2	2.83×10^{-3}	5.96×10^{-9}	1.23	32.6
D3	2.96×10^{-3}	6.58×10^{-9}	1.17	44.9

$$V_{EA} = I_D / g_d, \quad (5)$$

$$A_v = g_m / g_d = (g_m / I_D) V_{EA}. \quad (6)$$

The V_{EA} and A_v have been calculated from the equations (5) and (6). As per the results in Fig. 5, the device D3 shows higher early voltage as compared to the other three devices and in case of intrinsic gain. Intrinsic gain is calculated from (6) and is represented in logarithmic scale shown in the graph. There, D1 shows low gain as compared to other structures and D3 shows better results for gain (in dB). By comparing the extracted data among the three devices, shown in Table 3 and Table 4, D3 shows better results for V_{EA} , gain and TGF for the two different voltages at $V_{DS} = 0.05$ V and $V_{DS} = 1.0$ V.

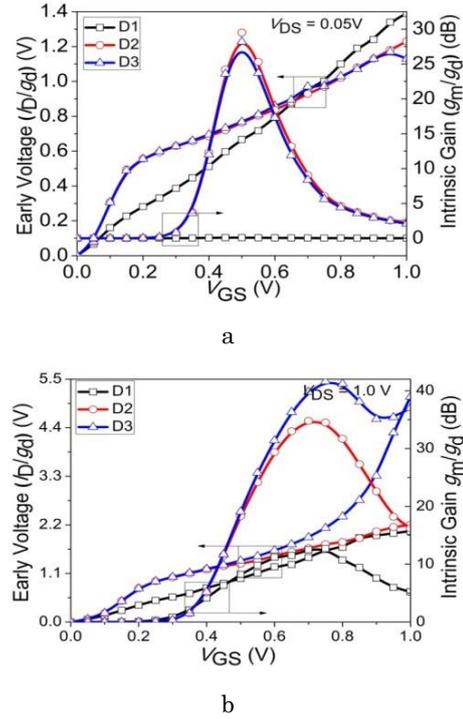


Fig. 5 – Early voltage (V_{EA}) and intrinsic gain (A_v) for V_{DS} of (a) 0.05 V, (b) 1.0 V

Table 4 – Analog performance of devices for $V_{DS} = 1.0$ V

Devices	g_m (S)	g_d (S)	V_{EA} (V)	TGF (V^{-1})
D1	1.50×10^{-2}	7.38×10^{-3}	2.06	20.6
D2	1.56×10^{-2}	5.32×10^{-3}	2.20	37.0
D3	1.63×10^{-2}	5.61×10^{-3}	5.10	36.8

3.2 RF Performances

The important RF parameters include the transconductance frequency product (TFP), gain frequency product (GFP) and gain transconductance frequency product (GTFP). Intrinsic capacitances like gate to source capacitances (C_{gs}) and gate to drain capacitances (C_{gd}) [18, 20] are shown in Fig. 6. The total gate capacitance (C_{gg}) [20] is measured by taking all the capacitances of the device in both the sub-threshold and strong inversion regions against V_{GS} as shown in Fig. 7.

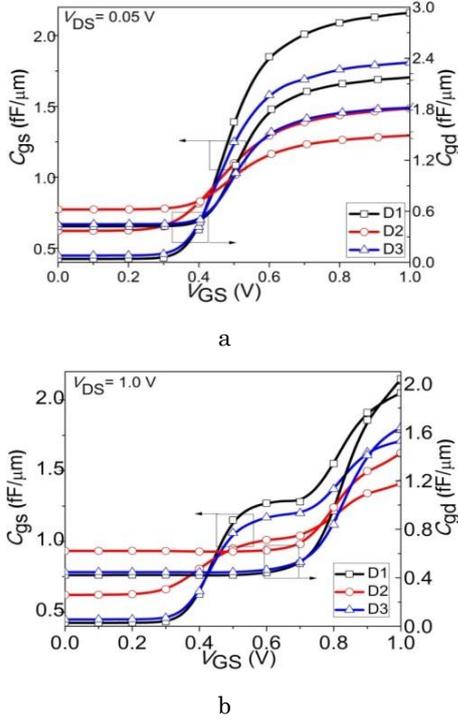


Fig. 6 – Intrinsic capacitances against V_{GS} : (a) gate to source capacitances (C_{gs}), (b) gate to drain capacitances (C_{gd})

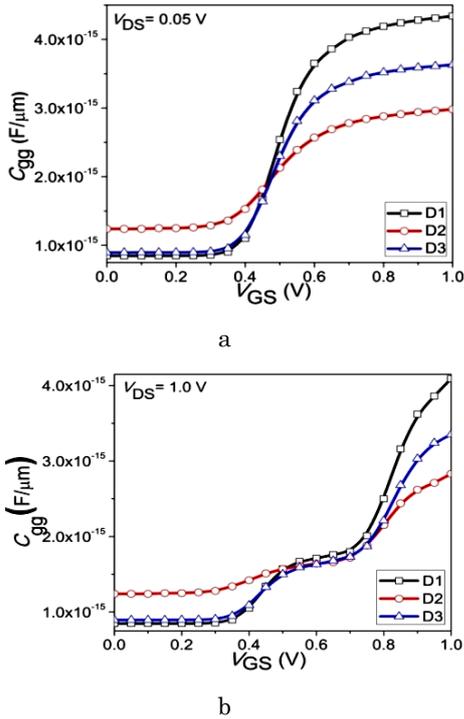


Fig. 7 – Capacitance C_{gg} against V_{GS} for V_{DS} (a) 0.05 V, (b) 1.0 V

The simulation has been carried out for the structures to study the AC small-signal analysis to extract the values of C_{gs} , C_{gd} and C_{gg} after the post-processing simulation of DC analysis. The AC analysis is done for the frequency of 1 MHz with a ramp voltage of 0 to 1 V and with the step size of 0.025 V. By comparing the three structures, it came into picture that the device with the high-*K* gives high values of the capacitances.

So, for D3 (GS-DG-FinFET), the values of the intrinsic capacitances due to the use of spacer in the structure show a contradictory result as compared to D2. This puts an appreciable impact on the cut-off frequency, which is discussed, in the next figure. The capacitances C_{gs} , C_{gd} and C_{gg} increase with increasing V_{GS} until both the values reach the saturation level. And after that they become constant without putting any effect on the junction. The cut-off frequency (f_T) is an important RF parameter and the performance is evaluated by using

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \quad (7)$$

where g_m , C_{gs} and C_{gd} are the transconductance, the gate to source capacitance and the gate to drain capacitance respectively.

In Fig. 8, the structure with gate stacking concept as gate oxide shows better result as compared with single layer device. Among the three devices, D3 shows higher value of f_T . This shows superiority on the gate controllability, higher transconductance and lower parasitic capacitances as compared to other devices in our study.

$$GFP = (g_m/g_d) \times f_T, \quad (8)$$

$$GTFP = (g_m/g_d) \times (g_m/I_D) f_T, \quad (9)$$

$$TFP = (g_m/I_D) \times f_T. \quad (10)$$

The GTFP, GFP and TFP are some unique FoMs in case of the RF analysis. GTFP is an important parameter of discussion given in Table 5 and Table 6, which is calibrated by both the switching speed and the intrinsic gain.

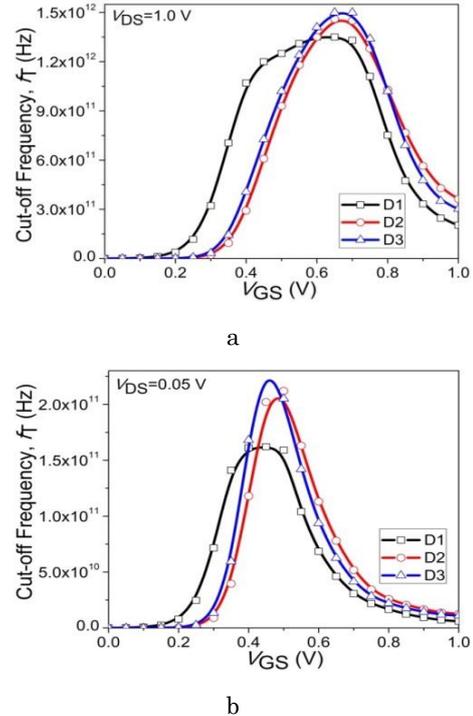


Fig. 8 – Cut-off frequency (f_T) as a function of V_{GS} for (a) $V_{DS} = 0.05$ V, (b) $V_{DS} = 1.0$ V

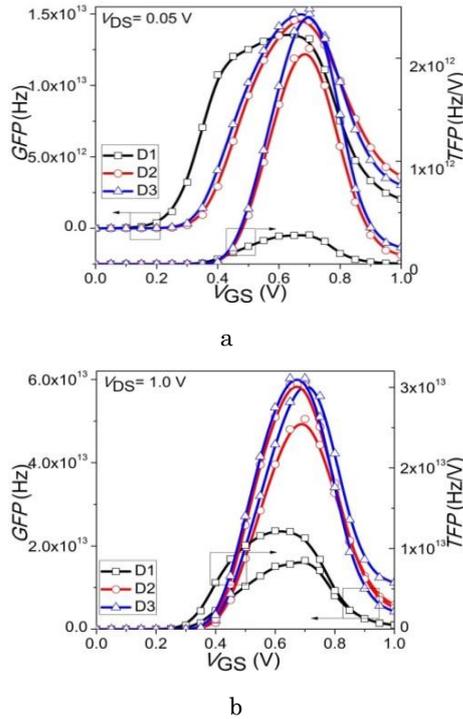


Fig. 9 – GFP and TFP as a function of V_{GS} for (a) $V_{DS} = 0.05$ V, (b) $V_{DS} = 1.0$ V

Table 5 – RF performance of devices for $V_{DS} = 0.05$ V

Devices	C_{gg} (fF)	f_T (GHz)	GFP (GHz)	TFP (GHz/V)	GTFP (GHz/V)
D1	4.34	162.00	1.35×10^4	1.41×10^5	7.72×10^5
D2	2.98	212.11	1.45×10^4	1.04×10^6	4.60×10^5
D3	3.63	236.59	1.50×10^4	1.23×10^6	8.95×10^5

Table 6 – RF performance of devices for $V_{DS} = 1.0$ V

Devices	C_{gg} (fF)	f_T (GHz)	GFP (GHz)	TFP (GHz/V)	GTFP (GHz/V)
D1	4.09	135.00	1.65×10^4	1.22×10^4	1.42×10^5
D2	2.83	146.63	5.05×10^4	3.03×10^4	1.05×10^5
D3	3.35	150.89	5.98×10^4	3.11×10^4	2.97×10^5

Here D3 shows better GTFP by trading off among the gain, transconductance and speed. And this is due to the higher value of f_T , g_m and lower value of g_d . The other FoM GFP calculated as per (8) is important for the operational amplifier in high frequency applications. Similarly, TFP given in (10) is represented as a trade-off between power and bandwidth and its utilization takes place from medium to high-speed applications.

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Both the GFP and TFP are shown in Fig. 9, which is plotted in linear and logarithmic scale respectively against V_{GS} for the V_{DS} of 0.05 V and 1.0 V. The plotting shown for GFP and TFP gives an idea that the two parameters increase linearly as V_{GS} increases in the sub-threshold region and in the saturation region, the values after decrease hold an optimal value. As per the comparative study, GS structure shows better results for GFP and TFP of about 7.09 % and 33.91 % respectively as the g_m and f_T values are high for the same structure.

4. CONCLUSIONS

The analog and RF FoMs have been investigated considering three DG-FinFET structures. No high- K dielectric and no spacer are used in D1; in the second structure, high- K dielectric material is used without spacer, and in the third structure both high- K dielectric and spacer are used. Complete device structure and simulation have been performed on Sentarus TCAD software. The different device performances have been analyzed by keeping the work function constant of about 4.6 eV.

The simulation results in Table 2 show that the structure D3 exhibits the lowest DIBL value of 26.32 mV/V, whereas by keeping a constant V_{DS} value of 0.05 V and 1 V, the SS and I_{ON}/I_{OFF} ratio are found less for D2 and D3 as compared to structure D1. Structure D1 shows low gain as compared to other structures, and structure D3 here shows better results for gain (in dB). By comparing the simulation results of the three devices, structure D3 shows better results for V_{EA} , gain and TGF for the two different voltages at $V_{DS} = 0.05$ V and $V_{DS} = 1.0$ V. The structure with gate stacking concept as gate oxide shows better result as compared with single layer device. Among the three devices, D3 shows higher value of f_T that is equal to 150.89 GHz at V_{DS} value of 1.0 V.

While comparing the GS-DG-FinFET, which is the D2 structure, with D3 structure, which is the GS-DG-FinFET with spacer, structure D3 has shown improvement in the DIBL, V_{EA} , f_T , GTFP, GFP, and TFP. By comparing the above said parameters, D3 gives better result in case of analog performances and has suitability towards RF performances. Therefore, this structure is preferable for the analog and RF performances of the circuit design giving the key emphasis on the spacer engineering on the DG-FinFET structure having GS engineering and without it. Henceforth, in the future work further modification can be done using gate-stacking concept with the spacer engineering so that a single device can be simulated for the analog and RF performance circuit design.

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Вплив high-*K* діелектричного матеріалу як буфера на аналогові та радіочастотні характеристики GS-DG-FinFET

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У багатоканальній технології транзистор DG-FinFET є новою структурою завдяки кращому електростатичному контролю над каналом. У роботі представлено дослідження транзистора FinFET з подвійним затвором (DG-FinFET), який був модифікований за допомогою high-*K* діелектричного матеріалу як стека затворів (GS) та спейсерної інженерії, що здатна покращити його властивості. Характеристики транзисторів DG-FinFET, GS-DG-FinFET і GS-DG-FinFET зі спейсерною конфігурацією порівнюються до показників якості короткоканальних ефектів (SCEs), аналогових і радіочастотних застосувань. Проаналізовані показники якості SCEs, такі як підпороговий нахил (SS), індуковане стосом зменшення бар'єру (DIBL) та відношення струмів переключення (I_{ON}/I_{OFF}). У роботі аналогова ефективність пристроїв досліджується на базі таких параметрів, як транспровідність (g_m), коефіцієнт посилення транспровідності (TGF), вихідна провідність (g_d), струм стоку (I_D), рання напруга (V_{EA}), внутрішнє посилення (A_v). Радіочастотна ефективність аналізується на основі показників якості паразитної ємності затвора (C_{gd} , C_{gs} та C_{gg}), порогової частоти (f_T), коефіцієнта посилення частоти (GFP) і частотного коефіцієнту транспровідності (TFP). При цьому ми намагалися провести порівняльне дослідження, щоб запропонувати можливість поліпшення характеристик структури GS-DG при $V_{DS} = 0,05$ В та 1,0 В. Тут параметр DIBL демонструє величину 49,8 %, а значення SS зменшилося на 32,65 %. Виходячи з дослідження аналогової ефективності, V_{EA} підвищився на 4,31 %, TGF пристрою покращився на 33,9%, а його посилення порівняно зі звичайним. Моделювання виконане з урахуванням параметрів 45 нм вузла відповідно до дорожньої карти ITRS для високошвидкісних додатків та низькоенергетичних схем.

Ключові слова: GS-DG-FinFET, Спейсерна інженерія, Внутрішні ємності, High-*K*, SCEs.