JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. **11** No 4, 04022(5pp) (2019)

ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том **11** № 4, 04022(5cc) (2019)

An Analogue Multiplier Using Carbon Nanotube Field-effect Transistor Technology

Seyedehsomayeh Hatefinasab*

CENIMAT, Department of Materials Science, Faculty of Science and Technology, NOVA University of Lisbon, 2829-516 Caparica, Portugal

(Received 23 April 2019; revised manuscript received 02 August 2019; published online 22 August 2019)

The endeavor to overcome problems of complementary metal oxide semiconductor technology (CMOS) makes the advent of carbon nanotube field-effect transistor (CNTFET). Improvement of carbon nanotube field-effect transistor structure leads to higher mobility and electrostatics of gate electrons. Therefore, many analog circuits are now designed based on carbon nanotube field-effect transistor technology. This paper presents a low power current mode four-quadrant analog multiplier based on CNTFET and CMOS technologies. All simulations were done with the synopsys Hspice simulator using 32 nm CNTFET model from Stanford University and 32 nm CMOS from PTM library at a supply voltage of 3.3 V. It was shown that the simulation of a multiplier based on carbon nanotube field-effect transistor technology performs better than a multiplier based on CMOS technology.

Keywords: Carbon nanotube field-effect transistor, Analog multiplier, Low power, Single-walled CNT.

DOI: 10.21272/jnep.11(4).04022 PACS number: 85.35.Kt

1. INTRODUCTION

CMOS (complementary metal oxide semiconductor) technology has continued to scale down below 32 nm. A reduction in the size of transistors may cause several problems in nanoscale. Therefore, the need for new technologies to improve the structure of nanoscale transistor increases a lot. Carbon nanotube field-effect transistor (CNTFET) is one of the best structures of nanoscale transistors. The thermal and mechanical characteristics of CNTs, such as current density, transconductance and lower parasitic capacitance make this nanotechnology better than other technologies in nanoscale integrated circuit. This creates the platform for many integrated circuits to be simulated based on carbon nanotube field-effect transistor technology such as logic gates in VLSI [1] and analog circuits in radio frequency (RF) devices [2].

One of the basic blocks in analog circuits is a multiplier, and it is the most important part of adaptive filters, modulators, signal processing circuits and fuzzy logic controllers. An ideal multiplier produces a linear output signal, which is obtained from two linear input signals with a constant designated as k [3]. The analog multiplier can be divided into two groups, voltage mode [4] and current mode [5-7].

This paper presents a low-power and high-speed four-quadrant analog multiplier in the current mode based on dual translinear loops using 32 nm CMOS and 32 nm carbon nanotube field-effect transistor technologies. Since different parameters of low-voltage circuits can be improved by enhancing the technology at the nanoscale, carbon nanotube field-effect transistor technology is applied. All the simulations were performed using Hspice with 32 nm CMOS from PTM library and 32 nm carbon nanotube field-effect transistor from Stanford University technologies.

2. BACKGROUND

2.1 The Carbon Nanotube Field Effect Transistor

Single-walled carbon nanotube (SWCNT) is a rolling sheet of graphene with specific direction, which is called chirality vector. Chirality vector shows the angle of the carbon to carbon (c-c) atoms. The length of the chirality vector can be calculated as shown in Eq. (1) [8].

$$C_h = \alpha\sqrt{n_1^2 + n_2^2 + n_1 n_2}, \quad (1)$$

where α is the lattice constant which is equal to 0.249 nm, n_1 and n_2 are pairs of integer numbers which are dependent on the chirality vector. CNT is metallic if $n_1 - n_2 = 3i\left(i \in Z\right)$, and other modes are semiconductor. The tube diameter (D_{CNT}) is determined as shown in Eq. (2) [8].

$$D_{CNT} = \frac{C_h}{\pi}, \quad (2)$$

The structure of a carbon nanotube field-effect transistor is similar to that of a CMOS transistor, but the channel of a carbon nanotube field-effect transistor is CNTs as shown in Fig. 1. Electrons move fast in the CNTs, so the mobility factor increases rapidly as a ballistic transport [9]. However, current leakages reduce because of less parasitic parameters. In a CNTFET, the number of tubes is determined by the drive current.

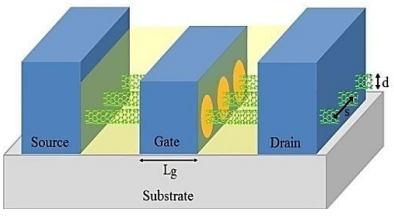


Fig. 1 – Three dimensional CNTFET structure with multiple nanotubes

*s.hatefinasab@campus.fct.unl.pt

There are three types of carbon nanotube field-effect transistors depending on their structures. First, Carbon nanotube field-effect transistors have the same structure as CMOS transistors. This kind of carbon nanotube field-effect transistors does not have any differences between n-channel and p-channel. Fig. 1 shows this kind of carbon nanotube field-effect transistors which is used in this paper. Second, carbon nanotube field-effect transistors are Schottky barrier (SB) with direct tunnels at the junction of the source-channel. The application of this kind of carbon nanotube field-effect transistors is in the RF frequency devices [10, 11]. Third, band-to-band tunneling carbon nanotube field-effect transistors. The current passes through the tunnels. The best application of these transistors is at the low voltage [12].

2.2 Analog Multiplier Design Theory

One of the most important fundamental blocks in analog integrated circuits is a multiplier. The one of the best CMOS based current mode four-quadrant analog multipliers is shown in Fig. 2 [13]. The two signals which are multiplied are not entered directly. The addition and subtraction of two signals (mentioned in (3) and (4)) which are multiplied are entered. If the circuit designed produces the square of each inputs and subtraction of these squares, the output signal of a four-quadrant analog multiplier is multiplication of two signals determined, which is written as shown in Eq. (5). The circuit in Fig. 2 can produce these equations, which are explained in [13]

$$I_{in1} = I_x + I_y, \tag{3}$$

$$I_{in2} = I_x - I_y, \tag{4}$$

$$\left(I_{in1}\right)^2 - \left(I_{in2}\right)^2 = \frac{\left(I_x + I_y\right)^2 - \left(I_x - I_y\right)^2}{I_b} = kI_xI_y, \tag{5}$$

where I_b represents a constant circuit in a multiplier. The use of appropriate input signals makes this circuit operate as a multiplier. All transistors in the inversion region are applied to prove that this circuit works as a CMOS multiplier. If this multiplier is implemented by using carbon nanotube field-effect transistor technology, the above equations can be applied. Also, the relationship between the source-drain current and the gate-source voltage applied in the saturation region of CMOS technology can be applied for carbon nanotube field-effect transistor technology. Therefore, the relationship between the input signals and the output signal of this circuit in carbon nanotube field-effect transistor technology is a multiplier.

2.3 Second Error Effects

This multiplier circuit has many errors. The most important of them are mismatches, channel effect modulation, body effect and mobility degradation, but these errors can be neglected because the value of these errors is smaller than the mean signals in a multiplier. In addition, a multiplier that uses carbon nanotube field-effect transistors has fewer errors introduced by the second error effects of CMOS technology. In this CMOS-based multiplier structure, m_1, m_2 and m_3 transistors can be

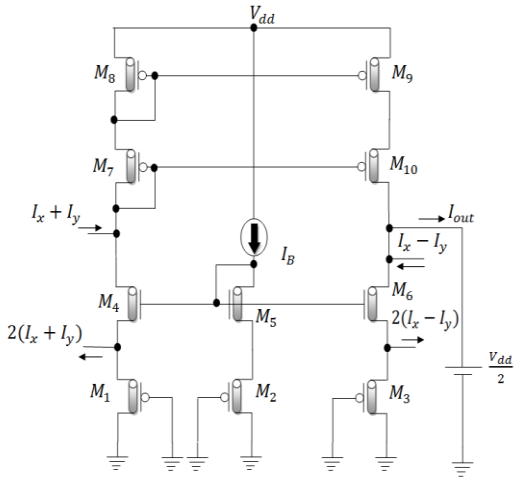


Fig. 2 – A carbon nanotube field-effect transistor based four-quadrant analog multiplier

built in different wells; therefore, the body effect (γ) can become zero in m_1, m_2 and m_3 transistors. Therefore, Eq. (6) can be simplified to $v_{th} = v_{th0}$. But, the body effect is not zero for m_4, m_5 and m_6 transistors because they cannot be built in different wells. Thus there is a different voltage between bulk and source in each m_4, m_5 and m_6 transistors, which means v_{SB} is not zero in these three transistors. The body effect error is important in CMOS-based transistors because this voltage affects the threshold voltage of transistors (v_{th}) as shown in Eq. (6)

$$v_{th} = v_{th0} + \gamma\left(\sqrt{\left|2\varphi_B + v_{SB}\right|} - \sqrt{2\varphi_B}\right), \tag{6}$$

where v_{th0} is the zero bias threshold voltage, φ_B is the bulk potential and γ is the body effect coefficient. In carbon nanotube field-effect transistors, the voltage threshold is inversely proportional to the nanotube diameter (D_{CNT}) as shown in Eq. (7)

$$v_{th} = \frac{0.42}{D_{cnt(n_1,n_2)}}v, \tag{7}$$

Therefore, the threshold voltage can be determined by the nanotube diameter in carbon nanotube field-effect transistors.

Mismatch of transistors is the second most important error. The design of this multiplier is assumed that all the transistors are well matched, $k_n = k_p$. But, in the reality, all transistors are not asymmetrical ($k_n \neq k_p$). In general, in silicon CMOS technology, the NMOS mobility is about 2 or 3 times higher than the PMOS mobility. However, in carbon nanotube field-effect transistors structure, *p*-CNTFET and *n*-CNTFET have the same transport carrier and transistor geometry.

2.4 Leakage

Total power consumption in integrated circuits results in three power consumptions including short circuit current that leads to the power consumption, static power consumption and dynamic power consumption. The appropriate circuit technique can reduce the short circuit current; however, the static power consumption of the

nanoscale circuits is very high. Therefore, traditional methods used to decrease static power are not very effective. In CMOS transistors, static power consumption can be indicated by some factors such as sub-threshold, gate tunneling and reverse-biased junction band-to-band tunneling leakage current. However, in carbon nanotube field-effect transistors, a band-to-band tunneling leakage current is the main factor that determines the current leakage. The current leakage is indicated by the full band gap of the CNTs and the band-to-band tunneling. In Table 1, the power consumptions of the current mode four-quadrant analog multipliers using CMOS and carbon nanotube field-effect transistor are highlighted.

3. SIMULATION RESULTS

The multiplier circuit was simulated with the Synopsys Hspice simulator using 32 nm carbon nanotube field-effect transistor model from Stanford University and 32 nm CMOS from PTM library at a supply voltage of 3.3 V. In both simulations of the multiplier using carbon nanotube field-effect transistor and CMOS, the output nodes of the circuits were connected to a power source voltage with the approximately $v_{dd}/2$ volt. In the multiplier, I_B is a constant current equal to 10 μA. Fig. 3 shows the DC transfer characteristics of a multiplier using 32 nm carbon nanotube field-effect transistor and 32 nm CMOS. These figures show more linearity of the carbon nanotube field-effect transistor based multiplier over a considerable range of inputs (– 10 μA to 10 μA) which have a maximum value that is equal to $\pm I_b$. The output signal range of a multiplier using 32 nm CMOS is between – 7 μA and 7 μA, but the output signal range of a multiplier using carbon nanotube field-effect transistor technology is between – 10 μA and 10 μA. Since the input signal range is equal, the multiplier that uses carbon nanotube field-effect transistors shows a higher range of output signals than the CMOS based multiplier because a carbon nanotube field-effect transistor based multiplier possesses more linearity.

In addition, a better linearity of the multiplier in carbon nanotube field-effect transistor technology can be indicated in the transient simulation. The input signals of a multiplier, I_x and I_y are two sine signals. Fig. 4 shows the output signals and the same input signals, I_x and I_y, for a multiplier in carbon nanotube field-effect transistor and CMOS technologies. As seen in Fig. 4, the output signal of the carbon nanotube field-effect transistor based multiplier looks closer to an ideal output signal than that of the CMOS based multiplier. This better result of a carbon nanotube field-effect transistor based multiplier in comparison with a CMOS based multiplier can be shown by transient error simulation and total harmonic distortion (THD). Fig. 5 shows the error of this multiplier using carbon nanotube field-effect transistor and CMOS in which a carbon nanotube field-effect transistor based multiplier has less error in comparison with a CMOS based multiplier.

THDs of the multiplier using CMOS and carbon nanotube field-effect transistor were calculated in three input signal frequencies such as 1 MHz, 100 MHz and 1 GHz. The simulation results are shown in Fig. 6. Comparison between the proposed multiplier and previous works are shown in Table 1.

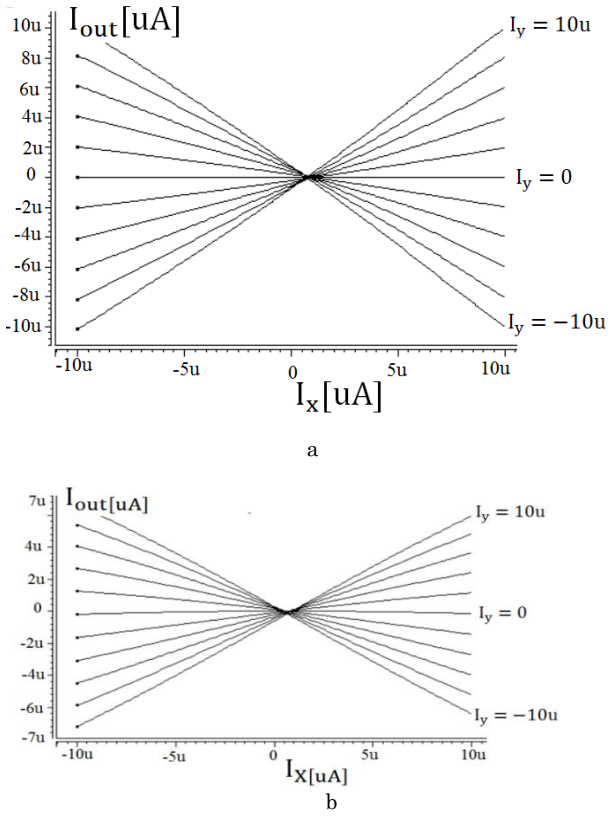


Fig. 3 – (a) DC transfer characteristic of a 32 nm carbon nanotube field-effect transistor based multiplier; (b) DC transfer characteristic of a 32 nm CMOS based multiplier

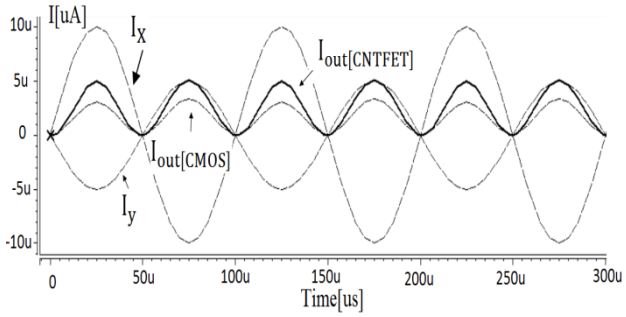


Fig. 4 – Simulation results for a transient analysis

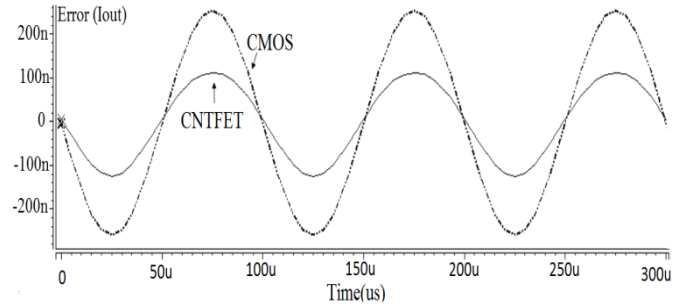
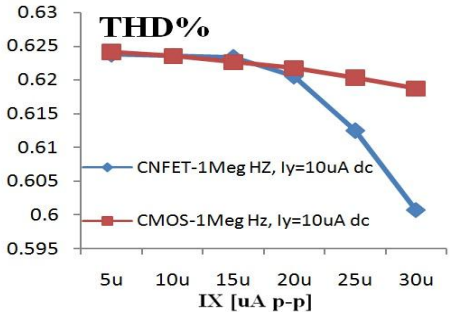


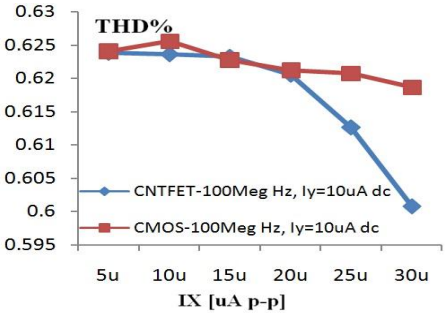
Fig. 5 – Simulation results for error of a transient analysis

Fig. 7 shows the – 3db bandwidths of the multiplier using CNTFET and CMOS technologies. As can be seen, the – 3db bandwidth of the CNTFET based multiplier is 110 GHz, although the bandwidth of the CMOS based multiplier is approximately 2.45 GHz.

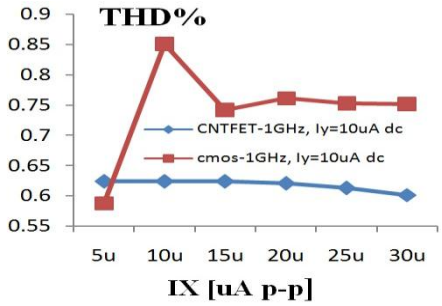
The CNTFET multiplier does not have any attenuation, but the CMOS multiplier has a 5*db* attenuation.



a



b



c

Fig. 6 – (a) Total harmonic distortion versus input currents at 1 MHz, (b) total harmonic distortion versus input currents at 100 MHz, (c) total harmonic distortion versus input currents at 1 GHz (various amplitudes of I_x signal and a fixed amplitude of I_y signal)

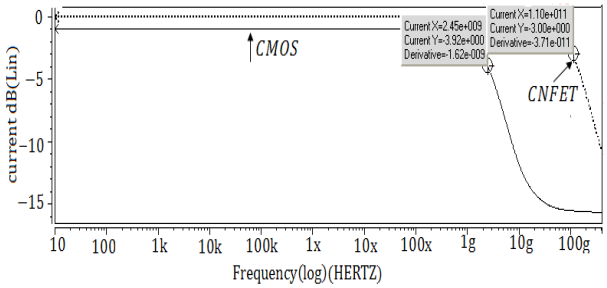


Fig. 7 – Simulation results for – 3*db* bandwidth

Table 1 – A comparison between this work and previous works

Four-quadrantanalogue multiplier	[5]	[6]	[13]	This article (CMOStechn.)	This article (CNTFET techh.)
Technology	0.35 um CMOS	0.35 um CMOS	0.25 um CMOS	32 nm CMOS	32 nm CNTFET
Power[μw]	5.5	340	214	185	99.4
I baise[μA]	0.25	10	10	10	10
V supply[v]	2	3.3	3.3	3.3	3.3
Thd [%]1 MHz,20 μA	1(1 kHz)	0.97	0.96	0.621	0.6205
–3*db* bandwidth	0.2	41.8	533	2450	110 GHz

4. CONCLUSIONS

This paper presents a current mode four-quadrant analog multiplier using CNTFET and CMOS technologies. At the same power supply, the simulations are calculated using the synopsys Hspice simulator. A carbon nanotube field-effect transistor based multiplier circuit has better features in comparison with a CMOS based multiplier, which includes high speed, high linearity, low power consumption in transient and dc simulations. A comparison between this work and previous works shows improvements in many parameters including THD, – 3*db* bandwidth in AC analyzes.

REFERENCES

1. S. Hatefinasab, *J. Nano- Electron. Phys.* **8** No 4, 04061 (2016).
2. B. Heidari, M. Kord Rostami, *IJAENT* **1** No 7, 4 (2014).
3. B. Gilbert, *IEEE J. Solid-State Circuit.* **3** No 4, 365 (1986).
4. C. Chen, Z. Li, *IEEE T. Circuit. Systems II: Express Briefs* **53** No 2, 100 (2006).
5. M. Gravati, M. Valle, G. Ferri, N. Guerrini, L. Reyes, *Proceedings of the 31st European Solid-State Circuits Conference,* 8802542 (Grenoble, France: IEEE: 2005).
6. A. Naderi, A. Khoei, K. Hadidi, H. Ghasemzadeh, *Int. J. Electron. Commun. (AEÜ)* **63** No 9, 769 (2009).
7. F.A. Usmani, M. Hasan, *Microelectron. J.* **41** No 7, 395 (2010).
8. J. Deng, H.-S.P. Wong, *IEEE T. Electron Dev.* **54** No 12, 3186 (2007).
9. P.L. McEuen, M.S. Fuhrer, H. Park, *IEEE T. Nanotechnol.* **1** No 1, 78 (2002).
10. P.A. Gowri Sankar, K. Udhayakumar, *J. Semiconductor.* **35** No 7, 075001 (2014).
11. R. Zarhoun, M.H. Moaiyeri, S.S. Farahani, N. Keivan, *ETRI J.* **36** No 1, 89 (2014).
12. A. Raychowdhury, K. Roy, *IEEE T. Circuit. Syst. I* **54** No 11, 2391 (2007).
13. A. Alikhani, A. Ahmadi, *Int. J. Electron. Commun. (AEÜ)* **66** No 7, 581 (2012).

Аналоговий мультиплікатор з використанням технології CNTFET

Seyedehsomayeh Hatefinasab

CENIMAT, Department of Materials Science, Faculty of Science and Technology, NOVA University of Lisbon, 2829-516 Caparica, Portugal

Зусилля, спрямовані на подолання проблем технологіїкомплементарної структури метал-оксид-напівпровідник(CMOS) зумовили створення польового транзистора на вуглецевих нанотрубках (CNTFET). Удосконалення структури CNTFET призводить до більш високої рухливості та електростатики електронів затвора. Саме тому багато аналогових схем зараз розроблені на основі технології CNTFET. У роботі представлено режим малої потужності з чотириквадрантним аналоговим мультиплікатором на основі технологій CNTFET і CMOS (технологія додаткового шару оксид-метал-напівпровідник). Усі моделювання були виконані із симулятором synopsys Hspice з використанням 32 нм моделі CNTFET із Стенфордського університету і 32 нм моделі CMOS з бібліотеки PTM при напрузі живлення 3.3 В. Було показано, що моделювання мультиплікатора на основі технології CNTFET здійснюється краще, ніж моделювання мультиплікатора на основі технології CMOS.

Ключові слова: Польовий транзистор на вуглецевих нанотрубках, Аналоговий мультиплікатор, Низька потужність, Одностінна CNT.