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Design and Analysis of Ternary D-Latch Using CNTFETs

Anirban Banerjee, Vikash Prasad, Debaprasad Das*

Department of Electronics and Communication Engineering, Assam University, Silchar, India

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Integrated circuit (IC) chips are designed using binary logic. However, over the last two decades the complexity of IC chips has become manifold. This has resulted in large chip area due to large number of interconnections. Hence, large parasitics associated with the interconnections have reduced the speed and increased the power dissipation. These problems can be overcome using multi-value logic (MVL). To design digital circuits based on MVL, it is required to control the threshold voltage of the devices depending on the logic levels. Carbon nanotube field effect transistor (CNTFET) is one such emerging device which is suitable for MVL circuits as the threshold voltage of CNTFET can easily be controlled by changing the diameter of the carbon nanotubes (CNTs). The diameter of the carbon nanotube (CNT) is controlled by varying the chirality of the CNT. Ternary logic is one of the promising multi-value logics where there are three logic levels. In this paper, we have designed a D-latch based on ternary logic using CNTFET. The setup and hold times for the D-latch have been characterized. The delay and power have also been analyzed.

Keywords: CNTFET, MVL, Ternary, D-latch, Setup and hold time.

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1. INTRODUCTION

Digital computation is generally performed based on two value logic i.e., using only two possible states; low (0) and high (1), where there is no other logic level. Multi-value logic (MVL) like ternary or fuzzy logic system permits more than two logic levels. Depending on the number of allowed levels, MVL circuits can be classified as ternary, where there are three logic levels, and quaternary, where there are four logic levels. The number of operations to perform digital computations is generally reduced using MVL due to simplified logic expressions. This results in the reduction of number of devices as well as interconnections which in turn reduces the propagation delay, chip area, and power dissipation. The pin-out problem of synthesizing large chips can also be overcome using MVL.

One of the requirements of designing MVL circuits is to control the threshold voltage of the devices. The MVL circuits are designed using CMOS logic where the threshold voltage of the MOS devices is varied by substrate/body bias. Carbon nanotube field effect transistor (CNTFET) is most suitable for MVL circuits as the threshold voltage of CNTFET can easily be controlled by changing the diameter of the carbon nanotubes (CNTs). The diameter of the carbon nanotube (CNT) is controlled by varying the chirality of the CNT.

Roy et al. in [1] have first proposed the multi-valued logic design using CNTFET. The SPICE compatible model for ballistic CNTFET is developed in this work, where the geometry and operating conditions have been the varied. Navi et al. have designed ternary logic circuits including negative, positive and standard ternary logics in [2] using 32 nm CNTFET technology.

Lombardi et al. have presented the design of ternary logic gates and arithmetic circuits using CNTFET technology in [3]. The authors have also designed ternary memory cell using MOSFET-like CNTFET in [4]. In [5], the design of MVL circuits is presented using pseudo N-type CNTFETs. The design of content addressable memory using MOSFET-like CNTFET is presented in [6].

A ternary D-latch is designed using CNTFET, where the design is implemented at the gate level. In [7], we have shown how ternary logic can be designed using MOSFET-like CNTFET and how the device parameters can be varied to achieve different threshold voltages which is key to the design of MVL circuits.

In this paper, we have designed a D-latch based on ternary logic using MOSFET-like CNTFET. The ternary D-latch is designed using transmission gate (TG) based methodology for 32 nm technology node. The chirality of CNTs is chosen in such a way that the desired threshold voltage is achieved for the ternary operations. The setup and hold times are characterized for the proposed D-latch. The design is implemented in Cadence virtuoso environment.

The rest of our paper is organized as follows. Section 2 describes the basics of MOSFET-like CNTFET and its characteristics. Ternary logic circuits are explained in Section 3. Section 4 presents the design of ternary D-latch. The simulation results and setup and hold time characterization are presented in Section 5. Finally, we summarize our conclusions in Section 6.

2. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

CNT has been one of the emerging nanomaterials, which has excellent electrical, thermal, and mechanical properties. It has a one-dimensional structure made of a rolled graphene sheet. CNTs are classified into three different types: armchair, zigzag, and chiral. The chirality of a CNT is defined by a pair of chiral index (n; m), where n and m are two integers.

For $n = m$, CNT exhibits metallic property whereas for $n - m \neq 3i$ (i is an integer), CNT exhibits semiconducting property.

* dasdebaprasad@yahoo.com

Different CNTFET structures have been proposed by different research groups. In Schottky barrier CNTFET, source/drain metal contacts are made of titanium or cobalt [8]. The nanotube acts as a channel between two metal contacts. In [9], band-to-band tunneling CNTFET (BTBT-CNTFET) is proposed by Appenzeller et al., where the tunneling properties of the nanotube devices have been utilized. Jie Deng et al. have proposed MOSFET-like CNTFET, which has very similar VI characteristics as that of MOSFET [10-12]. In this work, we have used MOSFET-like CNTFET due to its similar VI characteristics as that of the traditional Si-based MOSFETs. The device parameters of the CNTFET used in this work are obtained from [10, 11] and the device model is obtained from [12]. The p-type and *n*-type CNTFET models are created in Cadence virtuoso environment to design the ternary logic gates using this device model. In our model, the threshold voltage varies from 0.289 V to 0.559 V by varying the chirality from (10.0) to (19.0) of the nanotubes. Fig. 1 shows the VI characteristics of n-type CNTFET, where the chiral index *n* varies from 10 to 19. Similarly, VI characteristics of *p*-type CNTFET are also obtained, which have already been illustrated in [6]. In traditional CMOS circuits, sizing of MOSFET is done by varying the channel width of the MOSFET. However, in MOSFET-like CNTFET sizing is achieved by changing the number of tubes.

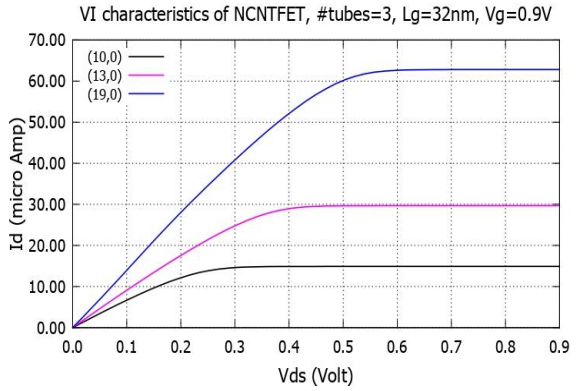

Fig.1 – V-I characteristics of *n*-type CNTFET

Table 1 – Truth table of ternary inverters

Inverter	Input	Output
STI	0	2
	1	1
	2	0
PTI	0	2
	1	2
	2	0
NTI	0	2
	1	0
	2	0

3. TERNARY LOGIC

In ternary logic, there are three logic states: 0 (false), 1 (intermediate) and 2 (true), which correspond to 0 V, 0:5 VDD and VDD, respectively, where, VDD is the power supply voltage.

In ternary logic, there are basically three sets of inverters: simple ternary inverter (STI), positive ternary inverter (PTI), and negative ternary inverter (NTI). The truth table of the different types of inverters in ternary logic is shown in Table 1. The circuit diagram of simple ternary inverter is shown in Fig. 2.

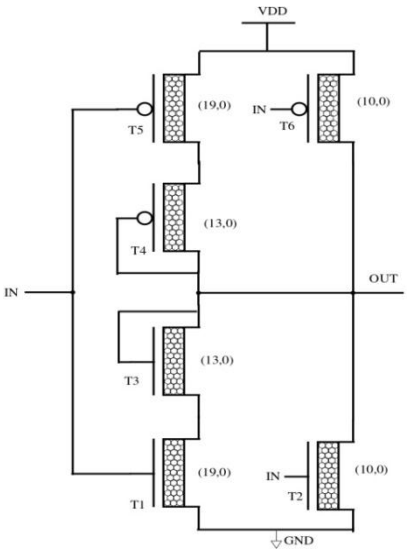

Fig. 2 – Circuit diagram of STI logic

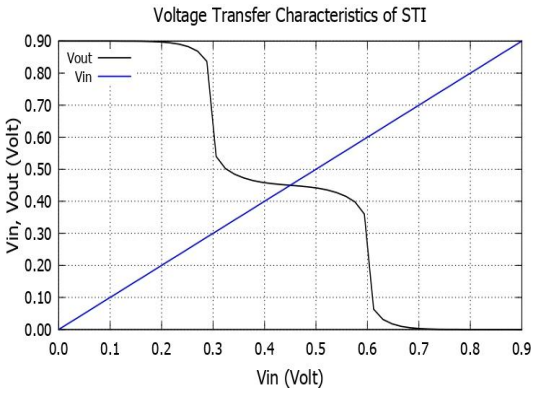

Fig. 3 – Voltage transfer characteristics of STI

The voltage transfer characteristics of STI are shown in Fig. 3. Three logic states 0, 1, and 2 correspond to 0 V, 0.45 V, and 0.9 V, respectively. When the input voltage is below 0.3 V, T6 is ON and T2 is OFF, and we get logic 2 (= 0.9 V) at the output. When the input voltage is above 0.6 V, T2 is ON and T6 is OFF, and we get logic 0 (= 0 V) at the output. When the input voltage is between 0.3 V and 0.6 V, T2 and T6 are OFF, however, T5 and T1 are ON. T3 and T4 are always ON as they are diode connected. Therefore, we get logic 1 (= 0.45 V) at the output. When, $V\text{in} < 0{:}3$ V or $V\text{in} > 0{:}6$ V, though the transistors T1, T3, T4, and T5 are ON, they produce higher resistance path as compared to the pull-up (through T6) and pulldown (through T2). So, the output is either VDD or ground.

4. TERNARY D-LATCH

In this paper, we have designed the ternary D-latch circuit using the conventional CMOS D-latch topology. Fig. 4 shows the ternary D-latch circuit, where the normal inverters are replaced by the STI and normal

transmission gates are replaced by ternary transmission gates. The transmission gates are used to pass the different logic levels (0, 0:5 V_{DD} and V_{DD}) based on the clock inputs. The first STI (STI1) provides the complementary output (Q_b) of the D-latch.

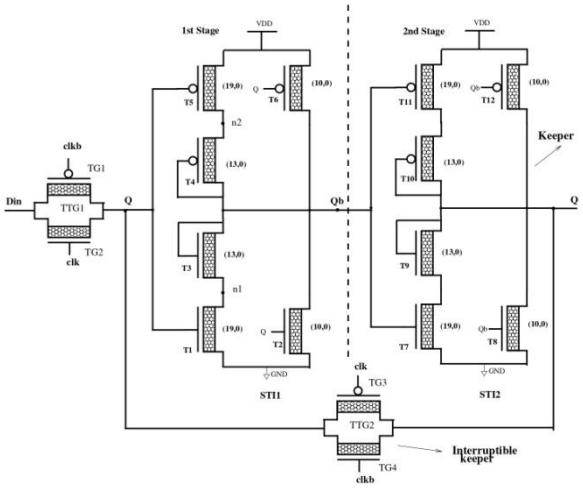

Fig. 4 – Circuit diagram of ternary D-latch

When the clock becomes high, the data input (D_{in}) passes through the first ternary transmission gate (TTG1) and its complement becomes available at the output of the first STI (STI1). However, when the clock goes low, TTG1 remains OFF, and its output becomes high-Z state. In order to avoid the charge loss during this state, a keeper circuit (STI2) is used at the output of the first STI (STI1). The second ternary transmission gate (TTG2) is used in the feedback path to avoid the contention issue as shown in Fig. 4.The first stage of the proposed circuit as shown in Fig. 4 consists of eight CNTFETs with the design parameters as shown in Table 2. The chirality of the CNTFETs is used in such a way that the logic levels corresponding to three ternary logic states pass through the circuit which is explained in the following subsections.

4.1 Case 1: Transfer of Logic Level 0

When the clock is high, the transmission gate TTG1 is ON and it passes the logic from its input to output. When the input of TTG1 is low (logic level 0), the output of TTG1 is also low (i.e., $Q = 0$). The entire operation of the circuit and operating conditions for each transistor are shown in Table 3.

Table 2 – CNTFET design parameters

CNTFET	Chirality (nm)	Diameter (nm)	Threshold voltage (V)
TG1	(19.0)	1.487	– 0.289
TG2	(19.0)	1.487	+ 0.289
T1	(19.0)	1.487	+ 0.289
T2	(10.0)	0.783	+ 0.559
T3	(13.0)	1.018	+ 0.428
T4	(13.0)	1.018	– 0.428
T5	(19.0)	1.487	– 0.289
T6	(10.0)	0.783	– 0.559

Table 3 – Working principle

Input	Clock	TG1	TG2	T1	T2	T3	T4	T5	T6
0	High	ON	ON	OFF	OFF	X	X	ON	ON
0 – 0.5×*V*dd	High	ON	ON	ON	OFF	ON	ON	ON	OFF
0.5×*V*dd – *V*dd	High	ON	ON	ON	ON	X	X	OFF	OFF

The gate terminals of T5/T6 and T1/T2 are connected to the output of transmission gate (TTG1). T1/T2 are OFF, and T5/T6 are ON, so the output of STI1 is high i.e., $Q_b = V_{DD}$. The second STI (STI2) complements the output of first STI (Q_b), so we get logic 0 at Q.

4.2 Case 2: Transfer of Logic Level 0.5 VDD

When the input of transmission gate TTG1 is 0.5 V_{DD}, i.e., 0.45 V, T6 is OFF, T5 is ON, T1 is ON and T2 is OFF. The diode connected CNTFETs T4 and T3 produce a voltage drop of 0.45 V from node n2 to Q_b and from node Q_b to n1 due to threshold voltages of T4 and T3. Therefore, the output voltage becomes 0.45 V (i.e., 0:5 V_{DD}), and we get logic level 1 at Q_b and also at Q.

4.3 Case 3: Transfer of Logic Level VDD

When the input of the transmission gate TTG1 is 0.9 V, i.e., V_{DD}, T6 and T5 are OFF and T1 and T2 are ON. Therefore, the output voltage is pulled down to the ground, and we get logic 0 at Q_b and logic 2 at Q. The ternary D-latch shown in Fig. 4 works when clock input is high, i.e., data transfer takes place when clock is at logic 2. It is also possible to make it work when clock input is low by replacing the clock (clk) and inverted clock (clkb) inputs in the TTG1 and TTG2 circuits.

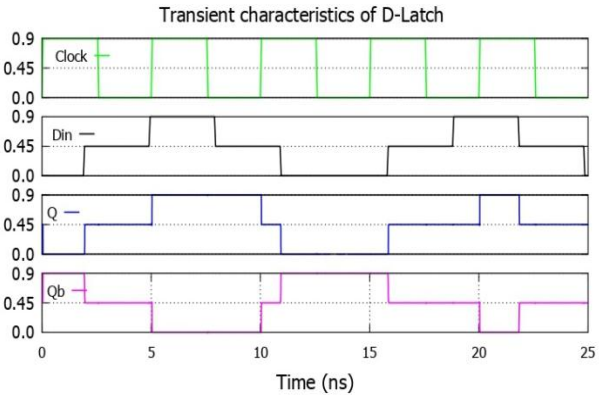

Fig. 5 – Transient characteristics of ternary D-latch

5. SIMULATION RESULTS

The proposed design is implemented using 32 nm technology node. The simulations are performed in Cadence Virtuoso environment. Fig. 5 shows the simulated input and output waveforms of the ternary D-latch. When clock remains high, the D input is passed to Q output and complement of D input is passed to Q_b output. The rise/fall delay of the ternary D-latch is calculated which are shown in Table 4.

Table 4 – Input-output delay of ternary logic based D-latch

Sl. No.	Transition	Rise Delay (ps)
1	0 to 0.5 × V_{DD}	23.88
2	0.5 × V_{DD} to V_{DD}	4.94
Sl. No.	**Transition**	**Fall Delay (ps)**
1	V_{DD} to 0.5 × V_{DD}	23.89
2	0.5 × V_{DD} to 0	4.93

Table 5 – Average delay, power, and PDP of ternary D-latch

Average delay (ps)	Average power (W)	PDP (aJ)
14.41	1.312	18.906

Table 6 – Setup and hold time of ternary logic based D-latch

Sl:No:	Transition	Setup time (ps)	Hold time (ps)
1	0 to 0.5×V_{DD}	20.0	20.0
2	0.5×V_{DD} to V_{DD}	30.0	28.0
Note: Clock -ve edge and data rising edge			

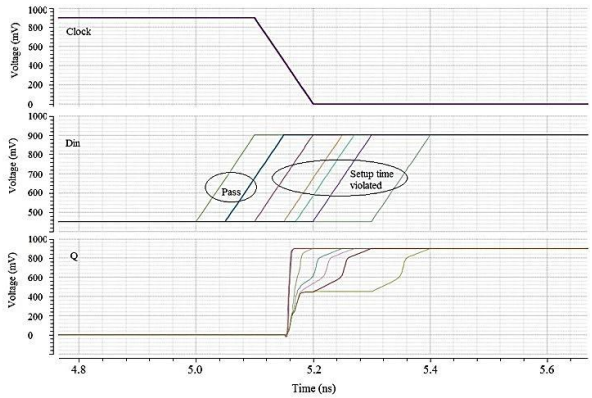

Fig. 6 – Setup time characterization of ternary D-latch

The D-latch is characterized to measure the setup and hold time. Setup time of a latch is the minimum time before the clocking transition; the data must arrive at the input of the latch. On the other hand, the hold time of a latch is the minimum time after the clocking transition the data must not change. Fig. 6 illustrates the setup time analysis for the design. The negative edge of the clock is used for setup time analysis while the data is switched from logic 1 to logic 2 (i.e., 0:5 V_{DD} to V_{DD}). As shown in Fig. 6, the data input is passed to the output for the first two transitions. When the data input is delayed further, it is not passed to the output as indicated for the last five transitions in Fig. 6. It is observed that data must be stable 30 ps before the clock transition to get a valid output at Q. A similar analysis has been performed for setup and hold time analysis for other logic levels and the results are shown in Table 5. Table 6 shows the delay and power values of the proposed design.

6. CONCLUSIONS

We have presented the design of ternary D-latch in this paper. The design is implemented using MOSFET-like CNTFET, where the threshold voltage of the CNTFETs is controlled by controlling the chirality of CNTs. The design of multi-threshold logic circuit using traditional MOS devices requires suitable tuning of the threshold voltages which is difficult to achieve. Our proposed design shows a unique technique to achieve proper tuning of the threshold voltage by suitably changing the chirality of the CNTs, which is the primary requirement of multi-threshold logic circuit design. The proposed ternary D-latch based on CNTFET works perfectly for all the logic levels as desired for ternary operation. The setup and hold time analyses have also been carried out to characterize the design.

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Розробка та аналіз трирівневого D-тригеру на базі польового транзистору з вуглецевих нанотрубок

Anirban Banerjee, Vikash Prasad, Debaprasad Das

Department of Electronics and Communication Engineering, Assam University, Silchar, India

Інтегральні мікросхеми базуються на використанні бінарної логіки. Однак останні два десятиліття складність мікросхем невпинно зростала. Це призвело до великої площі чіпів через велику кількість з'єднань. Отже, великі паразитні ємності, пов'язані з взаємозв'язками, зменшили швидкість і

збільшили розсіювання потужності. Ці проблеми можна подолати за допомогою багатозначної логіки (MVL). Для проектування цифрових схем на основі MVL необхідно контролювати порогову напругу пристроїв в залежності від логічних рівнів. Польовий транзистор з вуглецевих нанотрубок (CNTFET) є одним з таких пристроїв, який підходить для схем MVL, оскільки порогову напругу CNTFET можна легко контролювати шляхом зміни діаметра вуглецевих нанотрубок (CNTs). Діаметр вуглецевої нанотрубки (CNT) контролюється зміною її хіральності. Трирівнева логіка має три логічних рівня і є однією з перспективних багатозначних логік. У даній роботі ми розробили D-тригер на основі трирівневої логіки на базі CNTFET. Охарактеризовано часи встановлення та утримання D-тригеру. Проаналізовано також час затримки і потужність.

Ключові слова: CNTFET, MVL, Трирівневий, D-тригер, Час насичення та утримання.