JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. 11 No 3, 03019(5pp) (2019)
ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том 11 № 3, 03019(5cc) (2019)

Planar Defects Impact on Non-fundamental Efficiency Losses in *mc*-Si Solar Cells

A.V. Prykhodko[1,2]

[1] *Zaporizhzhya State Medical University, 26, Mayakovsky Ave. 69035 Zaporizhzhia, Ukraine*
[2] *Zaporizhzhya National University, 66, Zhukovsky St., 69600 Zaporizhzhya, Ukraine*

(Received 27 August 2018; revised manuscript received 11 June 2019; published online 25 June 2019)

Planar defects can severely limit the efficiency of multicrystalline silicon (*mc*-Si) solar cells for a lot of reasons. The impact of grain boundaries, twins and stacking faults on fill factor losses in *mc*-Si solar cells has been studied. No any clear influences of planar defects presence on parasitic resistances and minority carrier lifetime were observed. The mechanism resulting in an increase of recombination component of *p-n* junction saturation current due to the Suzuki interaction of stacking faults with some metal traces was proposed. The possibilities for useful stacking fault engineering during ingot solidification, its cutting and wafering were discussed. No grain boundary, twin and stacking fault effects on solar cell efficiency losses due to parasitic ohmic resistances were observed. Stacking fault clusters with deformation origin that are capable of accumulating recombination impurities have been detected besides visually observed grain and twin boundaries. When angles between planes of stacking faults and p-n junction are small, the most of depleted layers are occupied by them and recombination component of the saturation current increases significantly that results in the enhancement of efficiency losses.

Keywords: Solar cell, *mc*-Si, Fill factor, Parasitic ohmic resistance, Dark saturation current, Diode ideality factor, Grain boundary, Stacking fault, Twin.

DOI: 10.21272/jnep.11(3).03019 PACS number: 88.40.Jj

1. INTRODUCTION

Despite the benefits of solar cells (SCs) as a next-generation energy source, their high cost per wattage has kept them from achieving widespread use [1, 2]. Cost reduction of photovoltaic material is an important issue in the development of future industrial fabrication of SCs. Multicrystalline silicon is currently dominating at the silicon solar cell (SC) market due to low ingot costs, but its efficiency is limited by extended defects, metal traces and light-induced degradation [3]. The best achievements in 17-18 % efficiency of industrial *mc*-Si SCs [4, 5] is still well below 22.3 ± 0.4 % and 26.7 ± 0.5 % efficiency, which were respectively obtained in designated and aperture illumination areas of multicrystalline and crystalline cells [6].

Two types of efficiency loss processes occur in SCs. Fundamental or unavoidable processes, resulting in SC efficiency limit, include such loss mechanisms as «below E_g», electron thermalisation, electron kinetics, Fermi level and etendue losses [7] that were considered previously [8, 9]. The last three processes are usually grouped into the so-called thermodynamic losses. Non-fundamental or possibly preventable losses at most result in lowering a fill factor that in turn results in the losses of SC maximum power. Fill factor losses generally depend on p-n junction quality and parasitic ohmic resistances [10, 11]. Parasitic series resistance results in most power losses, whereas shunt resistance losses are an order of magnitude less in *mc*-Si SCs [12].

The main problem with low cost *mc*-Si is that it generally contains high concentrations of extended defects such as grain boundaries, twins, dislocations, stacking faults and transition element precipitates formed during ingot solidification [13]. Shunting, recombination, mobility reduction and minority carrier lifetime effects are directly associated with both impurity and structural imperfections in the crystal structure, and hence, increasing SC efficiency losses [14-16]. Despite numerous experimental [17, 18] and theoretical [19, 20] studies that indicate interest in the properties of extended defects in Si, there is relatively limited understanding of the mechanisms for efficiency losses because of their interactions with transition metals.

During the fabrication of Si SCs, many different techniques were proposed to reduce the impact of defects and improve the performance of *mc*-Si material [2, 16, 21, 22]. All of them are defect engineering techniques for removing deleterious defects or neutralization their impact on the SC performance. They will be successful only when defect interaction mechanisms and processes of SC efficiency losses are well known. The impact of planar defects such as grain boundaries, twins and stacking faults on series and shunt resistances, ideality factor and dark saturation current resulting in non-fundamental efficiency losses of *mc*-Si SCs has been studied.

2. EXPERIMENTAL

Multicrystalline silicon wafers of p-type conductivity and 210-230 microns thickness have been used in the present study. They were cut from ingots grown from upgraded metallurgical-grade silicon by the directional crystallization method. Control methods and background impurity content in the multicrystalline silicon have been described earlier [23].

Resistivity and minority carrier lifetime have been measured by non-contact microwave methods using the multifunctional measurement system WT-2000PV. Wafer average resistivity and lifetime were 0.57-1.21 Ohm·cm and 2.2-4.8 μs, respectively. The *mc*-Si SCs have been fabricated by standard screen printing technology with p+ – p back surface field (BSF) on the automatic Schmidt GmbH production line.

 © 2019 Sumy State University

Visually the separate grains and grain boundaries are clearly distinguishable even in completely manufactured SCs [24]. Multiwire wafering creates numerous micro damages along planes close to {111} on the wafer surface and therefore the reflected light intensity depends on crystallographic orientation of the grain in *mc*-Si wafer. Samples with one or a set of one type visually observed crystalline defects were cut from the SC wafers and fragments containing different types of grain and twin boundaries are shown in Fig. 1.

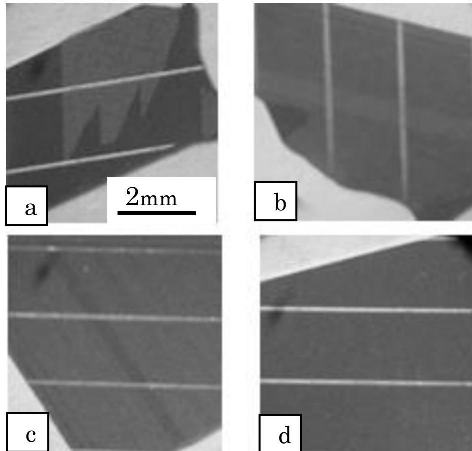

Fig. 1 – SC's fragments with special grain boundaries (a), twin lamellas and boundaries (b), different width twin lamellas (c) and single crystal fragment (d)

Direct and reverse current – voltage curve measurements in the dark were carried out with a thin conducting probe that was mounted on an aluminum "finger". Series resistances and diode characteristics were determined and analyzed using the previously described model [25] based on ***I-V*** curve empirical equation of the one junction solar cell:

$$J(U) = J_0 \times (e^{\frac{q\times(U-J\times R_{ser})}{AkT}} - 1), \qquad (1)$$

where J is the *p-n* junction current density; U is the applied voltage; J_0 is the dark saturation current density; q is the electron charge; R_{ser} is the series resistance; A is the diode ideality factor (diode coefficient).

According to the model [25] in the previously mentioned equation, leakage through the shunt resistance is not taken into account because it is very insignificant. This assumption has been confirmed earlier [12] by results of testing the industrial batch (1400 SCs) with H.A.L.M. electronic GmbH solar simulator. Shunt resistance leakages at applied voltages of 0.5 and 0.6 V were less than 2 % of the maximum power point current at AM1 spectrum illumination with an integrate power of 1000 W/m^2.

The series parasitic resistances R_{ser} were found from experimental *I-V* characteristics plotted in the «$dU/dJ - 1/J$» coordinates. According to equation (1) the *I-V* plot in these coordinates is a straight line that intersects the Y axis at a point that equal to the parasitic serial resistance of a unit SC area. And its slope is determined by the ratio AkT/q, from which diode ideality factor is easily calculated. Dark saturation current density J_0 was also determined from the experimental *I-V* curves and series resistances R_{ser} that were estimated previously. *I-V* curve in the "$lnJ_0 - (U - J \times R_{ser})$" coordinates is also a straight line that intersects the Y axis at point lnJ_0, and thus the dark saturation current density was determined.

In addition to the diode parameters, minority carrier lifetime was studied. Previously it has been selectively measured for the initial *mc*-Si wafers by a contactless microwave method of photoconductivity decay. And then contact method of the recovery reverse-biased p-n junction (analysis of the *p-n* junction switching transients or the Lax method) was used to measure lifetime in the *p*-region of fully manufactured SC's fragments. Electrical current pulse values and conditions for measuring effective minority carrier lifetime using by the Lax method had been described in detail earlier [24].

The crystal defect studies in multicrystalline silicon have been carried out using a selective etching and optical microscopy. After electrical measurements, a conductive aluminum grid and a non-stoichiometric silicon nitride antireflection coating were removed from the sample surface with hydrofluoric acid solution. All samples were then exposed to selective etching in a solution of hydrofluoric and nitric acids in a ratio of 1:3, and crystallographic defects were observed with an optical microscope.

3. RESULTS AND DISCUSSION

Fill factor defines essentially non-fundamental SC efficiency losses which therefore are called fill factor losses [7]. Parasitic resistances, dark saturation current and ideality factor that the most affect fill factor, and hence on the non-fundamental efficiency losses, have been analyzed on SC's fragments with different planar crystal defects. Dark ***I-V*** curves were measured at forward and reverse bias and the forward data are shown in Fig. 2a, b for some SC's fragments. In "$dU/dJ - 1/J$" and "$lnJ - (U - J \times R_{ser})$" coordinates, all experimental plots are straight lines with high approximation reliability R^2 being no less than 0.99 for all studied samples. This confirms the Steven S. Hegedus approach [25] and shunt resistance influence can be ignored. Thus, the empirical equation (1) is well suited for ***I-V*** curve of *mc*-Si SCs and it may be successfully used to find the series resistance and diode parameters.

Parasitic series resistance per 1 sq. cm of SC area, diode ideality factor and dark saturation current density have been found by using the plots in Fig. 2a, b following the procedures described above.

In addition, parasitic shunt resistance and minority carrier lifetime for *p*-region were measured on the same fragments. Studied parameters of SC's fragments with different planar defects are given in Table 1. Also values for single-crystal fragment without any visually observable boundaries (one grain) are presented.

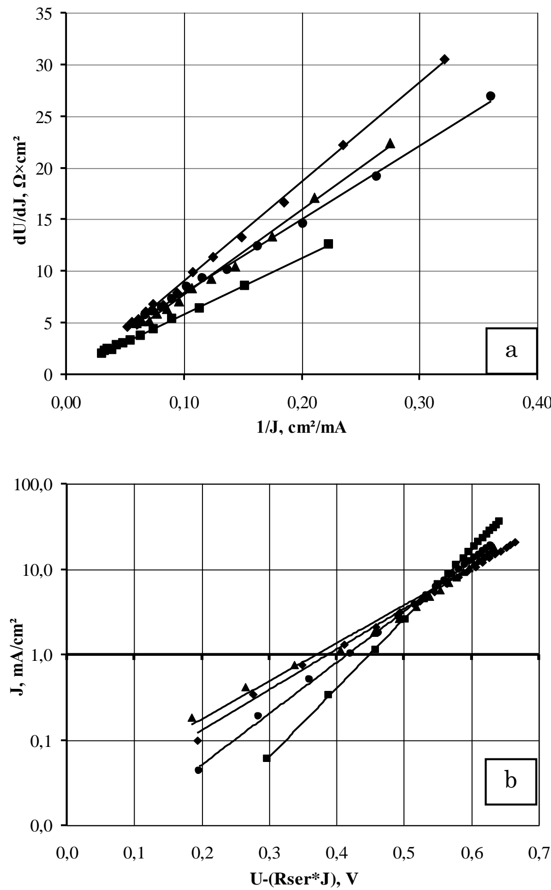

Fig. 2 – Forward $I(V)$ data of SC's fragments with special grain boundaries (■), twin lamellas and boundaries (●), different width twin lamellas (♦) and single crystal fragment (▲)

The parasitic resistances of SC's fragments with different boundaries vary randomly. However, theirvalues do not exceed the intervals 0.3-52.4 kΩ·cm^2 for shunt and 0.12-1.03 Ω·cm^2 for series resistances of whole 156 × 156 mm^2 cells that were found in testing an industrial lot of 1400 *mc*-Si SCs [12]. No significantly influences of grain and twin boundaries on series resistance were detected. Also, p-n junction shunting by the filamentary carbides SiC which are often precipitated at the grain boundaries [26] was not observed. The relation of series and shunt resistances turned out to be small enough so that shunt resistance neglection in equation (1) does not lead to significant inaccuracy.

Unexpectedly the highest dark saturation current density J_0 was observed in single-crystal fragments consisting of one silicon grain. It is about two orders of magnitude greater than the current density of fragments with a special grain boundary, and several times higher than the saturation current density of SC's fragments with random boundaries and twin lamellas.

The ideality factors of a *p-n* junction were determined twice from dependences in Fig. 2 a, b for each fragment, and as follows from Table 1, they hardly differ. Whereas A factors of fragments with different planar defects are significantly different. It also follows from Table 1 data that dark current density J_0 increases drastically with increasing diode coefficient. Current density dependence on the ideality factor A is shown in Fig. 3. Reliable linear correlation between logarithm of dark saturation current density and ideality factor A^{-1} with the reliability of approximation 0.996 was observed. Thus exponential dependence of dark saturation current on the p-n junction ideality factor [11], that has been observed experimentally for 156 × 156 mm^2 SCs produced from multicrystalline "solar grade" silicon [12], keep to remain and for SC's fragments with different planar defects.

Table 1 – Electrical parameters of SC's fragments with various planar defects

Defects	R_{sh}, kΩ·cm^2	R_{ser}, Ω·cm^2	R_{ser}/R_{sh} ×10^5	J_0, μA/cm^2	A (Fig. 2a)	A (Fig. 2b)	τ, μs
Special grain boundaries	1.8	0.39	2.2	0.2	2.08	2.07	2.5
Twin lamellas and boundaries	3.4	0.75	2.2	3.2	2.80	2.80	1.8
Different width twin lamellas	3.0	0.21	0.7	6.1	2.97	2.97	1.6
Single crystal fragments	2.3	0.46	2.0	22.5	3.79	3.77	3.0

In addition, minority charge carrier lifetimes for the p-region of SC fragments with the grain and twin boundaries as well as without them are presented in Table 1. The obtained lifetime values by the Lax method were slightly less than 2.2-4.8 μs that were observed previously for initial multicrystalline silicon wafers by photoconductivity decay microwave method [23]. In the Lax method used here, minority charge carrier injection occurs directly into the inner p-region of diode from the highly doped n+-region. Therefore, surface recombination effect on the lifetime measurement results is much less than in photoconductivity decay method. However, the lifetime values that were obtained with both methods turned out to be approximately the same. Recombination at multicrystaline wafer surface does not significantly affect the minority carrier lifetime, since there are also numerous grain and twin boundaries that can be potential areas of increased recombination [27-29].

And also, thermal treatments during SC manufacturing did not result in changing the recombination activity of grain or twin boundaries and state of the recombination centers, which are formed by metal traces. The selective etching and metallography were used to find out the possible reasons for this.

Numerous stacking faults shown in Fig. 4 were found in all SC's fragments besides visually observed boundaries and twins. They are located most often at small angles to the wafer surface and therefore occupy extended areas of *p-n* junction depletion zone. Most

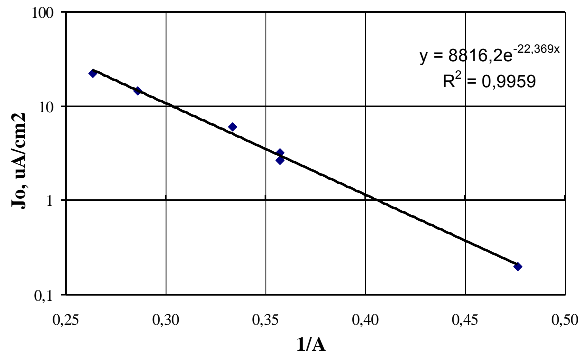

Fig. 3 – Saturation current density J_0 vs ideality factor A^{-1}

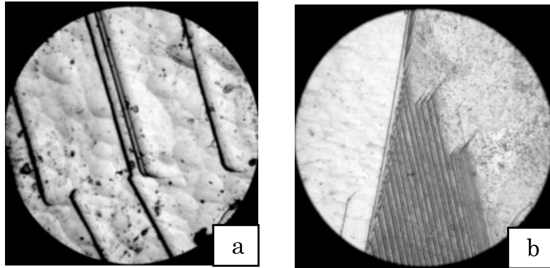

Fig. 4 — Single (a) and numerous (b) stacking faults; a – ×250, b – ×200

likely these stacking faults are having a deformation origin, as indicated by the presence of parallel stacking fault clusters (Fig. 4b). Thermal stresses arise inside the ingot during its solidification and cooling. Since slip lines and bands were not detected, probably the ingot temperature and stresses that needed for macroscopic movement of dislocations have not been achieved. But internal ingot temperature can be sufficient for stress relaxation through the low-temperature deformation mechanisms such as twinning and stacking fault formation. Twin lamellas and single twin boundaries can be seen visually at the wafer surface after multicrystalline ingot cutting (Fig. 1b, c), and the stacking fault clusters were revealed by an optical microscopy after selective etching (Fig. 4).

Single stacking faults (Fig. 4a) were present at all SC's fragments that have been studied. While dense clusters of the parallel stacking faults (Fig. 4b) were detected only for a single-crystal fragments that were free of twin and grain boundaries. It was established [27, 28, 30] that in themselves the stacking faults and special boundaries with a low density of coincidence lattice points $\Sigma3$-$\Sigma9$ do not have appreciable recombination activity, but they change locally the cubic symmetry of silicon crystal lattice to hexagonal. Due to the Suzuki interaction, these local regions might accumulate atoms of recombination metal traces Co, Mg, Te, Ti, Zn those per se crystallize into lattices with hexagonal symmetry.

Thereby, there may be many recombination centers in the depletion zone that accumulated by numerous stacking faults lying at small angles to the p-n junction and hence the recombination component of saturation current will increase. As a result, both ideality factor A and saturation current enlarge for the single-crystal SC's fragments (one grain), but minority charge carrier lifetime at low-resistance p-region does not change noticeably (Table 1). Despite the fact that ideality factor increase leads to fill factor rise (see eq. (1)), simultaneous exponential increase of dark saturation current results in SC efficiency losses [12].

4. CONCLUSIONS

$I(V)$ curves of SC's fragments with grain and twin boundaries, as well as of single-crystal fragments, may be described as highly successful by the empirical diode equation, which has been obtained with concentrated series [11] and infinitely high shunt [25] resistance approximations. No grain boundary, twin and stacking fault effects on the SC efficiency losses due to parasitic ohmic resistances were observed.

Stacking fault clusters with deformation origin that are capable of accumulating recombination impurities have been detected besides to visually observed grain and twin boundaries. When angles between planes of stacking faults and *p-n* junction are small, the most depleted layers are occupied by them and recombination component of the saturation current increases significantly that results in the enhancement of efficiency losses.

Defect engineering to control both stacking faults arising during *mc*-Si ingot solidification and their orientation relative to the *p-n* junction during ingot cutting and brig wafering, might be the successful ways to reduce *mc*-Si SC efficiency losses.

ACKNOWLEDGMENTS

The author would like to express his sincere gratitude to Millinet Solar Co. R&D group (Republic Korea) for the kindly provided solar cells for this study, to all laboratory personnel of metals physics department of Zaporizhzhya National University and Mrs. T.G. Tantsura personally for the services and continued assistance in carrying out metallographic studies.

REFERENCES

1. Xin Gu, Xuegong Yu, Kuanxin Guo, Lin Chen, Dong Wang, Deren Yang, *Sol. Energ. Mat. Sol. C.* **101,** 95 (2012).
2. S. Woo, M.Bertoni, K. Choia, S. Nama, S. Castellanos, D. M. Powell, T. Buonassisi, H. Choi, *Sol. Energ. Mat. Sol. C.* **155,** 88 (2016).
3. O.A. Al-Ani, A.M.A. Sabaawi, J.P. Goss, N.E.B. Cowern, P.R. Briddon, M.J. Rayson, *Sol. St. Phen.* **242,** 96 (2016).
4. K.M. Park, M.B. Lee, S.Y. Choi, *Sol. Energ. Mat. Sol. C.* **132,** 356 (2015).
5. Y.M. Yang, A. Yu, B. Hsu, W.C. Hsu, A. Yang, C.W. Lan, *Prog. Photovolt: Res. Appl.* **23** No3, 340 (2015).
6. A.M. Green, Y. Hishikawa, E.D. Dunlop, D.H. Levi, J. Hohl-Ebinger, A.W.Y. Ho-Baillie, *Prog. Photovolt: Res. Appl.* **26,** 3 (2018).
7. L.C. Hirst, N.J. Ekins-Daukes, *Prog. Photovolt: Res. Appl.* **19** No3, 286 (2011).
8. P.T. Landsberg, V. Badescu, *J. Phys. D: Appl. Phys.*, **33** No22, 3004 (2000).
9. T. Markvart, *Appl. Phys. Lett.* **91** No6, 064102 (2007).
10. S. Gatz, T. Dullweber, R. Brendel, *IEEE J. Photovolt.* **1**

No1, 37 (2011).
11. A.L. Fahrenbruch, R.H. Bube, *Fundamentals of solar cells. Photovoltaic solar energy conversion* (Moscow: Energoatomizdat Publishers: 1987).
12. A.V. Prykhodko, *J. Nano- Electron. Phys.* **7** No3, 03007 (2015).
13. S. Myers, M. Seibt, W. SchroËter, *J. Appl. Phys.* **88**, No7, 3795 (2000).
14. J. Bauer, O. Breitenstein, A. Lotnyk H. Blumtritt, In: *Proceedings of the 22nd European Photovoltaic Solar Energy Conference*, 994 (Milan: Italy: 2007).
15. A.A. Istratov et al., *J. Appl. Phys.* **94**, No10, 6552 (2003).
16. R. Raghunathan, E. Johlin, J.C. Grossman, *Nano Letters* **14**, No9, 4943 (2014).
17. M. Rumler. M. Rumler, M. Rommel, J. Erlekampf, M. Azizi, T. Geiger, A.J. Bauer, E. Meißner, L. Frey, *J. Appl. Phys.* **112**, No3, 034909 (2012).
18. V Naumann, D. Lausch, A. Graff, M. Werner, S. Swatek, J. Bauer, A. Hähnel, O. Breitenstein, S, Großer, J. Bagdahn, C. Hagendorf, *Phys. Status Solidi RRL* **7**, No5, 315 (2013).
19. J. Zhang, C.-Z. Wang, K.-M. Ho, *Phys. Rev. B* **80,** No 7, 174102 (2009).
20. A.Al-Ani Oras, A.M.A. Sabaawi, J.P. Goss, N.E.B. Cowern, P.R. Briddon, M.J. Rayson, *Sol. St. Phen.* **242**, 96 (2016).
21. N.E. Grant, F.E. Rougieux, D. Macdonald *Solid State Phenomena* **242**, 126 (2016).
22. J Hofstetter, C. del Cañizo, H. Wagner, S. Castellanos, T. Buonassisi, *Prog. Photovolt: Res. Appl.* **24**, No3, 122 (2016).
23. А.В. Приходько, *Изв. Вузов. Материалы электрон. техники* No1, 49 (2010).
24. А.В. Приходько, *Изв. Вузов. Материалы электрон. техники* No4, 8 (2008).
25. S.S. Hegedus, *Prog. Photovolt: Res. Appl.* **5**, No3, 151 (1997).
26. J. Bauer, O. Breitenstein, A. Lotnyk, H. Blumtritt, *22nd European Photovoltaic Solar Energy Conference,* **994**,(Milan: Italy: 2007).
27. J. Chen, D. Yanga, Z. Xi, *J. Appl. Phys.* **97** No3, 033701.1 (2005).
28. J. Chen, T. Sekiguchi, R. Xie, P. Ahmet, T. Chikyo, D. Yang, S. Ito, F. Yin, *Scr. Mater.* **52**, 1211 (2005).
29. A. Zuschlag, G. Micard, J. Junge, *33rd IEEE Photovoltaic Specialists Conference*. Proceedings. 4P (2008).
30. A. Cuevas, A. Cuevas, M. Stocks, S. Armand, M. Stuckings, A. Blakers, *Appl. Phys. Lett.* **70** No8, 1017 (1997).

Вплив двовимірних дефектів на нефундаментальні втрати ефективності в сонячних елементах із мультикристалічного кремнію

О.В. Приходько[1,2]

[1] *Запорізький державний медичний університет, пр. Маяковського, 26, 69035 Запоріжжя, Україна*
[2] *Запорізький національний університет, вул. Жуковського, 66, 69600 Запоріжжя, Україна*

Двовимірні дефекти можуть істотно обмежити ефективність сонячних елементів із мультикристалічного кремнію (*mc*-Si) з багатьох причин. Вивчено вплив границь зерен, двійників і дефектів пакування на втрати фактору заповнення в сонячних елементах із *mc*-Si. Ніяких явних залежностей паразитних опорів і часу життя неосновних носіїв від наявності двовимірних дефектів не було виявлено. Розглянуто механізм, обумовлений взаємодією Сузукі дефектів укладки з деякими металевими фоновими домішками, що призводить до збільшення рекомбінаційної складової струму насичення *p-n* переходу. Можливості корисного управління виникненням і властивостями дефектів пакування при кристалізації злитку та його розрізанні на пластини було обговорено. Не спостерігалося впливу меж зерен, двійників та дефектів пакування на втрати ефективності сонячних елементів через паразитні омічні опори. Крім візуально спостережуваних меж зерна і двійників, виявлені кластери деформаційних дефектів пакування, які здатні накопичувати рекомбінаційні домішки. Коли кути між площинами дефектів пакування і *p-n* переходом малі, то більша частина збідненого шару зайнята ними, а рекомбінаційна складова струму насичення істотно зростає, що призводить до підвищення втрат ефективності.

Ключові слова: Сонячний елемент, *mc*-Si, Фактор заповнення, Паразитний омічний опір, Темновий струм насичення, Коефіцієнт ідеальності діоду, Міжзеренні границі, Дефект пакування, Двійник.